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ATP AW12M7218BLK0MW

4GB DDR3-1600 Wide Temperature UNBUFFERED ECC SODIMM

DESCRIPTION

The ATP AW12M7218BLK0MW is a high performance 4GB DDR3-1600 Industrial Grade Unbuffered ECC SODIMM SDRAM memory module. It is organized as 512M x 72 in a 204-pin Small Outline Dual-In-Line Memory Module (SODIMM) package. The module utilizes nine 512Mx8 DDR3 SDRAMs in FBGA package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- Operation Temperature(TA): -40°C ~ +85°C
- High Density: 4GB (512M x 72)
- DIMM Rank: 1 Rank
- Cycle Time: 1.25ns (800MHz)
- CAS Latency: 11
- Power supply: 1.5V ± 0.075V
- Internal self calibration through ZQ
- Burst lengths: 8
- Auto & Self refresh
- Asynchronous Reset
- 7.8 μs refresh interval at lower than T_{CASE} 85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Dynamic On Die Termination
- Fly-by topology
- PCB Height: 1.18 inches
- RoHS compliant

| Part No. | Max Freq | Interface |
|-----------------|--------------------------|-----------|
| AW12M7218BLK0MW | 800MHz (1.25ns@CL=11) x2 | SSTL_15 |

PIN DESCRIPTION

| Pin Name | Description | Pin Name | Description |
|----------------|------------------------------|----------|--|
| A0~A9, A11~A15 | Address Inputs | ODT0 | On die termination |
| A10/AP | Address Input/Auto precharge | RAS | Row Address Strobe |
| BA0~BA2 | SDRAM Bank Address | CS0 | Chip Selects |
| CAS | Column Address Strobe | SA0~SA1 | SPD address |
| CK0~CK1 | Clock Inputs, positive line | SCL | Serial Presence Detect (SPD) Clock Input |
| CK0~CK1 | Clock Inputs, negative line | SDA | SPD Data Input/Output |
| CKE0 | Clock Enables | VDD | Core Power |
| DM0~DM8 | Data Masks | VDDSPD | SPD Power |
| DQ0~DQ63 | Data Input/Output | VSS | Ground |
| DQS0~DQS8 | Data strobes | RESET | This signal resets the DDR3 SDRAM |
| DQS0~DQS8 | Data strobes, negative line | WE | Write Enable |
| VREFDQ VREFCA | Input/Output Reference | Event | Temperature sensor Event output |
| A12/BC | Address Input/Burst chop | NC | No Connect |
| VTT | Termination voltage | TEST | Logic Analyzer specific test pin (No connect on SO-DIMM) |
| CB0~CB7 | DIMM ECC Check bits | | |

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PIN ASSIGNMENT

| No. | Designation | No. | Designation | No. | Designation | No. | Designation |
|-----|-------------|-----|-------------|-----|-------------|-----|-------------|
| 1 | VREFDQ | 2 | VSS | 105 | A1 | 106 | A2 |
| 3 | VSS | 4 | DQ4 | 107 | A0 | 108 | BA1 |
| 5 | DQ0 | 6 | DQ5 | 109 | VDD | 110 | VDD |
| 7 | DQ1 | 8 | VSS | 111 | CK0 | 112 | CK1 |
| 9 | VSS | 10 | DQS0 | 113 | CK0 | 114 | CK1 |
| 11 | DM0 | 12 | DQS0 | 115 | VDD | 116 | VDD |
| 13 | DQ2 | 14 | VSS | 117 | A10/AP | 118 | NC |
| 15 | DQ3 | 16 | DQ6 | 119 | BA0 | 120 | NC |
| 17 | VSS | 18 | DQ7 | 121 | WE | 122 | RAS |
| 19 | DQ8 | 20 | VSS | 123 | VDD | 124 | VDD |
| 21 | DQ9 | 22 | DQ12 | 125 | CAS | 126 | ODT0 |
| 23 | VSS | 24 | DQ13 | 127 | CS0 | 128 | NC |
| 25 | DQS1 | 26 | VSS | 129 | NC | 130 | A13 |
| 27 | DQS1 | 28 | DM1 | 131 | VDD | 132 | VDD |
| 29 | VSS | 30 | RESET | 133 | DQ32 | 134 | DQ36 |
| 31 | DQ10 | 32 | VSS | 135 | DQ33 | 136 | DQ37 |
| 33 | DQ11 | 34 | DQ14 | 137 | VSS | 138 | VSS |
| 35 | VSS | 36 | DQ15 | 139 | DQS4 | 140 | DM4 |
| 37 | DQ16 | 38 | VSS | 141 | DQS4 | 142 | DQ38 |
| 39 | DQ17 | 40 | DQ20 | 143 | VSS | 144 | DQ39 |
| 41 | VSS | 42 | DQ21 | 145 | DQ34 | 146 | VSS |
| 43 | DQS2 | 44 | DM2 | 147 | DQ35 | 148 | DQ44 |
| 45 | DQS2 | 46 | VSS | 149 | VSS | 150 | DQ45 |
| 47 | VSS | 48 | DQ22 | 151 | DQ40 | 152 | VSS |
| 49 | DQ18 | 50 | DQ23 | 153 | DQ41 | 154 | DQS5 |
| 51 | DQ19 | 52 | VSS | 155 | VSS | 156 | DQS5 |
| 53 | VSS | 54 | DQ28 | 157 | DM5 | 158 | VSS |
| 55 | DQ24 | 56 | DQ29 | 159 | DQ42 | 160 | DQ46 |
| 57 | DQ25 | 58 | VSS | 161 | DQ43 | 162 | DQ47 |
| 59 | DM3 | 60 | DQS3 | 163 | VSS | 164 | VSS |
| 61 | VSS | 62 | DQS3 | 165 | DQ48 | 166 | DQ52 |
| 63 | DQ26 | 64 | VSS | 167 | DQ49 | 168 | DQ53 |
| 65 | DQ27 | 66 | DQ30 | 169 | VSS | 170 | VSS |
| 67 | VSS | 68 | DQ31 | 171 | DQS6 | 172 | DM6 |
| 69 | CB0 | 70 | VSS | 173 | DQS6 | 174 | DQ54 |
| 71 | CB1 | 72 | CB4 | 175 | VSS | 176 | DQ55 |
| | | | | 177 | DQ50 | 178 | VSS |
| 73 | VSS | 74 | CB5 | 179 | DQ51 | 180 | DQ60 |
| 75 | DQS8 | 76 | DM8 | 181 | VSS | 182 | DQ61 |
| 77 | DQS8 | 78 | VSS | 183 | DQ56 | 184 | VSS |
| 79 | VSS | 80 | CB6 | 185 | DQ57 | 186 | DQS7 |
| 81 | CB2 | 82 | CB7 | 187 | VSS | 188 | DQS7 |
| 83 | CB3 | 84 | VREFCA | 189 | DM7 | 190 | VSS |
| 85 | VDD | 86 | VDD | 191 | DQ58 | 192 | DQ62 |
| 87 | CKE0 | 88 | A15 | 193 | DQ59 | 194 | DQ63 |
| 89 | CKE1 | 90 | A14 | 195 | VSS | 196 | VSS |
| 91 | BA2 | 92 | A9 | 197 | SA0 | 198 | Event |
| 93 | VDD | 94 | VDD | 199 | VDDSPD | 200 | SDA |
| 95 | A12/BC | 96 | A11 | 201 | SA1 | 202 | SCL |
| 97 | A8 | 98 | A7 | 203 | VTT | 204 | VTT |
| 99 | A5 | 100 | A6 | | | | |
| 101 | VDD | 102 | VDD | | | | |
| 103 | A3 | 104 | A4 | | | | |

Notes1: This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

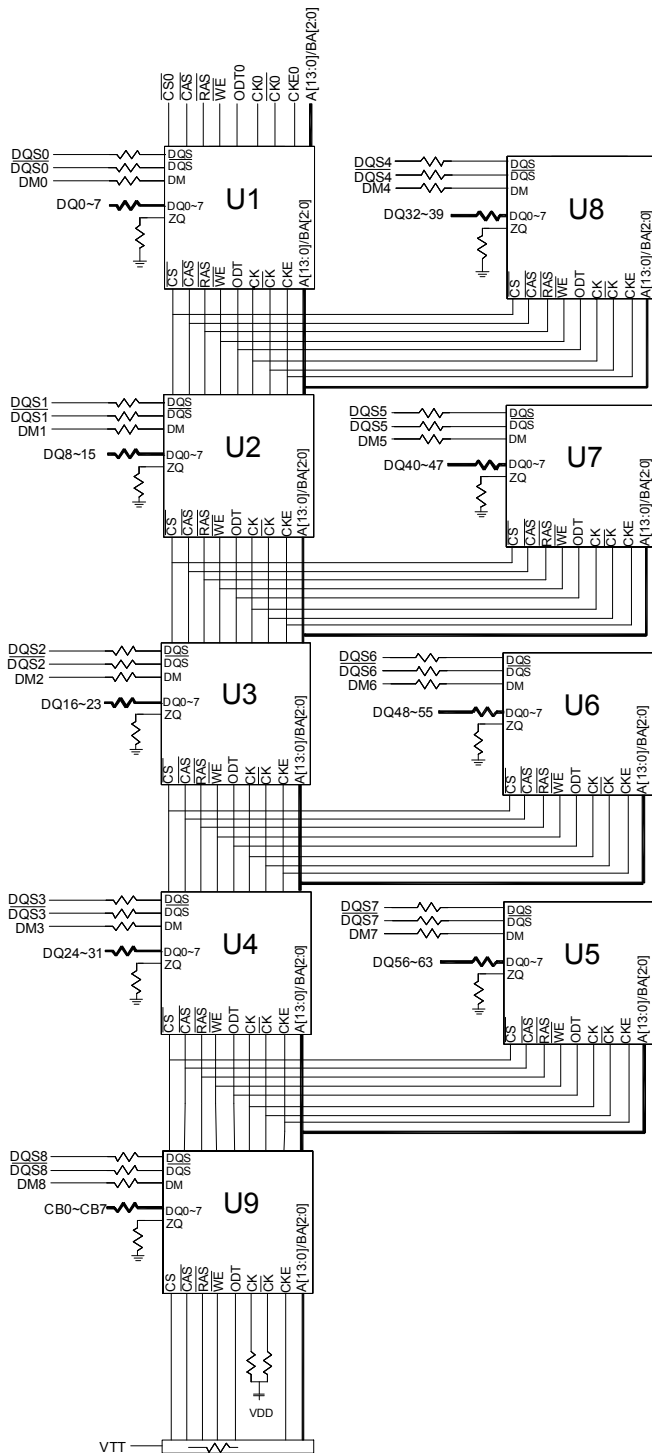
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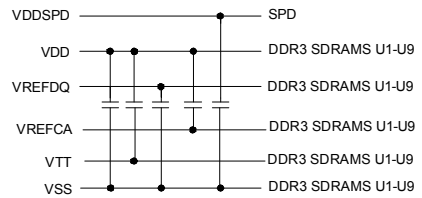
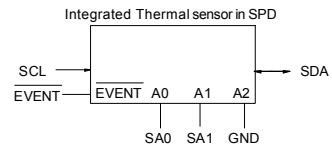


ATP AW12M7218BLK0MW

FUNCTIONAL BLOCK DIAGRAM



Serial PD w/ integrated Thermal sensor



- BA0-BA2 → DDR3 SDRAMs U1-U9
- A0-A14 → DDR3 SDRAMs U1-U9
- RAS → DDR3 SDRAMs U1-U9
- CAS → DDR3 SDRAMs U1-U9
- WE → DDR3 SDRAMs U1-U9
- RESET → DDR3 SDRAMs U1-U9
- CK0 → DDR3 SDRAMs U1-U9
- CK0 → DDR3 SDRAMs U1-U9
- CK1 →
- CK1 →

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ABSOLUTE MAXIMUM DC RATINGS

| Item | Symbol | Rating | Units | Notes |
|---|-------------------|----------------|-------|-------|
| Voltage on V_{DD} pin relative to V_{SS} | V_{DD} | -0.4V ~ 1.975V | V | 1 |
| Voltage on V_{DDQ} pin relative to V_{SS} | V_{DDQ} | -0.4V ~ 1.975V | V | 1 |
| Voltage on any pin relative to V_{SS} | V_{IN}, V_{OUT} | -0.4V ~ 1.975V | V | 1 |
| Storage Temperature | T_{STG} | -55 to +100 | °C | 1 |
| Operating Temperature | T_{CASE} | -40 to +95 | °C | 1,2,3 |
| | T_A | -40 to +85 | °C | 1,4,5 |

Note:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (Refresh interval =3.9 μ s) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.
4. Both temperature specifications must be satisfied.
5. Operating ambient temperature surrounding the package.

AC & DC OPERATING CONDITIONS (SSTL- 15)

Recommended operating conditions

| Item | Symbol | Min. | Typical | Max. | Units |
|--|---------------|-------------------|------------------|-------------------|-------|
| Supply Voltage | V_{DD} | 1.425 | 1.5 | 1.575 | V |
| Supply Voltage for Output ⁴ | V_{DDQ} | 1.425 | 1.5 | 1.575 | V |
| VREFCA(DC) | I/O | 0.49 * V_{DDQ} | 0.50 * V_{DDQ} | 0.51 * V_{DDQ} | V |
| VREFDQ(DC) | I/O | 0.49 * V_{DDQ} | 0.50 * V_{DDQ} | 0.51 * V_{DDQ} | V |
| Input High Voltage (DC) | V_{IH} (DC) | $V_{REF} + 0.100$ | - | V_{DD} | V |
| Input High Voltage (AC) | V_{IH} (AC) | $V_{REF} + 0.175$ | - | - | V |
| Input Low Voltage (DC) | V_{IL} (DC) | V_{SS} | - | $V_{REF} - 0.100$ | V |
| Input Low Voltage (AC) | V_{IL} (AC) | - | - | $V_{REF} - 0.175$ | V |

Note:

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
2. Peak to peak AC noise on V_{REF} may not exceed $\pm 2\%$ V_{REF} (DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDL} tied together.

RELIABILITY

| MTBF @25 °C (Hours) ¹ | FIT @ 25 °C ² | MTBF @40 °C (Hours) ¹ | FIT @ 40 °C ² |
|----------------------------------|--------------------------|----------------------------------|--------------------------|
| 12,454,000 | 87 | 6,085,000 | 164 |

Note:

1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours.

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IDD SPECIFICATION PARAMETER & POWER CONSUMPTION

(IDD values are for full operating range of Voltage and Temperature)

| Symbol | Proposed Conditions | Value | Units |
|--------|--|-------|-------|
| IDD0 | Operating one bank active-precharge current; CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Timing table ; BL: 8; AL: 0/ CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 500 | mA |
| IDD1 | Operating one bank active-read-precharge current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Timing table ; BL: 8; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 590 | mA |
| IDD2P0 | Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit | 160 | mA |
| IDD2P1 | Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Timing table; BL: 8); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit | 290 | mA |
| IDD2N | Precharge standby current; CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog- gling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 290 | mA |
| IDD2NT | Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog- gling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers | 350 | mA |
| IDD2Q | Precharge quiet standby current; CKE: High; External clock: On; tCK, CL: see Timing table; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0 | 290 | mA |
| IDD3P | Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0 | 340 | mA |
| IDD3N | Active Standby Current CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog- gling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 340 | mA |
| IDD4R | Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Timing table; BL: 8; AL: 0; /CS: High between RD; Command, Address, Bank Address Inputs: par- tially toggling ; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 1,410 | mA |
| IDD4W | Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: par- tially toggling ; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH; | 1,130 | mA |
| IDD5B | Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Timing table ; BL: 8; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 1,400 | mA |
| IDD6 | Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normale); CKE: Low; External clock: Off; CK and CK: LOW; CL: see Timing table ; BL: 8; AL: 0; /CS, Command, Address, Bank Address, Data IO: FLOATING; DM:stable at 0; Bank Activity: Self- Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: FLOATING | 180 | mA |
| IDD7 | Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Timing table ; BL: 8; AL: CL-1; /CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one ; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; | 1,980 | mA |
| PDIMM | Power Consumption per DIMM System is operating at 800 MHz clock with VDD = 1.5V. This parameter is calculated at a common loading. | 2,310 | mW |

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TIMING PARAMETER

| Parameter | Symbol | DDR3-1600 | | Units |
|--|-----------|-----------------------------|---------|------------------|
| | | min | Max | |
| Clock cycle time at CL=11, CWL=8 | tCK | 1.25 | <1.5 | ns |
| Internal read command to first data | tAA | 13.75(13.125 ²) | 20 | ns |
| ACT to internal read or write delay time | tRCD | 13.75(13.125 ²) | | ns |
| PRE command period | tRP | 13.75(13.125 ²) | | ns |
| ACT to ACT or REF command period | tRC | 48.75(48.125 ²) | | ns |
| ACTIVE to PRECHARGE command period | tRAS | 35 | 9*tREFI | ns |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | tCK |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | tCK |
| DQS, \overline{DQS} to DQ skew, per group, per access | tDQSQ | | 100 | ps |
| DQ output hold time from DQS, \overline{DQS} | tQH | 0.38 | | tCK |
| DQ low-impedance time from CK, \overline{CK} | tLZ(DQ) | -450 | 225 | ps |
| DQ high-impedance time from CK, \overline{CK} | tHZ(DQ) | | 225 | ps |
| Data setup time to DQS, \overline{DQS} referenced to Vih(ac)/Vil(ac) levels | tDS(base) | 10 | | ps |
| Data hold time to DQS, \overline{DQS} referenced to Vih(ac)/Vil(ac) levels | tDH(base) | 45 | | ps |
| DQS, \overline{DQS} READ Preamble | tRPRE | 0.9 | - | tCK |
| DQS, \overline{DQS} differential READ Postamble | tRPST | 0.3 | | tCK |
| DQS, \overline{DQS} output high time | tQSH | 0.4 | - | tCK |
| DQS, \overline{DQS} output low time | tQSL | 0.4 | - | tCK |
| DQS, \overline{DQS} WRITE Preamble | tWPRE | 0.9 | - | tCK |
| DQS, \overline{DQS} WRITE Postamble | tWPST | 0.3 | - | tCK |
| DQS, \overline{DQS} rising edge output access time from rising CK, \overline{CK} | tDQSCK | -225 | 225 | ps |
| DQS, \overline{DQS} low-impedance time (Referenced from RL-1) | tLZ(DQS) | -450 | 225 | ps |
| DQS, \overline{DQS} high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 225 | ps |
| DQS, \overline{DQS} differential input low pulse width | tDQSL | 0.45 | 0.55 | tCK |
| DQS, \overline{DQS} differential input high pulse width | tDQSH | 0.45 | 0.55 | tCK |
| DQS, \overline{DQS} rising edge to CK, \overline{CK} rising edge | tDQSS | -0.27 | 0.27 | tCK |
| DQS, \overline{DQS} falling edge setup time to CK, \overline{CK} rising edge | tDSS | 0.18 | - | tCK |
| DQS, \overline{DQS} falling edge hold time to CK, \overline{CK} rising edge | tDSH | 0.18 | - | tCK |
| DLL locking time | tDLLK | 512 | | nCK ¹ |
| Internal READ Command to PRECHARGE Command delay | tRTP | max(4nCK,7.5ns) | | |
| Delay from start of internal write transaction to internal read command | tWTR | max(4nCK,7.5ns) | | |
| WRITE recovery time | tWR | 15 | | ns |
| Mode Register Set command cycle time | tMRD | 4 | | nCK ¹ |
| Mode Register Set command update delay | tMOD | max(12nCK,15ns) | | |
| \overline{CAS} to \overline{CAS} command delay | tCCD | 4 | | nCK ¹ |
| Auto precharge write recovery + precharge time | tDAL | tWR + roundup (tRP / tCK) | | nCK ¹ |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | | nCK ¹ |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | max(4nCK,6ns) | | |
| Four activate window for 1KB page size | tFAW | 30 | | ns |
| Command and Address setup time to CK, \overline{CK} referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 45 | | ps |
| Command and Address hold time from CK, \overline{CK} referenced to Vih(ac) / Vil(ac) levels | tIH(base) | 120 | | ps |
| Power-up and RESET calibration time | tZQinitl | 512 | | nCK ¹ |
| Normal operation Full calibration time | tZQoper | 256 | | nCK ¹ |
| Normal operation short calibration time | tZQCS | 64 | | nCK ¹ |
| Exit Reset from CKE HIGH to a valid command | tXPR | max(5nCK, tRFC+ 10ns) | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max(3nCK,6ns) | | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | ns |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOPFD | 2 | 8.5 | ns |
| ODT turn-on | tAON | -225 | 225 | ps |
| RTT_NOM and RTT_WR turn-off time from ODTLoff reference | tAOF | 0.3 | 0.7 | tCK |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | tCK |
| 4Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval | tRFC | 260 | 70,200 | ns |
| Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C) | tREFI | 7.8 | 7.8 | us |
| Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C) | tREFI | 3.9 | 3.9 | us |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | max(5nCK,tRFC+10ns) | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | | nCK ¹ |
| Power Down Entry to Exit Timing | tPD | tCK(min) | 9*tREFI | tCK |
| Write leveling output delay | tWLO | 0 | 7.5 | ns |
| Write leveling output error | tWLOE | 0 | 2 | ns |

1:Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

2: For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match.

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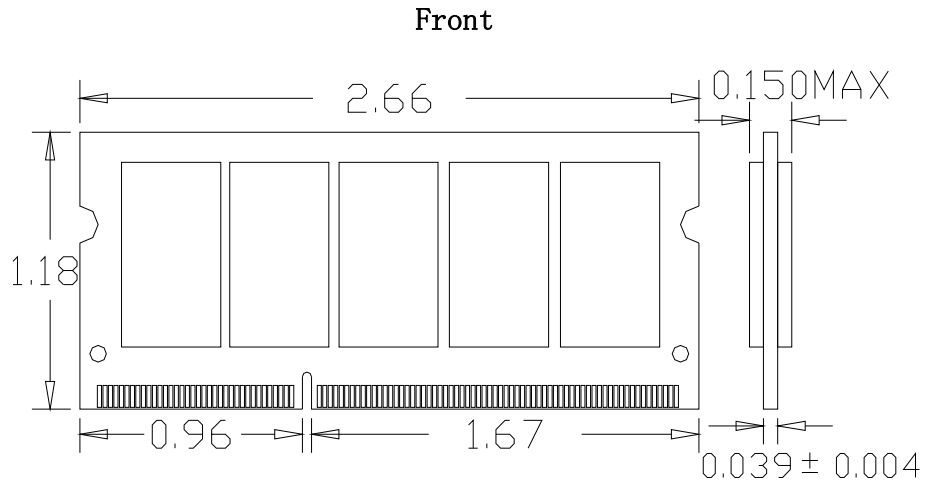


ATP AW12M7218BLK0MW

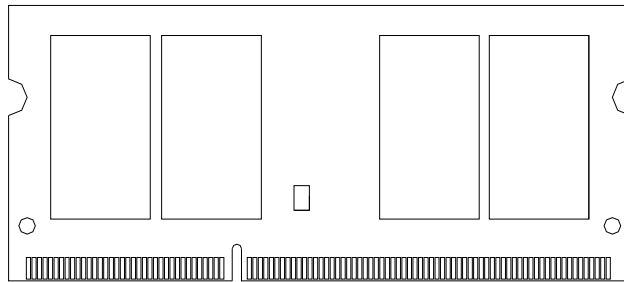
PHYSICAL DIMENSIONS (UNITS IN INCHES)

(Drawing not to scale)

204-pin DIMM



Back



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