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FAIRCHILD SEMICONDUCTOR®

September 2005

RMPA5255
4.9–5.9 GHz WLAN Linear Power Amplifier Module

Features

- Full 4.9 to 5.9 GHz operation
- 34 dB small signal gain
- 230 mA total current at 18 dBm modulated power out
- 2.3% EVM at 18 dBm modulated power out
- 3.3 V collector supply voltage
- Integrated power detector with 20 dB dynamic range
- RoHS compliant 5 x 5 x 1.5 mm leadless package
- Internally matched to 50Ω and DC blocked RF input/output
- Internal DC bias de-coupling
- Optimized for use in 802.11a applications

Description

The RMPA5255 power amplifier module is designed for high performance WLAN applications in the 4.9–5.9 GHz frequency band. The 10 pin, 5 x 5 x 1.5 mm package with internal matching on both input and output to 50Ω, and internal bias network components, allow for extremely simplified integration. An on-chip detector provides power sensing capability. The PA's low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Device

Electrical Characteristics[1] 802.11a OFDM Modulation

(176 µs burst time, 100 µs idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	4.9		5.9	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage		2.9		V
Mirror Supply Current		26		mA
Gain		33		dB
Total Current @ 18dBm Pout		230		mA
EVM @ 18dBm Pout[2]		2.3		%
Detector Output @ 18dBm Pout		450		mV
Detector Threshold[3]		5		dBm

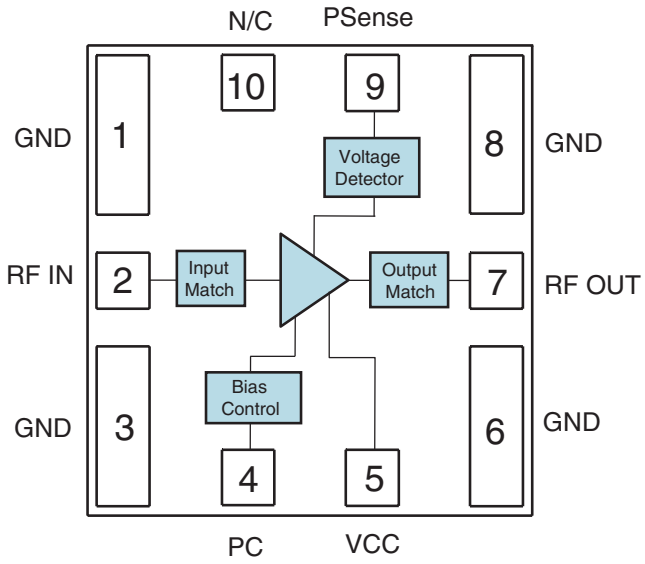
Notes:
1. VCC = 3.3V, VPC = 2.9V, T_A = 25°C, PA is constantly biased, 50Ω system.
2. Percentage includes system noise floor of EVM = 0.8%.
3. P_{OUT} measured at P_{IN} corresponding to power detection threshold.

Electrical Characteristics[1] Single Tone

Parameter	Min	Typ	Max	Units
Frequency	4.9		5.9	GHz
Supply Voltage (VCC)	3.0	3.3	3.6	V
Power Control Voltage (VPC)	2.6	2.9	3.1	V
Gain		33.5		dB
Total Quiescent Current		160		mA
Bias Current at pin VPC[2]		26		mA
P1dB Compression		26		dBm
Current @ P1dB Compression		508		mA
Shutdown Current (VPC = 0V)		<1.0		µA
Input Return Loss		12		dB
Output Return Loss		20		dB
Detector Output at P1dB Compression		1.1		V
Detector Pout Threshold[4]		5		V
Turn-On Time[3]		<1.0		µS

Notes:
1. VCC = 3.3V, VPC = 2.9V, T_A = 25°C, PA is constantly biased, 50Ω system.
2. Power Control bias current is included in the total quiescent current.
3. Measured from Device On signal turn on, (Logic Low) to the point where RF P_{OUT} stabilizes to 0.5dB.
4. P_{OUT} measured at P_{IN} corresponding to power detection threshold.

Functional Block Diagram

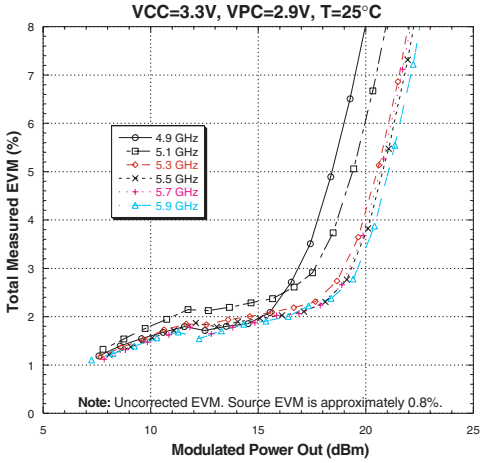


Performance Data

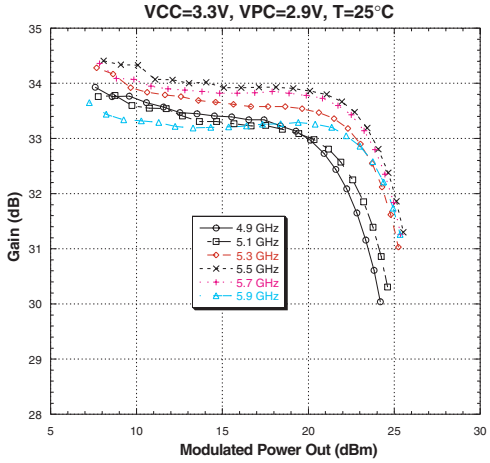
802.11a OFDM Modulation

(176 ms burst time, 100 ms idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

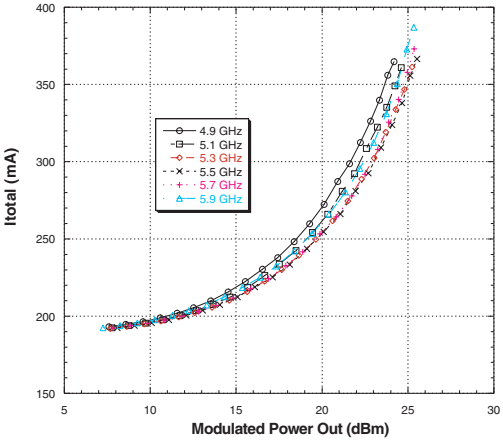
RMPA5255 EVM vs. Modulated Pout
VCC=3.3V, VPC=2.9V, T=25°C



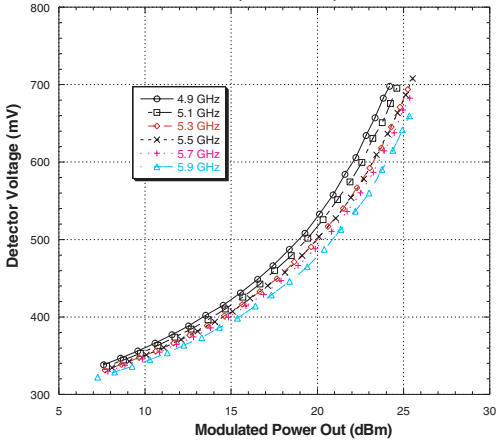
RMPA5255 Gain vs. Modulated Pout
VCC=3.3V, VPC=2.9V, T=25°C



RMPA5255 Total Current vs. Modulated Pout
VCC=3.3V, VPC=2.9V, T=25°C



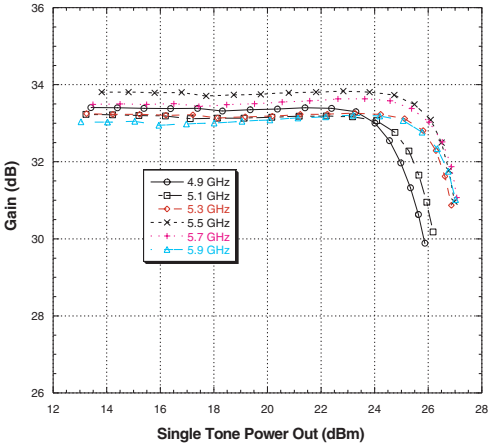
RMPA5255 Detector Voltage vs. Modulated Pout
VCC=3.3V, VPC=2.9V, T=25°C



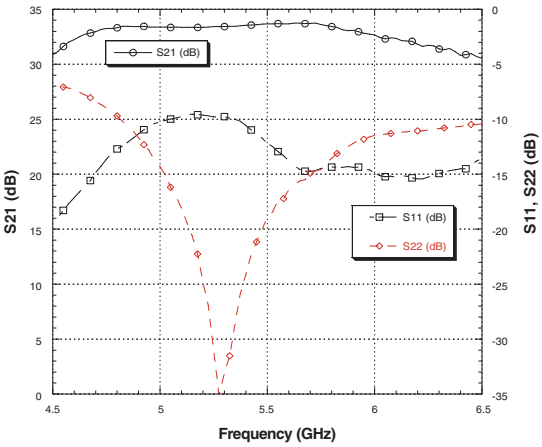
Performance Data

Single Tone

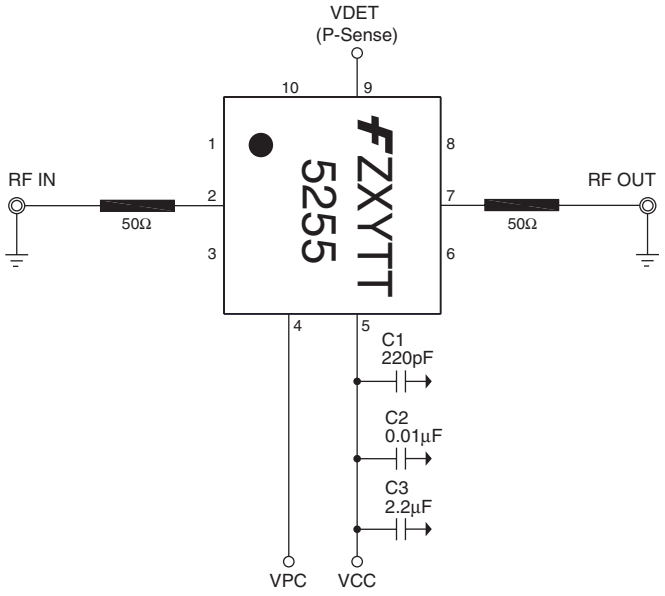
RMPA5255 Gain vs. Single Tone Pout
VCC=3.3V, VPC=2.9V, T=25°C



RMPA5255 S-Parameters vs. Frequency
VCC=3.3V, VPC=2.9V, T=25°C

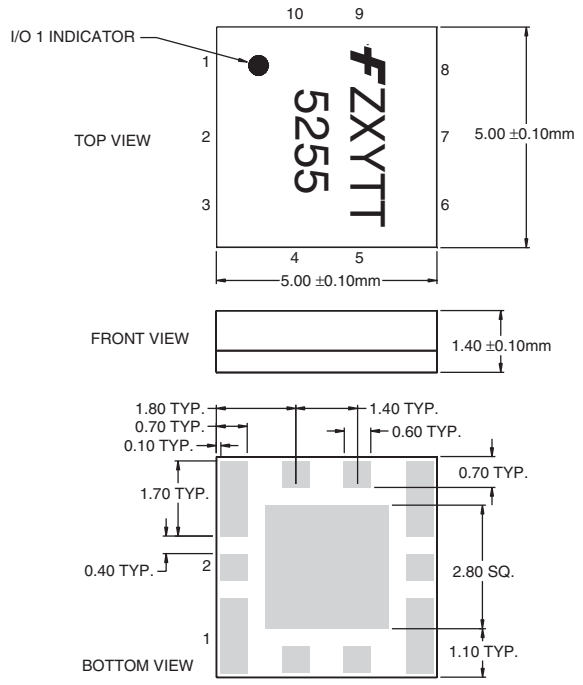


Schematic



Pin	Description
1	GND
2	RF IN
3	GND
4	VPC
5	VCC
6	GND
7	RF OUT
8	GND
9	VDET (P-Sense)
10	N/C
11	CENTER GND

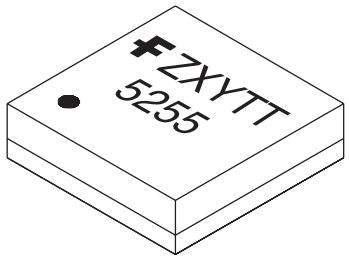
Package Outline



NOTES:

1. PACKAGE BASE MATERIAL AND INTERCONNECT METALLIZATION:
   BT GRADE CCL-HL832, AuNiCu,
   Au 0.38 MICROMETERS MINIMUM.
2. SMT EXPOSURE: THIS DEVICE WILL WITHSTAND EXPOSURE TO TEMPERATURES OF 240°C MAXIMUM FOR DWELL TIME OF 10 SECONDS MAXIMUM.

= EXPOSED METAL CONTACT PADS



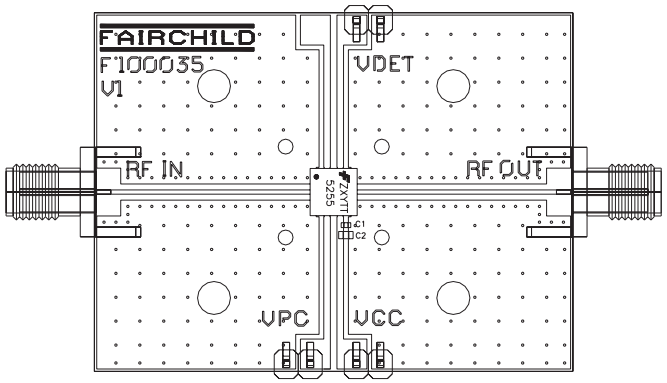
Dimensions in mm

Evaluation Board Bill of Materials

MATERIALS LIST

QTY	ITEM NO.	PART NUMBER	DESCRIPTION	VENDOR
1	1	F100035	PC, BOARD	FAIRCHILD
2	2	#142-0701-841	SMA CONNECTOR	JOHNSON
6	3	#2340-5211TN	TERMINALS	3M
REF	4	F100058	ASSEMBLY, RMPA5255	FAIRCHILD
1	5 (C1)	GRM1885C1H221JA01D	220 pF CAPACITOR (0603)	MURATA
1	6 (C2)	GMC10X7R103M25NT	0.01 uF CAPACITOR (0603)	MURATA
1	7 (C3)	GRM188R60J225KE01D	2.2 uF CAPACITOR (0603)	MURATA
A/R	8	SN63	SOLDER PASTE	INDIUM CORP.
A/R	9	SN96	SOLDER PASTE	INDIUM CORP.

Evaluation Board Layout



Actual Board Size = 2.0" X 1.5"

Evaluation Board Turn-On Sequence[1]

Recommended turn-on sequence:

1) Connect common ground terminal to the Ground (GND) pin on the board.
2) Connect voltmeter to VDET (P-Sense).
3) Apply positive supply voltage (3.3 V) to pin VCC (Collector voltage).
4) Apply positive bias voltage (2.9 V) to pin VPC (Power Control voltage).
5) At this point, you should expect to observe the following positive currents flowing into the pins:

Pin	Current
VCC	150 – 170 mA
VPC	21 – 31 mA

6) Apply input RF power to SMA connector pin RFIN. Current for pin VCC will vary depending on the input drive level.
7) Vary positive voltage VPC from +2.9 V to +0 V to shut down the amplifier or alter the power level. Shut down current flow into the pins:

Pin	Current
VCC	<1 nA

Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

Note:

1. Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design.

Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Assemble the devices within 7 days of removal from the dry pack.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure, at 125°C for 24 hours minimum, must be performed.

Solder Materials & Temperature Profile:
Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

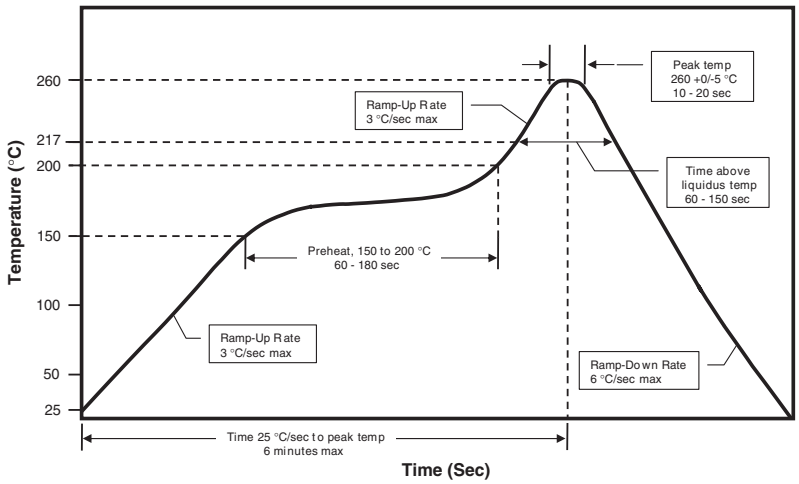
Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A maximum heating rate is 3°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 60-180 seconds at 150-200°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 20 seconds. Soldering temperatures should be in the range 255–260°C, with a maximum limit of 260°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should be subjected to no more than 15°C above the solder melting temperature for no more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile



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