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RF7211

3V W-CDMA BAND 11/21 LINEAR PA MODULE

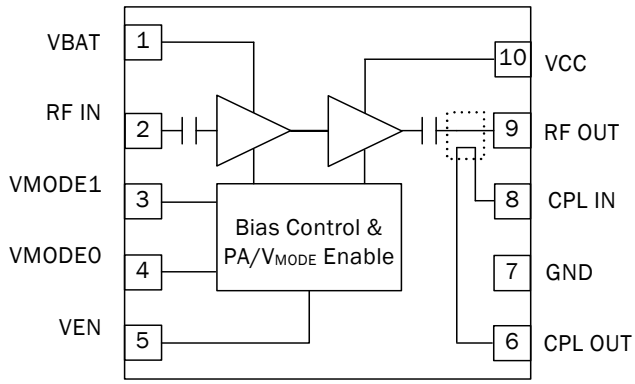
Package Style: Module, 10-Pin, 3mmx3mmx1.0mm

Features

- HSPA+ Compliant
- Low Voltage Positive Bias Supply (3.0V to 4.2V)
- +28dBm Linear W-CDMA Rel 99 Output Power (+26.5dBm HSPA+ and HSDPA)
- High Efficiency Operation
  38% at P_{OUT}=28dBm
  33% at P_{OUT}=+26.5dBm
  16% at P_{OUT}=+18.0dBm
  (Without DC/DC Converter)
- Low Quiescent Current in Low Power Mode: 18mA
- Internal Voltage Regulator Eliminates the Need for External Reference Voltage (V_{REF})
- 3-Mode Power States with Digital Control Interface
- Supports DC/DC Converter Operation
- Integrated Power Coupler
- Integrated Blocking and Collector Decoupling Capacitors

Applications

- WCDMA/HSDPA/HSPA+ Wireless Handsets and Data Cards
- Dual-Mode UMTS Wireless Handsets and Data Cards



Functional Block Diagram

Product Description

The RF7211 is a high-power, high-efficiency, linear power amplifier designed for use as the final RF amplifier in 3V, 50Ω W-CDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for UMTS Band 11 and 21 operating in the transmit frequency band from 1427.9MHz to 1462.9MHz. The RF7211 has two digital control pins to select one of three power modes to optimize performance and current drain at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7211 is fully HSPA+ compliant and is assembled in a 10-pin, 3mmx3mm module.

Ordering Information

RF7211	3V W-CDMA Band 11/21 Linear PA Module
RF7211PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage, V_{BAT}	6.0	V
Control Voltage, VMODE0, VMODE1	3.5	V
Control Voltage, V_{EN}	3.5	V
RF - Input Power	+6	dBm
RF - Output Power	+30	dBm
Output Load VSWR (Ruggedness)	10:1	
Operating Ambient Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C

No damage as long as only one parameter is at limit at one time with the other parameters set at recommended operating conditions.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Operating Frequency Range	1427.9		1462.9	MHz	
V_{BAT}	+3.0	+3.4	+4.2	V	
V_{CC}	+3.0[1]	+3.4	+4.2	V	
V_{EN}	0		0.5	V	PA disabled.
	1.4	1.8	3.0	V	PA enabled.
V_{MODE0}, V_{MODE1}	0		0.5	V	Logic “low”.
	1.5	1.8	3.0	V	Logic “high”.
P_{OUT}					
Maximum Linear Output (HPM)	26.5[2,3]			dBm	High Power Mode (HPM)
Maximum Linear Output (MPM)	18.0[2,3]			dBm	Medium Power Mode (MPM)
Maximum Linear Output (LPM)	7.0[2,3]			dBm	Low Power Mode (LPM)
Ambient Temperature	-30	+25	+85	°C	

Notes:

[1]Minimum V_{CC} for max P_{OUT} is indicated. V_{CC} down to 0.5V may be used for backed-off power when using DC/DC converter to conserve battery current.

[2]For operation at V_{CC}=+3.0V, derate P_{OUT} by 1.3dB. At V_{CC}=3.2V, derate P_{OUT} by 0.6dB.

[3]P_{OUT} is specified for HSDPA and HSPA+ modulation:
HSDPA Configuration: βc=12, βd=15, βhs=24
HSPA+ Configuration: 3GPP Release 7 Subtest 1

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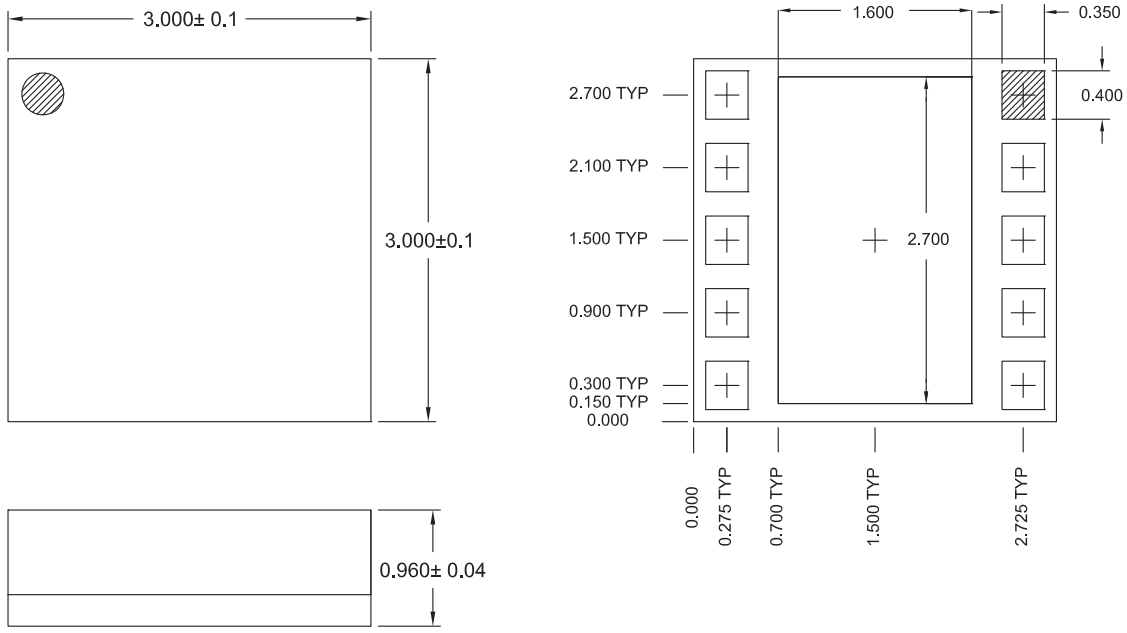
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					T_C=+25°C, V_{CC}=V_{BAT}=+3.4V, V_{EN}=+1.8V, HSPA+ Modulation, and 50Ω system, unless otherwise specified.
Gain	25.0	26.5	30	dB	HPM, P_{OUT}=26.5dBm
	14	16.5	20	dB	MPM, P_{OUT}≤18.0dBm
	10	13.5	15	dB	LPM, P_{OUT}≤7.0dBm
Gain Linearity		±0.4		dB	HPM, 18.0dBm≤P_{OUT}≤26.5dBm
ACLR - 5MHz Offset		-39	-36.5	dBc	HPM, P_{OUT}=26.5dBm
		-39	-36.5	dBc	MPM, P_{OUT}=18.0dBm
		-38	-36.5	dBc	LPM, P_{OUT}=7.0dBm
ACLR - 10MHz Offset		-55	-48	dBc	HPM, P_{OUT}=26.5dBm
		-54	-48	dBc	MPM, P_{OUT}=18.0dBm
		-55	-48	dBc	LPM, P_{OUT}=7.0dBm
PAE Without DC/DC Converter	27.5	33	40	%	HPM, P_{OUT}=26.5dBm
	12	16	25	%	MPM, P_{OUT}=18.0dBm
	2.8	4.1	7	%	LPM, P_{OUT}=7.0dBm
Current Drain	328	400	477	mA	HPM, P_{OUT}=26.5dBm
	93	120	155	mA	MPM, P_{OUT}=18.0dBm
	21	36	53	mA	LPM, P_{OUT}=7.0dBm
Quiescent Current	65	100	140	mA	HPM, DC only
	5	24	35	mA	MPM, DC only
	5	18	28	mA	LPM, DC only
Enable Current		0.3	1.0	mA	Source or sink current. V_{EN}=1.8V.
Mode Current (I_{MODE0}, I_{MODE1})		0.3	1.0	mA	Source or sink current. V_{MODE0}, V_{MODE1}=1.8V.
Leakage Current		5.0	15.0	µA	DC only. V_{CC}=V_{BAT}=4.2V, V_{EN}=V_{MODE0}=V_{MODE1}=0V.
Noise Power in Receive Band		-135		dBm/Hz	All power modes, measured at duplex offset frequency (FTX+48MHz). Rx: 1475.9MHz to 1510.9MHz, P_{OUT}≤26.5dBm
Input Impedance		1.7:1		VSWR	No ext. matching, P_{OUT}≤26.5dBm, all modes.
Harmonic 2FO		-20	-13	dBm	P_{OUT}≤26.5dBm, all power modes.
Harmonic 3FO		-40		dBm	P_{OUT}≤26.5dBm, all power modes.
Spurious Output Level			-70	dBc	All spurious, P_{OUT}≤26.5dBm, all conditions, load VSWR≤6:1, all phase angle.
Insertion Phase Shift		±30		°	Phase shift at 18dBm when switching from HPM to MPM and MPM to LPM.
DC Enable Time			10	µS	DC only. Time from V_{EN}=high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	µS	P_{OUT}≤26.5dBm, all modes. 90% of target, DC settled prior to RF.
Coupling Factor		19.5		dB	P_{OUT}≤26.5dBm, all modes.
Coupling Accuracy - Temp/Voltage		±0.5		dB	P_{OUT}≤26.5dBm, all modes. -30°C≤T_C≤85°C, 3.0V≤V_{CC} & V_{BAT}≤4.2V, referenced to 25°C, 3.4V conditions.
Coupling Accuracy - VSWR		±0.7		dB	P_{OUT}≤26.5dBm, all modes, load VSWR=2:1, ±0.7dB accuracy corresponds to 12dB directivity.

Pin	Function	Description
1	VBAT	Supply voltage for bias circuitry and the first stage amplifier.
2	RF IN	RF input internally matched to 50Ω and DC blocked.
3	VMODE1	Digital control input for power mode selection (see Operating Modes truth table).
4	VMODE0	Digital control input for power mode selection (see Operating Modes truth table).
5	VEN	Digital control input for PA enable and disable (see Operating Modes truth table).
6	CPL OUT	Coupler output.
7	GND	This pin must be grounded.
8	CPL IN	Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler.
9	RF OUT	RF output internally matched to 50Ω and DC blocked.
10	VCC	Supply voltage for the second stage amplifier which can be connected to battery supply or output of DC-DC converter.
Pkg Base	GND	Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

V_{EN}	V_{MODE0}	V_{MODE1}	V_{BAT}	V_{CC}	Conditions/Comments
Low	Low	Low	3.0V to 4.2V	3.0V to 4.2V	Power down mode
Low	X	X	3.0V to 4.2V	3.0V to 4.2V	Standby Mode
High	Low	Low	3.0V to 4.2V	3.0V to 4.2V	High Power Mode (HPM)
High	High	Low	3.0V to 4.2V	3.0V to 4.2V	Medium Power Mode (MPM)
High	High	High	3.0V to 4.2V	3.0V to 4.2V	Low Power Mode (LPM)
High	Low	Low	3.0V to 4.2V	≥0.5V	Optional lower V_{CC} in Low Power Mode (LPM)

Package Drawing



NOTES:
1. SHADED AREAS REPRESENT PIN 1 LOCATION.

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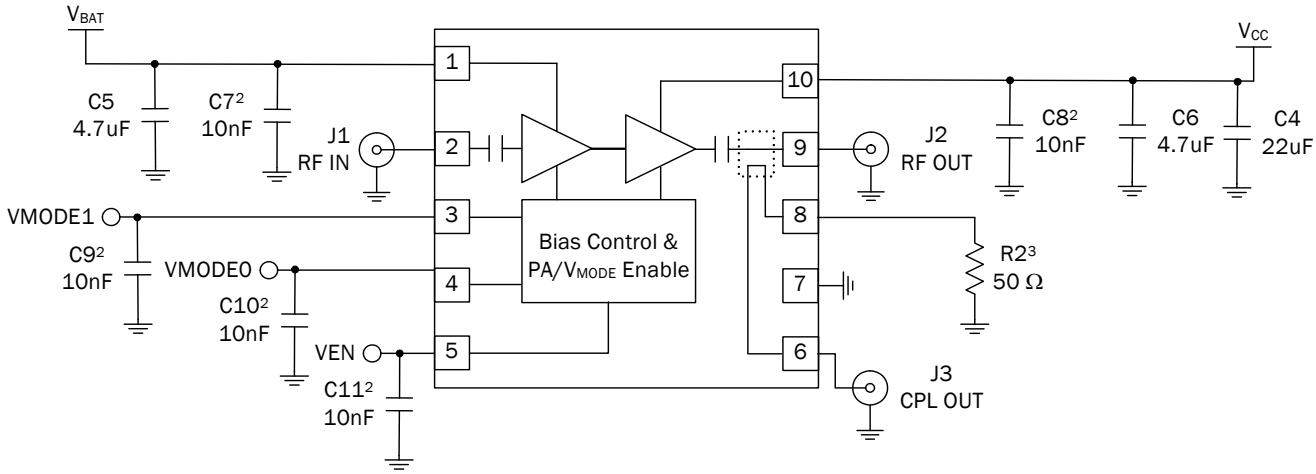
Preliminary Application Schematic



NOTES:

1 VCC and VBAT are connected together if DC-DC converter is not used.

2 Place these capacitors as close to PA as possible.

3 50 Ω resistor will be removed if pin 8 is connected to another coupler.

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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

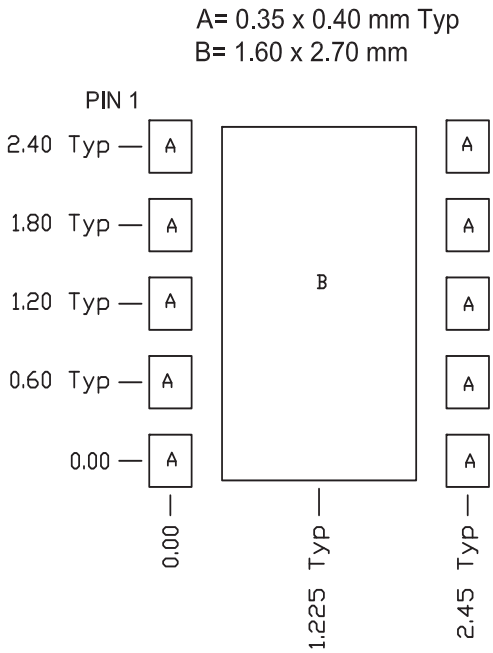

Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

A= 0.45 x 0.50 mm Typ
B= 1.70 x 2.80 mm

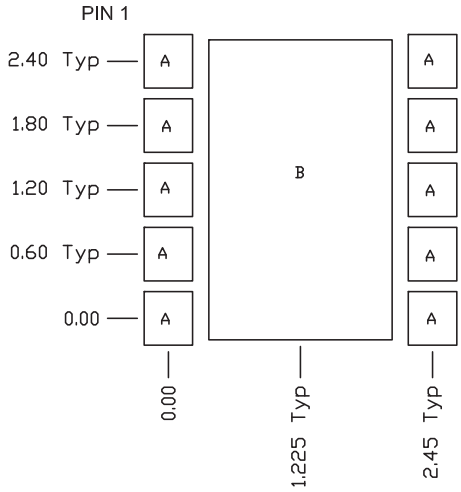

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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