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TPIC82000 Series
Tire Pressure Monitoring System TX Module

Data Manual

TEXAS INSTRUMENTS

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Literature Number: SLDS189
May 2012

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Tire Pressure Monitoring System TX Module

Check for Samples: TPIC82000 Series

1 INTRODUCTION

1.1 Features

- **Operating Voltage Range: 1.5 V to 3.5 V (315 MHz), 1.75 V to 3.5 V (434 MHz)**
- **Operating Temperature Range : –40°C to 125°C**
- **Low Current Consumption to Support a Coin Size Lithium Battery Operation**
- **In Package Pressure Sensor (Operation Range: 50 kPa to 635 kPa)**
- **In Package Accelerometer**
- **On Chip Temperature Sensor**
- **On Chip Battery Voltage Sensor**
- **13-bit ADC for Sensors**
- **Dual Band 315/434 MHz Transmitter With One Crystal Oscillator**
- **Fully Integrated PLL Synthesizer**
- **ASK/FSK Baseband Modulator for 10K bits/s Manchester/BiPhase Coding, Capable up to 20K bits/s for FSK**
- **Dual Band Quadrature Modulator for Transmit Frequency Tuning (~ ±700 kHz)**
- **125 kHz LF ASK Receiver (4K bits/s Manchester/BiPhase Code)**
- **LF Antenna Q Tuning Function**
- **Selectable LF Format**
- **8051 Compatible Microcontroller**
- **16KB ROM (for Program Code)**
- **43 Words (7-bit x 43 Word) EEPROM**
- **128-byte Battery Backed up RAM (BuRAM) (Uninitialized RAM at MCU Sleep Mode)**
- **8-bit CRC Generator for BuRAM**
- **16 PIN Ceramic Package with Diaphragm for Pressure Sensor (Shielded for EMI Protection)**

1.2 General Description

The TPIC82000 series integrates the functions required for a transmit (TX) module in Tire Pressure Monitoring System (TPMS) into a single ceramic package. The functions required for TPMS applications such as measurement functions (tire pressure, tire temperature, tire acceleration, battery voltage), RF data transmission, and LF command receiving functions are integrated in one device. The device consists of a ceramic package with diaphragm for pressure sensing, an accelerometer, and an LSI. The LSI integrates an 8051 microcontroller, RF transmitter, LF receiver, and Analog Front-End (AFE) with a 13-bit ADC for sensor measurements.

To minimize the power consumption and maximize the battery life of the system, the device can wake up periodically for measurements and RF transmissions using an internal ultra low power programmable timer or the 125 kHz LF trigger signal detector. Also, to support maximum usage of battery energy, the device can operate over the wide power supply range from 3.5 V to 1.5 V. (For 434 MHz RF transmission, the minimum voltage is 1.75 V)

The LF receiver enables control of this device remotely using a 125 kHz LF signal.

The 315 and/or 434 MHz local carrier signal is generated by the internal PLL synthesizer with one external crystal resonator.

The RF transmit frequency tuning is achieved using a baseband signal generator and a quadrature modulator. The baseband signal generator can control the baseband frequency up to 700 kHz.

The device supports automotive temperature range (–40°C to 125°C) and quality.

In the TPIC82000 series, the accelerometer is an optional component, and for the pressure sensor there are two selections: A and B at TI-TEST factory. For the RF transmission characteristic of 315 and 434 MHz band, one of the RF bands is tested at TI-TEST factory. The device names are defined below.

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Device Name		Accelerometer Type / Pressure Sensor Selection A and B	
TPIC820X00	X	0: No Accelerometer	1: 1-Axis (Z) Accelerometer
TPIC8200Y0	Y	0: Passenger car (Selection A)	2: Passenger Car (Selection B)
TPIC82000Z	Z	3: 315 MHz	4: 434 MHz

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2 PIN CONFIGURATION AND DESCRIPTIONS

2.1 Pin Configuration

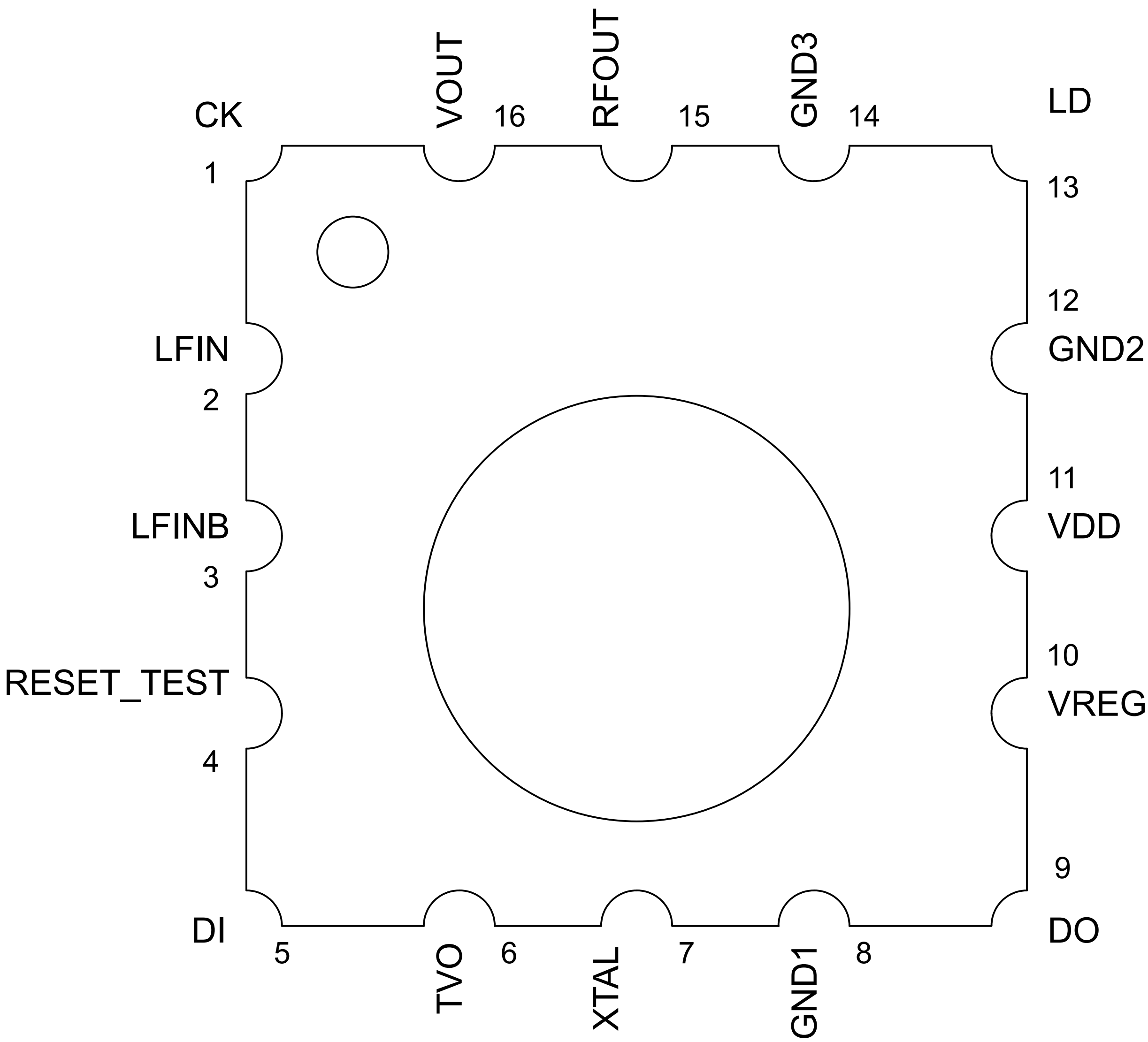

Figure 2-1. Top View from Diaphragm

2.2 Pin Descriptions

PIN			PULL UP-DOWN	DESCRIPTION
NAME	NO.	TYPE		
CK	1	I	Pull down	SPI CK input terminal
LFIN	2	I		LF receiver input terminal 1
LFINB	3	I		LF receiver input terminal 2
RESET_ TEST	4	I	Pull down	H/W reset and Test Mode input terminal
DI	5	I	Pull up	SPI DATA input terminal at EN_UART = 0 UART RXD output terminal at EN_UART = 1
TVO	6	O		TVO output terminal
XTAL	7	I		XTAL component connection terminal
GND1	8	GND		GND (Common GND)

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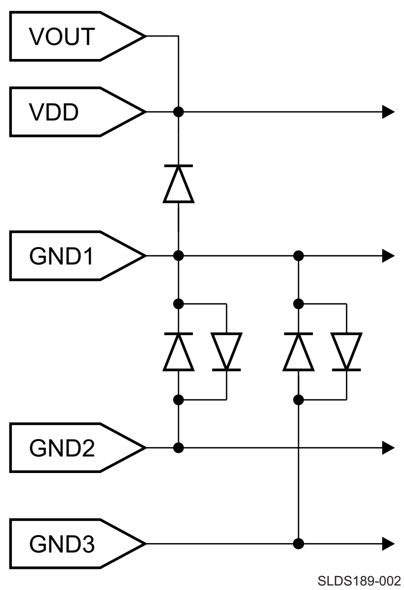
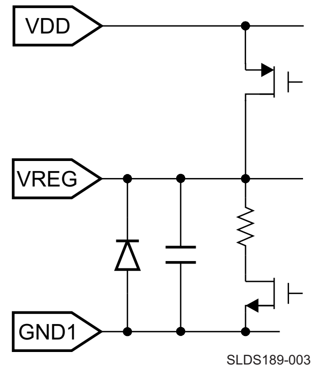
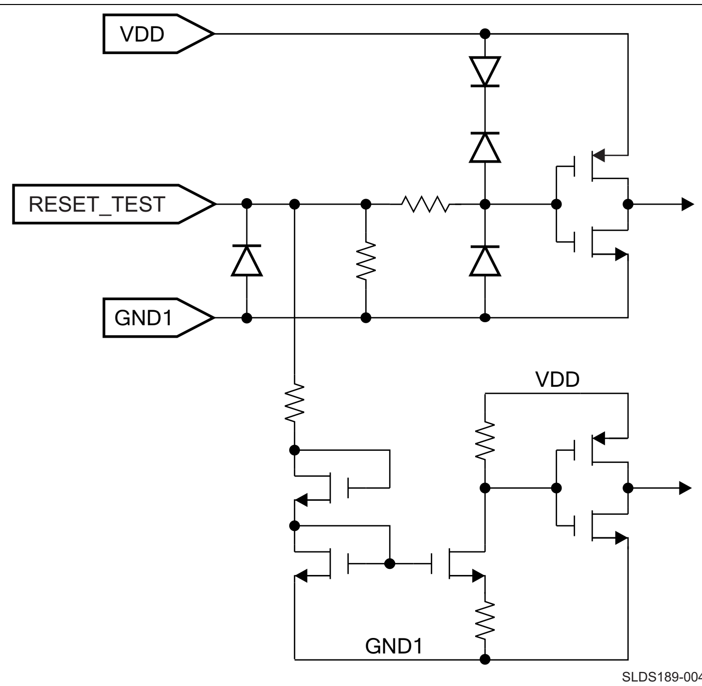
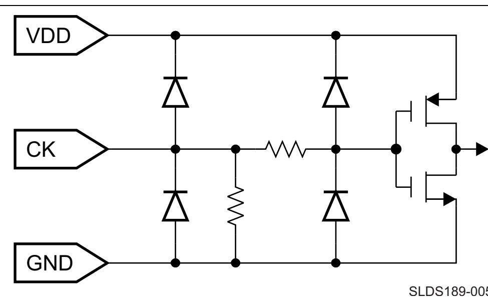
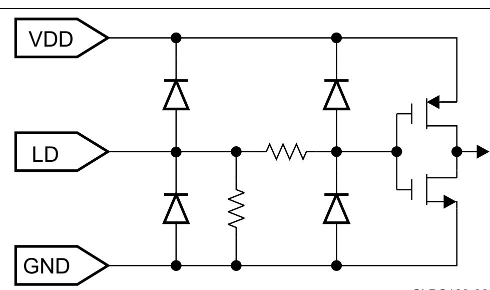
PIN			PULL UP-DOWN	DESCRIPTION
NAME	NO.	TYPE		
DO	9	O		SPI DO output terminal at EN_UART = 0 UART TXD output terminal at EN_UART = 1
VREG	10	O		Internal voltage regulator output A decoupling capacitor (0.1 µF) needs to be connected between this terminal and GND. VREG should not be used to supply external loads.
VDD	11	Supply		Battery supply voltage
GND2	12	GND		GND (RF block except PA)
LD	13	I	Pull down	SPI CS input terminal
GND3	14	GND		GND (RF PA)
RFOUT	15	O		RF PA output terminal
VOUT	16	O		V_{DD} for load of PA (connected to V_{DD} internally)

2.3 Pin Equivalent Circuits

PIN			PULL UP-DOWN	EQUIVALENT CIRCUITS
NAME	NO.	TYPE		
VDD	11	Supply		
GND1	8			
GND2	12			
GND3	14			
VOUT	16			

PIN			PULL UP-DOWN	EQUIVALENT CIRCUITS
NAME	NO.	TYPE		
VREG	10	O		
RESET_ TEST	4	I	Pull down	
CK	1	I	Pull down	
LD	13	I	Pull down	

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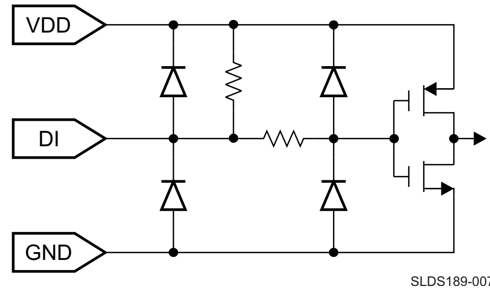
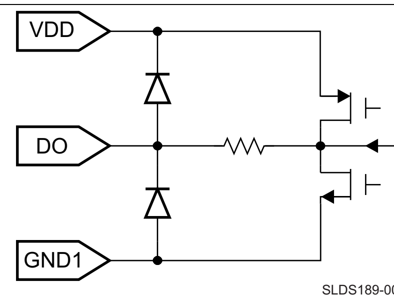
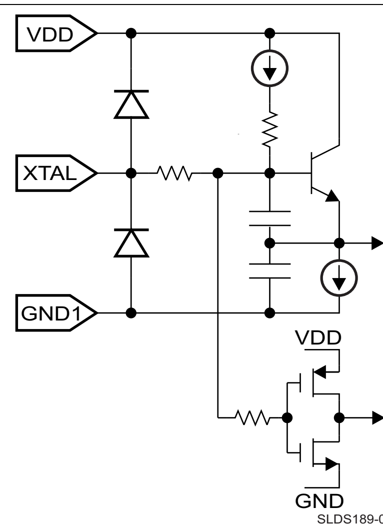
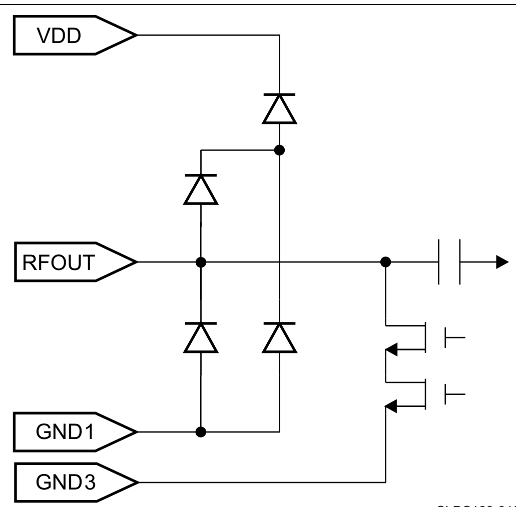
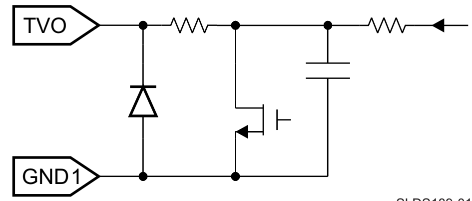
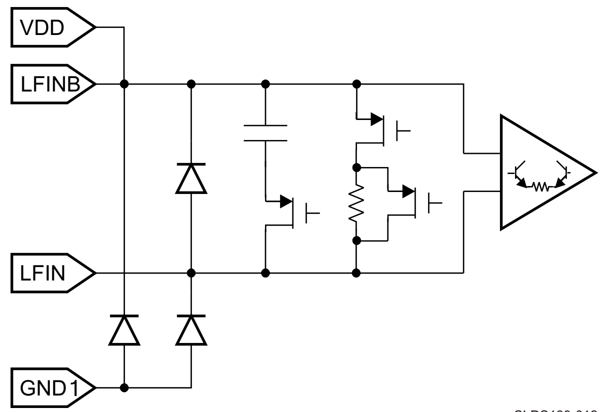
PIN			PULL UP-DOWN	EQUIVALENT CIRCUITS
NAME	NO.	TYPE		
DI	5	I	Pull up	
DO	9	O		
XTAL	7	I		
RFOUT	15	O		

PIN			PULL UP-DOWN	EQUIVALENT CIRCUITS
NAME	**NO.**	**TYPE**		
TVO	6	O		 SLDS189-011
LFINB	3	I		 SLDS189-012
LFIN	2			

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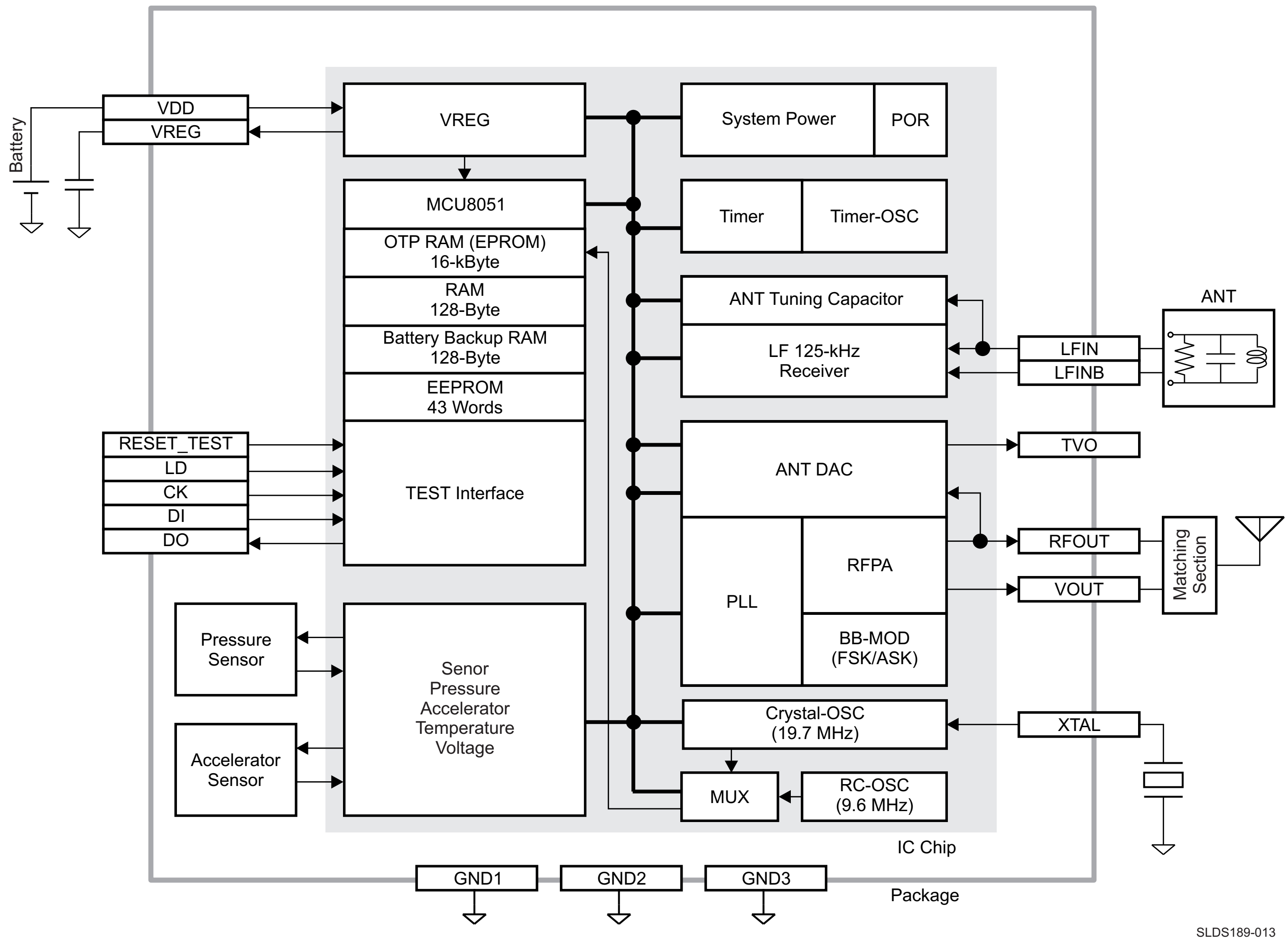
3 FUNCTION DESCRIPTION

3.1 Functional Block Diagram (Whole Device)

The block diagram below shows the overview of the whole TPIC82000 device.

The TPIC82000 consists of a pressure sensor which is structured within the ceramic package, an accelerometer for motion sensing, and a mixed signal LSI. The LSI integrates the 8051 microcontroller, a voltage regulator for internal block operation, an Analog Front-End for the sensor signal conditioning, clock generators for processor and internal blocks, an RF transmitter, and an LF signal receiver. The details of each block are described in the following sections.

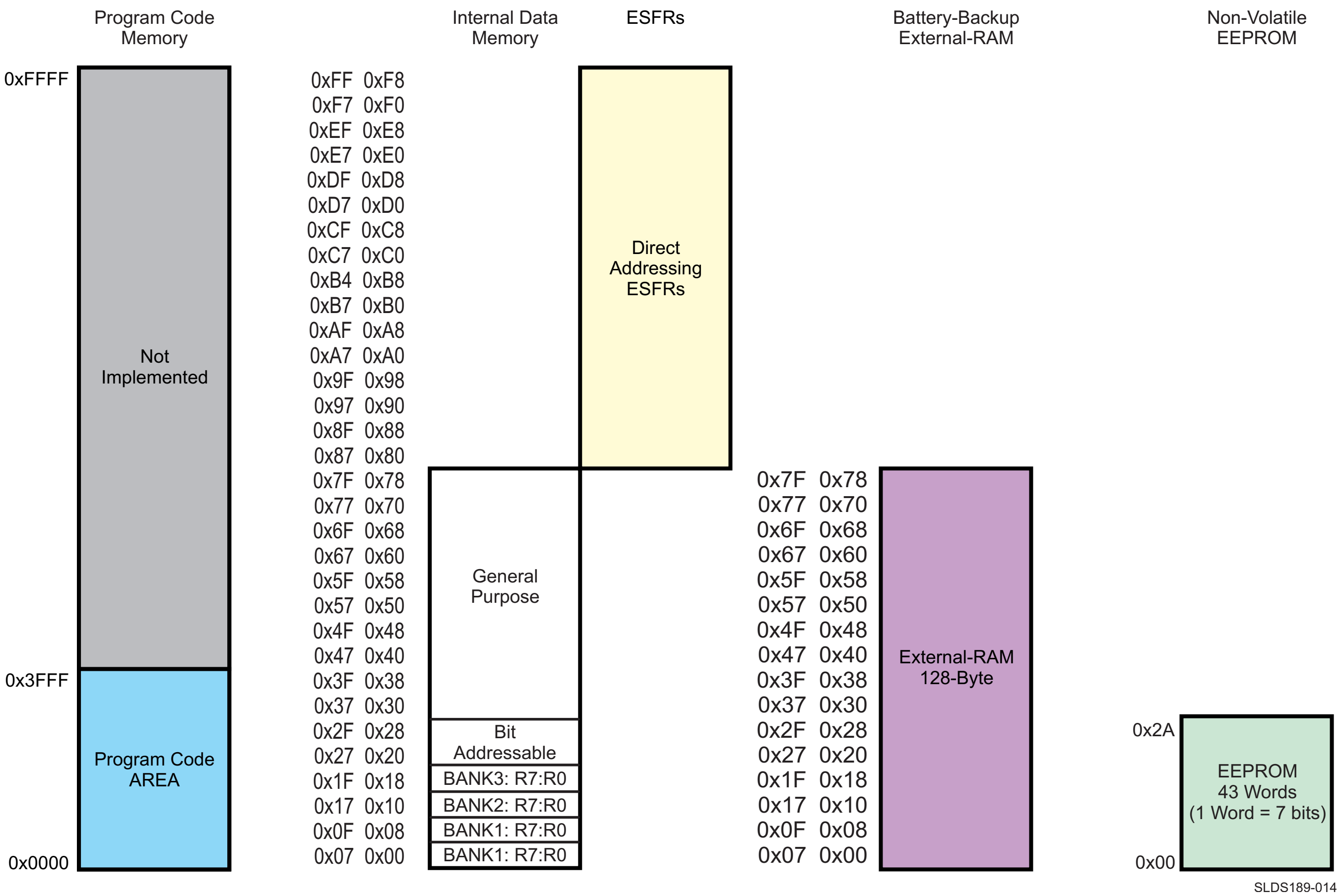


3.2 MCU8051 core

The TPIC82000 integrates a high performance version 8-bit microcontroller that is software compatible with the industry standard 8051. The MCU8051 core uses an internal RC oscillator (about 9.6 MHz) or an external crystal (about 19.7 MHz) as the clock source. It uses a two-clock period machine cycle to realize faster operation.

The MCU can address up to 16K bytes of program memory (ROM) and up to 128 bytes of internal data memory (RAM). The MCU can also access the integrated External Special Function Registers (ESFR) space up to 128 bytes. The control registers for built-in peripheral analog/logic circuit control, non-volatile EEPROM memory control and the Battery Backup External-RAM memory control are allocated in this ESFR space. The 43-word EEPROM (7bit x 43word) is prepared as a non-volatile data storage for the various variable parameters such as device ID and calibration parameters. The Battery Backup External-RAM is a volatile memory but the contents of the memory can be kept by the internal regulator when the device is in sleep mode.

3.2.1 Memory Resource Map



3.2.2 Program Code Memory (ROM)

The 16K byte program code memory is located in the address space from 0x0000 to 0x3FFF. This portion is configured by Mask ROM, which is locked by a hardware disabling the SPI DO output as default to protect the ROM code.

NOTE

If using the built-in firmware prepared by TI, the program code area for the application software becomes smaller than 16K bytes (Typically around half of 16K bytes are available for application software).

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3.2.3 Internal Data Memory (RAM)

The 128-bytes of RAM are available as the volatile data storage for standard 8051 application program. During MCU sleep mode, the RAM is powered off and their contents are lost. Right after the Power-On-Reset or the Power-up of the MCU, the RAM data is not initialized.

3.2.4 External Special Function Registers (ESFR)

The ESFRs are mapped on physical memory spaces 0x80 to 0xFF on the MCU8051 core to control and monitor the built-in peripherals. Figure 3-1, Figure 3-2, and Figure 3-3 show the register allocations.

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3.2.4.1 ESFR Table

ESFR Address	Write Register			Read Register		
	Name	Reset (Note 1)		Name	Reset (Note 1)	
		Power on	Timer		Power on	Timer
FF	-			-		
FE	-			-		
FD	-			-		
FC	-			-		
FB	-					
FA	-					
F9	EEpromCONT	X011 1111	X011 1111			
F8	IP1 (Not Usable)	0000 0000	0000 0000	IP1 (Not Usable)	0000 0000	0000 0000
F7	-			-		
F6	-			-		
F5	-			-		
F4	-			-		
F3	AntDac	0000 0000	0UUU UUUU			
F2	RFbias	0000 0000	0000 0000			
F1	RFpower	0000 0000	0000 0000			
F0	B	0000 0000	0000 0000	B	0000 0000	0000 0000
EF	-			-		
EE	-			-		
ED	SLoffset	XXXU UUUU	XXXS SSSS	-		
EC	LFcont	UUUU UUUU	SSSS SSSS	LFdataCount	0000 0000	DDDD DDDD
EB				ModState	U1XX XXXX	U1XX XXXX
EA				SystemState	0X11 1110	1XDD 1DD0
E9				Timer state	00XX 1110	00XX DDDD
E8	IE1 (Not Usable)	0000 0000	0000 0000	IE1 (Not Usable)	0000 0000	0000 0000
E7	-			-		
E6	-			-		
E5	-			-		
E4	-			-		
E3				LocalState	XXX0 00U0	XXX0 00D0
E2				LFrxData	0000 0000	DDDD DDDD
E1				LFanalogFE	UUUU UUUU	DDDD DDDD
E0	ACC	0000 0000	0000 0000	ACC	0000 0000	0000 0000
DF	BuRAM_CRC_Start_Adr	X000 0000	X000 0000	BuRAM_CRC_Start_Adr	X000 0000	X000 0000
DE	BuRAM_CRC_End_Adr	0000 0000	0000 0000	BuRAM_CRC_End_Adr	0000 0000	0000 0000
DD	LFCarrierDet	XXX0 0000	XXXD DDDD	BuRAM_CRC_Status	0XXX XXXX	0XXX XXX
DC	Lfabort	0000 0000	DDDD DDDD	BuRAM_CRC_Result	1111 1111	1111 1111
DB				-		
DA				-		
D9				-		
D8						

Note 1	Power on	Initial value from Power-On-Reset
Note 2	Timer	Initial value from WAKEUP-EVENT (Timer / LF trigger / RF trigger)
	0	DATA 0
	1	DATA 1
	D	DATA 0 or DATA 1, depend on the EVENT/State
	U	Unknown, or DATA loss in MCU sleep state
	X	Not implemented
	S	DATA kept during SLEEP state
	(white)	Accessible ESFR on TPIC82000
	- (blue)	Reserved (Not Used)
	(light cyan)	Reserved (by MCU Core)
	(yellow)	Reserved (for FW & Internal use)

Figure 3-1. ESFR Table (Address FF–D8)

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3.2.4.2 ESFR Table (Continued)

ESFR Address	Write Register			Read Register		
	Name	Reset (Note 1)		Name	Reset(Note 1)	
		Power on	Timer		Power on	Timer
D7	RC-OSC (Note 2)	0000 1110	000S SSSS	RC-OSC	0000 1110	000S SSSS
D6	-			-		
D5	-			-		
D4	-			-		
D3	ModCONT	0X00 0000	0X00 0000	-		
D2	ModScale	UUUU UUUU	UUUU UUUU	-		
D1	ModOffset	UUUU UUUU	UUUU UUUU	-		
D0	PSW	0000 0000	0000 0000	PSW	0000 0000	0000 0000
CF	-			-		
CE				-		
CD	LFwake1H	UUUU UUUU	SSSS SSSS	-		
CC	LFwake1L	UUUU UUUU	SSSS SSSS	-		
CB	ModTxData	UUUU UUUU	UUUU UUUU	-		
CA	ModRamAdd	XXUU UUUU	XXUU UUUU	-		
C9	ModRamData	UUUU UUUU	UUUU UUUU	-		
C8				LFstate	0000 0000	DDDD DDDD
C7	LFmodeRSSI	0UUU UUXX	0SSS SSXX	-		
C6	LFagcSET	XXUU UUUU	XXSS SSSS	LFagcSET	XX00 0000	XXDD DDDD
C5	LFdataC	UUUU UUUU	SSSS SSSS	-		
C4	TimerLFwake	1111 1111	SSSS SSSS	-		
C3				TESTvector	DD00 0000	DD00 0000
C2	PLLlocalOSC	1000 0000	1000 0000	-		
C1	BuRAM_DATA	UUUU UUUU	SSSS SSSS	BuRAM_DATA	UUUU UUUU	SSSS SSSS
C0				SensorState	00UX XXXX	00UX XXXX
BF	SensorDC6	0000 0000	0000 0000	-		
BE	SensorDC5	X000 0000	X000 0000	-		
BD	SensorDC4	X000 0000	X000 0000	-		
BC	SensorDC3	X000 0000	X000 0000	-		
BB	SensorDC2	X000 0000	X000 0000	-		
BA	SensorDC1	X000 0000	X000 0000	-		
B9	SensorDC0	X000 0000	X000 0000	-		
B8	IP	1111 1111	1111 1111	IP	1111 1111	1111 1111
B7	SensorBaseH	XXX0 0000	XXX0 0000	-		
B6	SensorBaseL	0000 0000	0000 0000	-		
B5	SensorOffsetH	XX00 0000	XX00 0000	-		
B4	SensorOffsetL	0000 0000	0000 0000	-		
B3	SensorCONT	0000 0000	0000 0000	-		
B2	LFANT	UUUU UUUU	SSSS SSSS	-		
B1	LFwake0H	UUUU UUUU	SSSS SSSS	-		
B0	P3	1111 1111	1111 1111	P3	1111 1111	1111 1111
AF	LFwake0L	UUUU UUUU	SSSS SSSS	-		
AE	LFsync1	XUUU UUUU	XSSS SSSS	-		
AD	LFsync0	UUUU UUUU	SSSS SSSS	-		
AC	LFpLT	UUUU UUUU	SSSS SSSS	-		

Note 1	Power on	Initial value from Power-On-Reset
Note 2	Timer	Initial value from WAKEUP-EVENT (Timer / LF trigger / RF trigger)
	0	DATA 0
	1	DATA 1
	D	DATA 0 or DATA 1, depend on the EVENT/State
	U	Unknown, or DATA loss in MCU sleep state
	X	Not implemented
	S	DATA kept during SLEEP state
	(white)	Accessible ESFR on TPIC82000
	- (blue)	Reserved (Not Used)
	(light cyan)	Reserved (by MCU Core)
	(yellow)	Reserved (for FW & Internal use)

Figure 3-2. ESFR Table (Address D7–AC)

3.2.4.3 ESFR Table (Continued)

ESFR Address	Write Register			Read Register		
	Name	Reset(Note 1)		Name	Reset(Note 1)	
		Power on	Timer		Power on	Timer
AB	LFpUT	UUUU UUUU	SSSS SSSS	-		
AA	LFrssiVT	UUUU UUUU	SSSS SSSS	-		
A9	-			-		
A8	IE	0000 0000	0000 0000	IE	0000 0000	0000 0000
A7	LFOSC	UUUU UUUU	SSSS SSSS	-		
A6	LFdelay	UUUU UUUU	SSSS SSSS	-		
A5	LFbias	UUUU UUUU	SSSS SSSS	-		
A4	LFmode	0UUU UUUU	0SSS SSSS	-		
A3	EEpromData	X000 0000	X000 0000	EEpromData	0UUU UUUU (E2prom)	0SSS SSSS (E2prom)
A2	RFdetCONT	000X XXXU	UUUX XXXU	-		
A1	BuRAM_ADDR	0000 0000	0000 0000	BuRAM_ADDR	0000 0000	0000 0000
A0	P2 (Not Usable)	1111 1111	1111 1111	P2 (Not Usable)	1111 1111	1111 1111
9F	-			-		
9E	-			-		
9D	-			-		
9C	-			-		
9B	-			-		
9A	-			-		
99	SBUF	0000 0000	0000 0000	SBUF	0000 0000	0000 0000
98	SCON	0000 0000	0000 0000	SCON	0000 0000	0000 0000
97	TimerOSC	0000 0000	0SSS SSSS	-		
96	TimerPre	1111 1111	SSSS SSSS	-		
95	TimerPost	1111 1111	SSSS SSSS	TimerPost	1111 1111	DDDD DDDD
94	SystemPower	100X XXXX	100X XXXX	-		
93	BPL	0000 0000	0000 0000	-		
92	BPU	XX00 0000	XX00 0000	-		
91	TESTvector	0000 0000	0000 0000	-		
90	P1 (Not Usable)	1111 1111	1111 1111	P1 (Not Usable)	1111 1111	1111 1111
8F	-			-		
8E	-			-		
8D	TH1	0000 0000	0000 0000	TH1	0000 0000	0000 0000
8C	TH0	0000 0000	0000 0000	TH0	0000 0000	0000 0000
8B	TL1	0000 0000	0000 0000	TL1	0000 0000	0000 0000
8A	TL0	0000 0000	0000 0000	TL0	0000 0000	0000 0000
89	TMOD	0000 0000	0000 0000	TMOD	0000 0000	0000 0000
88	TCON	0000 0000	0000 0000	TCON	0000 0000	0000 0000
87	PCON	0000 0000	0000 0000	PCON	0000 0000	0000 0000
86	XtalBias	XXXX 0000	XXXX 0000	-		
85	TESTmux1	0000 0000	0000 0000	-		
84	TESTmux0	0000 0000	0000 0000	-		
83	DPH	0000 0000	0000 0000	DPH	0000 0000	0000 0000
82	DPL	0000 0000	0000 0000	DPL	0000 0000	0000 0000
81	SP	0000 0000	0000 0000	SP	0000 0000	0000 0000
80	P0 (Not Usable)	1111 1111	1111 1111	P0 (Not Usable)	1111 1111	1111 1111

Note 1	Power on	Initial value from Power-On-Reset
Note 2	Timer	Initial value from WAKEUP-EVENT (Timer / LF trigger / RF trigger)
	0	DATA 0
	1	DATA 1
	D	DATA 0 or DATA 1, depend on the EVENT/State
	U	Unknown, or DATA loss in MCU sleep state
	X	Not implemented
	S	DATA kept during SLEEP state
	(white)	Accessible ESFR on TPIC82000
	- (blue)	Reserved (Not Used)
	(light cyan)	Reserved (by MCU Core)
	(yellow)	Reserved (for FW & Internal use)

Figure 3-3. ESFR Table (Address AB–80)

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3.2.5 *Battery Backup External-RAM (BuRAM)*

On the TPIC82000 device, the 128-byte RAM area is prepared as the Battery Backup External-RAM on the device and can be used to store status parameters for TPMS applications while the device is in sleep mode. The BuRAM area is structured as the volatile memory but is backed up by internal regulator voltage while in sleep mode. Right after Power-on-Reset, the data contents of RAM are not initialized.

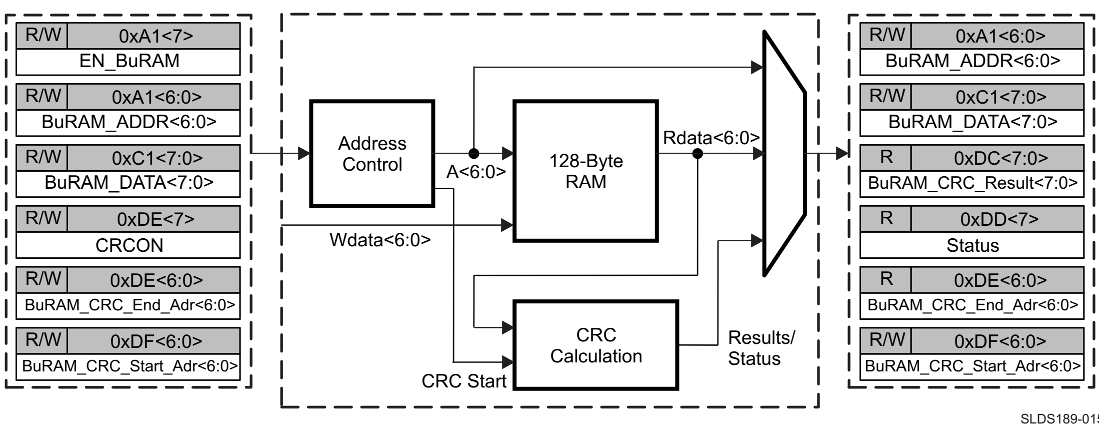
3.2.5.1 CRC (Cyclic Redundancy Check) Generator Function

BuRAM has an 8-bit CRC generator of BuRAM memory, which is shown in Section 3.2.5.2.

The CRC calculation is done through the following steps:

1. Set the CRC calculation start address (**SAR**) of BuRAM memory.
2. Set the CRC calculation end address (**EAR**) of BuRAM memory with CRCON = 1.
   - When CRCON is set to 1, CRC calculation starts from **SAR** to **EAR** data of the BuRAM memory.
   - Each CRC calculation is done by every system clock cycle.
   - CRC initial value is 0xFF.
   - If **SAR** and **EAR** are the same, the CRC calculation result is one address calculation.
   - If **SAR** > **EAR**, calculation starts from **SAR** to 127 and continuously calculates 0 to **EAR**.
3. When CRC calculation is done, the status bit (**BuRAM_CRC_Status** [7]) turns to 1. This flag is cleared by setting CRCON bit to 0.
4. The CRC calculation result appears in the **BuRAM_CRC_Result** register.

3.2.5.2 BuRAM with CRC Generator Block Diagram



3.2.5.3 8-bit CRC Polynomial Expression

The CRC generator uses the following 8-bit polynomial expression shown in Figure 3-4

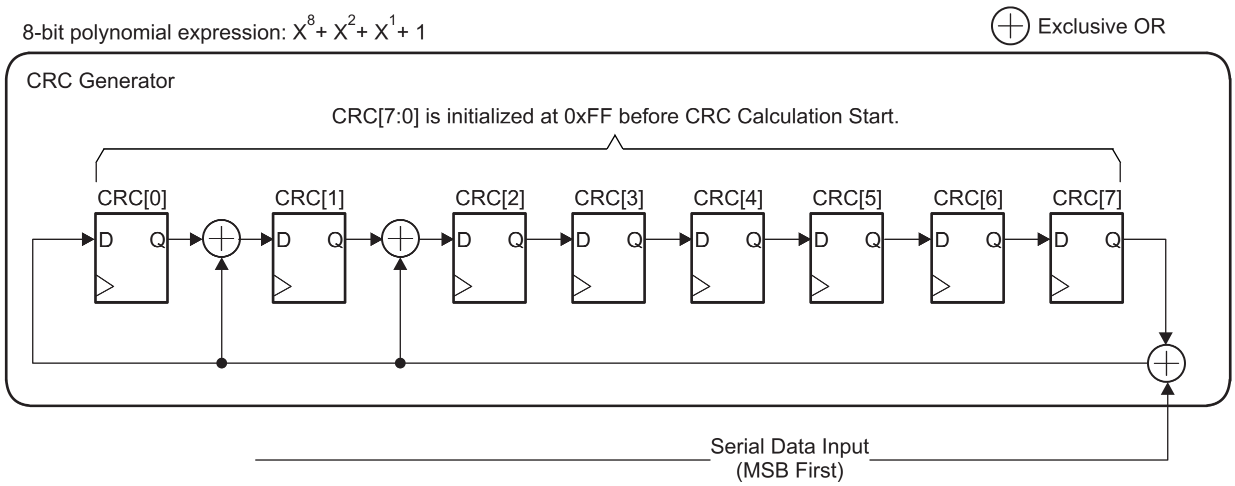
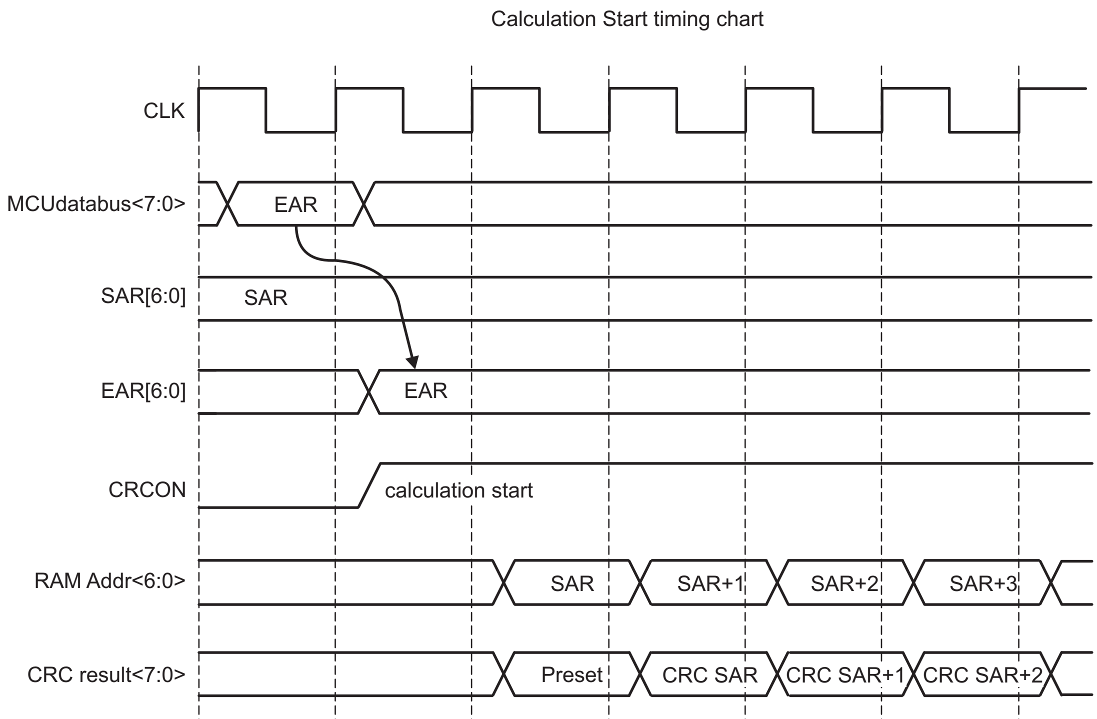


Figure 3-4. CRC Generator 8-bit Polynomial Expression

3.2.5.4 Timing Chart of CRC Calculation from Start Address



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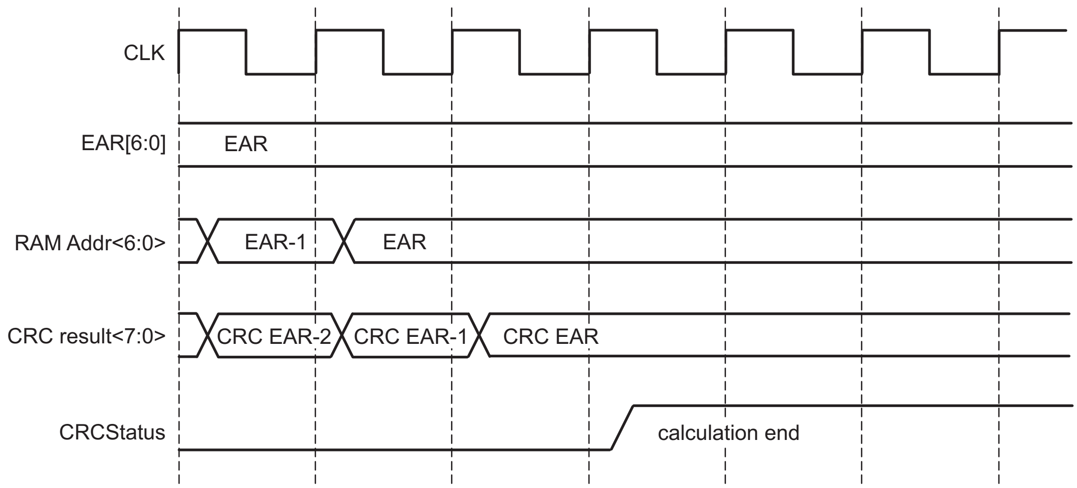
3.2.5.5 Timing Chart of CRC Calculation at the End Address

Calculation End timing chart



3.2.5.6 Battery Backup External-RAM (BuRAM) Control ESFR

- Battery backup RAM Read/Write Address Control — Not Bit Addressable

ESFR: 0xA1 — BuRAM_ADDR

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	EN_BuRAM	BuRAM_ADDR<6:0>						
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

EN_BuRam — BuRAM Read/Write access control bit
1 = Access Enable
0 = Access Disable

BuRAM_ADDR<6:0> — BuRAM Read/Write Address

- Battery backup RAM Read/Write DATA Register — Not Bit Addressable

ESFR: 0xC1 — BuRAM_DATA

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BuRAM_DATA<7:0>							
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

BuRAM_DATA<7:0> — BuRAM Read/Write DATA

- Battery backup RAM CRC Start Address Register — Not Bit Addressable

ESFR: 0xDF — BuRAM_CRC_Start_Adr

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	BuRAM CRC Start Adr<6:0>						
Access	–	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

BuRAM_CRC_Start_Adr<6:0> — CRC calculation start address

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- Battery backup RAM CRC End Address Register Not Bit Addressable

ESFR: 0xDE BuRAM_CRC_End_Adr

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CRCON	BuRAM CRC End Adr<6:0>						
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

CRCON CRC calculation: (1), Normal mode: (0)
BuRAM_CRC_End_Adr<6:0> CRC calculation end address

- Battery backup RAM CRC Status Register Not Bit Addressable

ESFR: 0xDD BuRAM_CRC_Status

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Status	—						
Access	r	–	–	–	–	–	–	–
At Power on reset	0	x	x	x	x	x	x	x
At Timer reset	0	x	x	x	x	x	x	x

Status CRC calculation: Done: (1), BUSY: (0)
Cleared to 0 when CRCON = 0

- Battery backup RAM CRC Result Register Not Bit Addressable

ESFR: 0xDC BuRAM_CRC_Result

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BuRAM CRC Result<7:0>							
Access	r	r	r	r	r	r	r	r
At Power on reset	1	1	1	1	1	1	1	1
At Timer reset	1	1	1	1	1	1	1	1

BuRAM_CRC_Result<7:0> CRC calculation Result

3.2.6 Non-volatile EEPROM

In the TPIC82000 device, the 7-bits x 43-words of EEPROM are available as non-volatile data storage for the various variable parameters. All 7-bits can be used for data storage or the register can be configured for 3-bits Error Correction Code (ECC) + 4-bits of Data.

NOTE

This EEPROM area is also used for the trimming/calibration parameter storage by TI and firmware. Therefore, the actual accessible area for the user is limited for address 0x02 to 0x0F. The interface board and Support Software are prepared to support the EEPROM programming.

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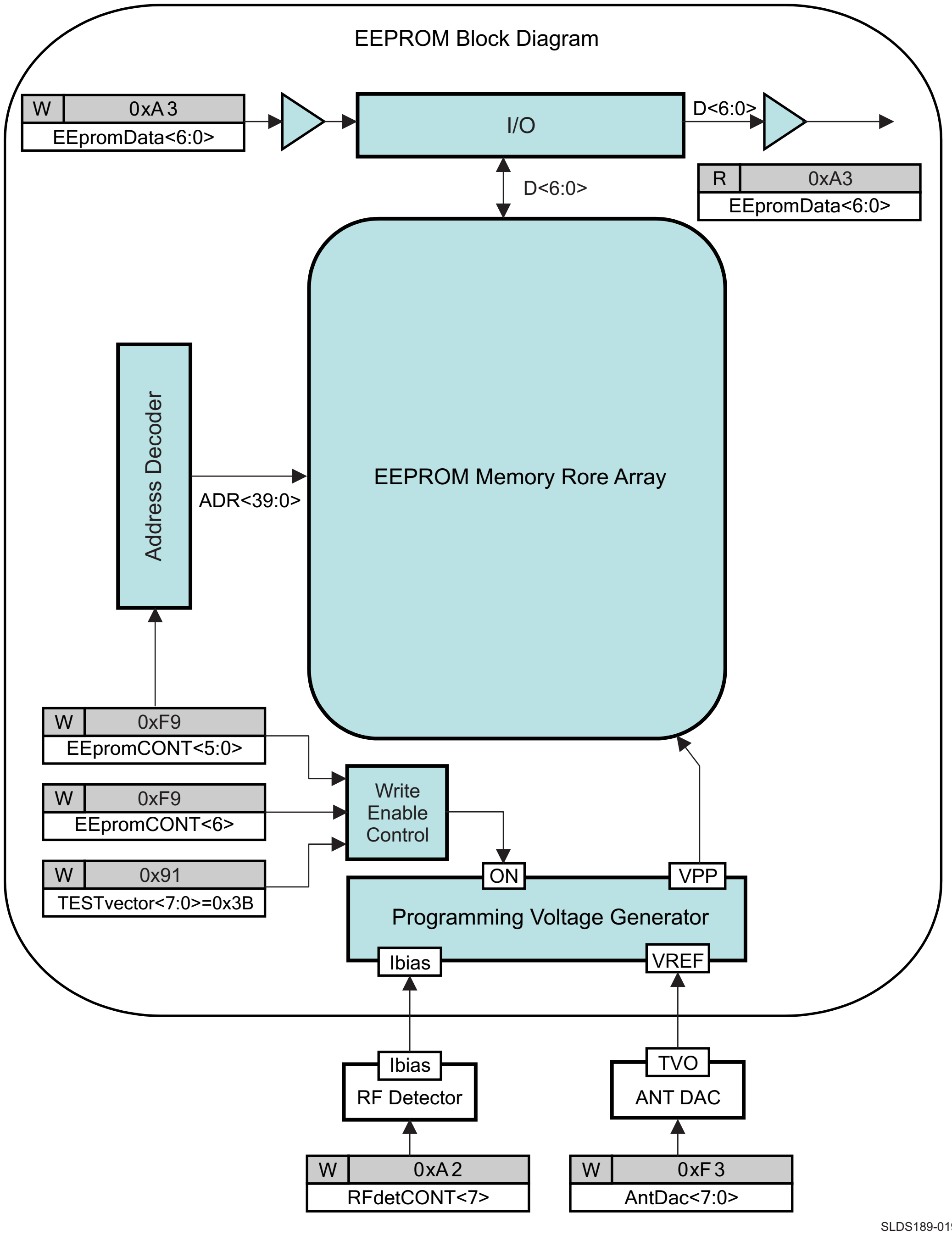
3.2.6.1 EEPROM Block Diagram



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3.2.6.2 EEPROM Unit Structure and DATA/ECC Implementation

EEPROM is mapped on the ESFR space. It has a 43 words memory unit. Each unit has 7 bits (D6:D0). The upper three bits (D6:D4) are allocated for Error Correcting Code (ECC) and the lower four bits (D3:D0) are for data. The ECC contains Hamming codes. Hamming codes can detect up to two simultaneous bit errors, and correct single-bit errors. The Hamming codes are calculated by the following equations:

$$D4 = \overline{D2 \text{ XOR } D1 \text{ XOR } D0}$$

$$D5 = \overline{D3 \text{ XOR } D1 \text{ XOR } D0}$$

$$D6 = \overline{D3 \text{ XOR } D2 \text{ XOR } D0}$$

	ECC				DATA				
One Word	D6	D5	D4		D3	D2	D1	D0	
Hamming Codes	1	1	1	7	0	0	0	0	0
	0	0	0	0	0	0	0	1	1
	1	0	0	4	0	0	1	0	2
	0	1	1	3	0	0	1	1	3
	0	1	0	2	0	1	0	0	4
	1	0	1	5	0	1	0	1	5
	0	0	1	1	0	1	1	0	6
	1	1	0	6	0	1	1	1	7
	0	0	1	1	1	0	0	0	8
	1	1	0	6	1	0	0	1	9
	0	1	0	2	1	0	1	0	A
	1	0	1	5	1	0	1	1	B
	1	0	0	4	1	1	0	0	C
	0	1	1	3	1	1	0	1	D
	1	1	1	7	1	1	1	0	E
	0	0	0	0	1	1	1	1	F

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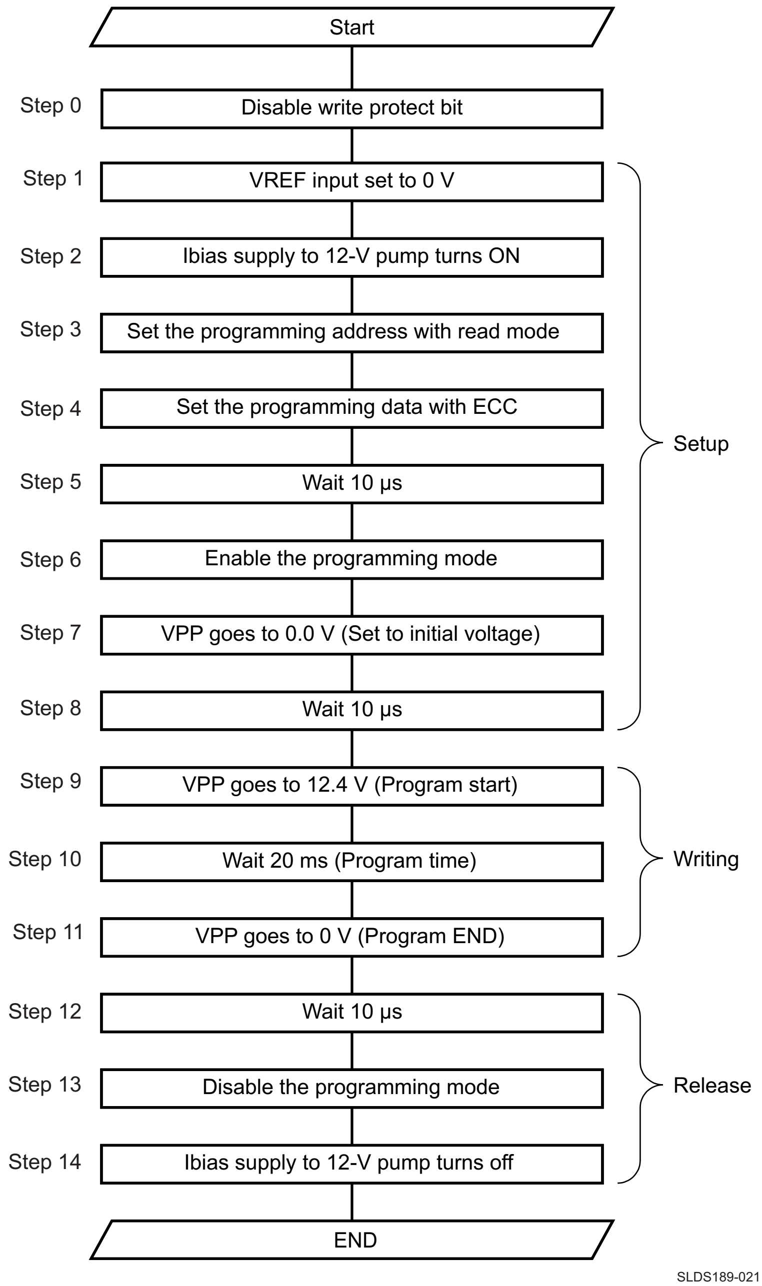
3.2.6.3 EEPROM Programming Procedure



Step	Register		Setting Values	Operation
0	TestVector	0x91	0X3B	Disable write protect
1	AntDac	0xF3	0X00 (OFF)	VREF input set to 0 V
2	RFdetCONT	0xA2	0X80 (ON)	Ibias supply to 12 V PUMP turns on
3	EEprom CONT	0xF9	0x00–0x2A (Write address) + 0x00 (Read mode)(1)	Set the programming address with read mode
4	EEprom Data	0xA3	0x00–0x7F (Write data)	Set the programming data with ECC
5				Wait 10 µs
6	EEprom CONT	0xF9	0x00–0x2A (Write address) + 0x40 (Write mode)(1)	Enable the programming mode
7(2)	AntDac	0xF3	0x00 (OFF) → 0xC0 (ON)	VPP goes to the initial voltage (0 V)
8				Wait 10 µs
9	AntDac	0xF3	0x17 (1.24 V) + 0xC0 (ON)	VPP goes to 12.4 V (Programming voltage)
10				Programming time 20 ms at typical is controlled by firmware.
11	AntDac	0xF3	0x00 (OFF)	VPP goes to 0 V (Forced to GND)
12				Wait 10 µs
13	EEprom CONT	0xF9	0x00–0x2A (Write address) + 0x00 (Read mode)	Disable the programming mode
14	RFdet CONT	0xA2	0x00 (OFF)	Ibias supply to 12 V PUMP turns off

(1) The user areas of EEPROM are assigned from 0x02 to 0x0F. The other areas are reserved for TI internal use and are not usable.
(2) For steps 7–9: The AntDac register should be set to the value of 0xC0 to define the initial voltage of TVO to 0 V. After the register setting, wait about 10 µs. Then the AntDac register is set to the value of 0xD7 to bias the TVO voltage to 1.24 V. The programming voltage generator generates 12.4 V by using the TVO voltage of 1.24 V at typical condition, and the programming voltage can be changed by using the AntDac register. For step 10: programming time is set to 20 ms.

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3.2.6.4 EEPROM Control ESFR

■ EEprom Write Address Register — Not Bit Addressable

ESFR: 0xF9 — EEpromCONT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	EEpromWrite	EEpromWRadd<5:0>					
Access	–	w	w	w	w	w	w	W
At Power on reset	x	0	1	1	1	1	1	1
At Timer reset	x	0	1	1	1	1	1	1

EEpromWrite — ON: (1), OFF: (0)

EEpromWRadd<5:0> — EEprom Write address

■ EEprom DATA Register — Not Bit Addressable

ESFR: 0xA3 — EEpromData

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	EEpromData<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

EEpromData<6:0> — EEprom DATA — Note: This Register is common to RFdetThres<7:0>

■ EEprom DATA Register — Not Bit Addressable

ESFR: 0xA3 — EEpromData

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Testout	EEpromData<6:0>						
Access	r	r	r	r	r	r	r	r
At Power on reset	0	U	U	U	U	U	U	U
At Timer reset	0	S	S	S	S	S	S	S

Testout — Test output

EEpromData<6:0> — EEprom DATA — Note: This Register is common to RFdetThres<7:0>

■ Test Mode Control — Not Bit Addressable

ESFR: 0x91 — TESTvector

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	TestVector<5:0>					
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

TestVector<5:0> — Test Vector Setting;

TestVector<5:0> = 0x3B; Enable to Write access of the EEprom (Upper address: 0x10 to 0x27)

■ RF Detector Control — Not Bit Addressable

ESFR: 0xA2 — RFdetCONT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RFdetPower	–	–	–	–	–	–	–
Access	w	w	w	–	–	–	–	w
At Power on reset	0	0	0	x	x	x	x	U
At Timer reset	U	U	U	x	x	x	x	U

RFdetPower — EEPROM Bias Power Control — Note: This bit is consolidated with RF Detector Power Control.

1 = Power On, 0 = Power Off

■ TX ANT-Tuning DAC control Not Bit Addressable

ESFR: 0xF3 AntDac

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ANTdacPower	SEL_PumpCk	ANTDAC<5:0>					
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	U	U	U	U	U	U	U	U

ANTdacPower Control the EEPROM programming voltage generator power On/Off
0 = Power Off, 1 = Power ON

SEL_PumpCK Charge Pump Clock select:
Always keep to 1 (Internal Oscillator)

ANTDAC<5:0> EEPROM Programming Voltage Control
Set to 0x17 (= 1.24 V) for EEPROM programming

Note: These Register bits are commonly used with Antenna Tuning DAC Control.

3.2.7 MCU8051 Registers

This section describes the internal registers used in the MCU. All I/O, timer/counter and UART operations for the MCU 8051 core are accessed via specific ESFRs. These registers occupy the direct internal data memory spaces of 0x80 to 0xFF.

3.2.7.1 MCU8051 Core SFR Map

Description	Label	Address	Reset Value	Bit Addressable
Port0 (1)	P0	0x80	0xFF	O
Stack Pointer	SP	0x81	0x07	
Data Pointer Low Byte	DPL	0x82	0x00	
Data Pointer High Byte	DPH	0x83	0x00	
Power Control Register (1)	PCON	0x87	0x00	
Timer / Counter Control (1)	TCON	0x88	0x00	O
Timer / Counter Mode Control	TMOD	0x89	0x00	
Timer / Counter 0 Low Byte	TL0	0x8A	0x00	
Timer / Counter 1 Low Byte	TL1	0x8B	0x00	
Timer / Counter 0 High Byte	TH0	0x8C	0x00	
Timer / Counter 1 High Byte	TH1	0x8D	0x00	
Port1 (1)	P1	0x90	0xFF	O
Serial Control Register	SCON	0x98	0x00	O
Serial Data Buffer	SBUF	0x99	0x00	
Port2 (1)	P2	0xA0	0xFF	O
Interrupt Enable Register 0 (1)	IE	0xA8	0x00	O
Port3 (1)	P3	0xB0	0xFF	O
Interrupt Priority Register 0 (1)	IP	0xB8	0xFF	O
Program Status Word	PSW	0xD0	0x00	O
Accumulator	A	0xE0	0x00	O

(1) The following functions and/or registers are not implemented on this device instead the standard 8051 core has:
- Port 0 (0x80), Port 1 (0x98), Port 2 (0xA8) are not connected physically or usable.
- Bit 2 to bit 6 of Port 3 are not physically connected or usable as a general I/O port.
- Extended functions assigned on Port 3 at bit 3 (NINT1), bit 4 (TO), bit 5 (T1) are not connected or usable.
- External Interrupt functions for IE1 and Extended Interrupt functions IE5 through IE13 are not supported or usable.
- Based on 4), the Internal Enable Register 1 (IE1) (0xE8) is not configured or usable.
- Based on 4), the Interrupt Priority Register 1 (IP1) (0xF8) is not configured or usable.
- Based on 4), the control bits of External Interrupt 1 and 5 related functions on the Interrupt Enable Register 0 (IE) (0xA8), bit 2 (EX1) and bit 5 (EI5) are not configured or usable.
- Based on 4), the control bits of External Interrupt 1 and 5 related functions on the Interrupt Priority Register 0 (IP) (0xB8), bit 2 (PX1) and bit 5 (PI5) are not configured or usable.
- Based on 4), the related control bits of IE1 control on Timer/Counter Register (TCON), bit 2 (IT 1) and bit 3 (IE1) are not configured or usable.

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Description	Label	Address	Reset Value	Bit Addressable
Interrupt Enable Register 1 (1)	IE1	0xE8	0x00	O
B Register	B	0xF0	0x00	O
Interrupt Priority Register 1 (1)	IP1	0xF8	0x00	O

3.2.7.2 I/O PORT (P0,P1,P2,P3)

On the 8051 MCU, P0, P1, P2 and P3 are assigned as the 32 quasi-bi-directional I/O lines. However, on the TPIC82000 device, only the ports P3<1:0> can be used for a general purpose I/O (GPIO), the others are not configured or usable.

- I/O PORTS(P0,P1,P2,P3) (1) Bit Addressable

ESFR: 0xB0 P3

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	–	–	–	P3<1>	P3<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	w	r
At Power on reset	1	1	1	1	1	1	1	1
At Timer reset	1	1	1	1	1	1	1	1

Some of the Port 3 have alternate functions as shown below.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	–	–	NINT0	TXD	RXD
	–	–	–	–	–	input	output	Input

BIT1: TXD	output	Serial Transmit Data from UART and transmit clock in UART mode 0.
BIT0: RXD	input	Serial Receive Data to UART

(1) The functions NINT1, T0 and T1 originally assigned at bit 3, bit 4 and bit 5, respectively, on this extended register (on a standard 8051 core) are not supported or usable on the TPIC82000 device.

3.2.7.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into internal data memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory during RET and RETI instructions. Data may also be saved on or retrieved from the stack using PUSH and POP instructions. Instructions that use the stack automatically pre-increment or post-decrement the Stack Pointer. Therefore, the Stack Pointer always points to the last byte written to the stack, which is on the top of the stack. On reset, the Stack Pointer is set to 0x07. The programmer should ensure that the location of the stack in the internal data memory does not interfere with other data stored therein.

- Stack Pointer (SP) Not Bit Addressable

ESFR: 0x81 SP

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SP<7>	SP<6>	SP<5>	SP<4>	SP<3>	SP<2>	SP<1>	SP<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

3.2.7.4 Data Pointer (DPTR)

The Data Pointer (DPTR) is a 16-bit register that may be accessed via the two SFR locations, Data Pointer High Byte (DPH) and Data Pointer Low Byte (DPL). Two true 16-bit operations are allowed on the Data Pointer: load immediate and increment. The Data Pointer is used to form 16-bit addresses for the External Data Memory Accesses (MOVX), for program byte moves (MOVC) and for indirect program jumps (JMP @A+DPTR). On reset, the Data Pointer is set to 0x0000.

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- Data Pointer (DPTR) Not Bit Addressable

ESFR: 0x82 DPL

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DPTR<7>	DPTR<6>	DPTR<5>	DPTR<4>	DPTR<3>	DPTR<2>	DPTR<1>	DPTR<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

ESFR: 0x83 DPH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DPTR<15>	DPTR<14>	DPTR<13>	DPTR<12>	DPTR<11>	DPTR<10>	DPTR<9>	DPTR<8>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

3.2.7.5 8051 Power Control Register (PCON)

The Power Control Register (PCON) controls the power mode and Serial I/F Baud Rate of the 8051 core.

The power supply for the 8051 core on this device is controlled by the System Power Control block and System Power Control Register (ESFR: 0x94). Refer to Section 3.3 for more detail about the device power control.

- Power Control Register (PCON) Not Bit Addressable

ESFR: 0x87 PCON

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SMOD				GF1	GF0	PD	IDL
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

The bit definitions for this register are:

BIT7: SMOD	Double baud rate bit. For use, see the Serial Interface section.
BIT3: GF1	General purpose flag bit
BIT2: GF0	General purpose flag bit
BIT1: PD	Power-Down bit. If 1, Power-Down mode is entered.
BIT0: IDL	Idle bit. If 1, Idle mode is entered.

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3.2.7.6 Timer/Counter Registers

Two 16-bit timer/counters are provided. TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the timer/counters. The timer/counter values are stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

3.2.7.6.1 Timer/Counter Control (TCON)

- Timer/Counter Register (TCON) Bit Addressable

ESFR: 0x88 TCON

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TF1	TR1	TF0	TR0	–	–	IE0	IT0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

The bit definitions for this register are:

Timer1	BIT7: TF1	Timer 1 overflow flag. Set by hardware when Timer/Counter 1 overflows. Cleared by hardware when the processor calls the interrupt service routine.
Timer1	BIT6: TR1	Timer 1 run control. If 1, timer runs; if 0, timer is halted.
Timer0	BIT5: TF0	Timer 0 overflow flag. Set by hardware when Timer/Counter 0 overflows. Cleared by hardware when the processor calls the interrupt service routine.
Timer0	BIT4: TR0	Timer 0 run control. If 1, timer runs; if 0, timer is halted.
External Interrupt1 (1)	BIT3: IE1	External Interrupt 1 edge flag. Set by hardware when an External Interrupt 1 edge is detected.
External Interrupt1 (1)	BIT2: IT1	External Interrupt 1 control bit. If 1, External Interrupt 1 is edge-triggered; if 0, External Interrupt 1 is level triggered.
External Interrupt0	BIT1: IE0	External Interrupt 0 edge flag. Set by hardware when an External Interrupt 0 edge is detected.
External Interrupt0	BIT0: IT0	External Interrupt 0 control bit, if 1, External Interrupt 0 is edge-triggered; if 0, External Interrupt 0 is level triggered.

(1) External Interrupt related functions IE1 and IT1 that are assigned at bit 2 and bit 3, respectively, in the TCON register (in a standard 8051 core) are not supported or usable on the TPIC82000 device.

3.2.7.6.2 Timer/Counter Mode (TMOD)

- Timer/Counter Mode (TMOD) Not Bit Addressable

ESFR: 0x89 TMOD

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	M1(1)	M0(1)	GATE0	CNT0	M1(0)	M0(0)
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

The bit definitions for this register are:

Timer1 (1)	BIT7: GATE1	Timer 1 gate flag. When TCON.6 is set and GATE1 = 1, Timer/Counter 1 only runs if the NINT1 pin is 1 (hardware control). When GATE1 = 0, Timer/Counter 1 only runs if TCON.6 = 1 (software control).
Timer1 (1)	BIT6: CNT1	Timer/Counter 1 selector, if 0, input is from the internal system clock; if 1, input is from the T1 pin.
Timer1	BIT5: M1(1)	Timer 1 Mode control bit M1
Timer1	BIT4: M0(1)	Timer 1 Mode control bit M0
Timer0	BIT3: GATE0	Timer 0 gate flag. When TCON.4 is set and GATE0 = 1, Timer/Counter 0 only runs if the NINT0 pin is 1 (hardware control). When GATE0 = 0, Timer/Counter 0 only runs if TCON.4 = 1 (software control).
Timer0	BIT2: CNT0	Timer/Counter 0 selector. If 0, input is from the internal system clock; if 1, input is from the T0 pin.
Timer0	BIT1: M1(0)	Timer 0 Mode control bit M1
Timer0	BIT0: M0(0)	Timer 0 Mode control bit M0

(1) On the TPIC82000 device, the interrupt pins NINT1 and T1 are not supported. Therefore, the GATE1 and CNT1 functions assigned at bit 7 and bit 6, respectively, in the TMOD register (in a standard 8051 core) are not usable.

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For both timer/counters, the mode bits M0 and M1 apply as shown in the following table:

M1	M0	Operating Mode
0	0	13-bit timer/counter (M8048 compatible mode)
0	1	16-bit timer/counter
1	0	8-bit auto-reload timer/counter
1	1	Timer 0 is split into two halves. TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer/counter controlled by the standard Timer 1 control bits. TH1 and TL1 are held (Timer 1 is stopped).

3.2.7.6.3 *Timer/Counter Data (TL0 TL1 TH0 TH1)*

TL0 and TH0 are the low and high bytes of Timer/Counter 0 respectively. TL1 and TH1 are the low and high bytes of Timer/Counter 1, respectively. In Mode 2, the TL register is an 8-bit counter and TH stores the reload value. On reset, all timer/counter registers are 0x00.

- Timer/Counter Data (TL0 TL1 TH0 TH1) Not Bit Addressable

ESFR: 0x8A TL0

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TL0<7>	TL0<6>	TL0<5>	TL0<4>	TL0<3>	TL0<2>	TL0<1>	TL0<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

ESFR: 0x8B TL1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TL1<7>	TL1<6>	TL1<5>	TL1<4>	TL1<3>	TL1<2>	TL1<1>	TL1<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

ESFR: 0x8C TH0

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TH0<7>	TH0<6>	TH0<5>	TH0<4>	TH0<3>	TH0<2>	TH0<1>	TH0<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

ESFR: 0x8D TH1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TH1<7>	TH1<6>	TH1<5>	TH1<4>	TH1<3>	TH1<2>	TH1<1>	TH1<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

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3.2.7.7 UART Registers

The UART uses two SFRs, SCON and SBUF. SCON is the control register, and SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received and transmitted data registers are independent.

3.2.7.7.1 UART Control (SCON)

■ UART Control (SCON) Bit Addressable

ESFR: 0x98 SCON

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

The bit definitions for this register are:

BIT7: SM0 UART mode specifier

BIT6: SM1 UART mode specifier

BIT5: SM2 UART mode specifier

BIT4: REN If 1, enables reception; if 0, disables reception.

BIT3: TB8 In Modes 2 and 3, this is the ninth data bit sent.

BIT2: RB8 In Modes 2 and 3, this is the ninth data bit received.
In Mode 1, if SM2 = 0, this is the stop bit received.
In Mode 0, this bit is not used.

BIT1: TI Transmit interrupt flag. Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes.
Must be cleared by software.

BIT0: RI Receive interrupt flag. Set by hardware at the end of the eighth bit in Mode 0, or at the half point of the stop bit in other modes.
Must be cleared by software.

The mode control bits operate as shown in the following table:

Mode	SM0	SM1	Operating Mode	Baud Rate[(1)]
Mode 0	0	0	Mode 0: 8-bit shift register	Baud Rate = ftimer_clk / 2
Mode 1	0	1	Mode 1: 8-bit UART	Baud Rate = (SMOD+1) * ftimer_clk / (32 * 2 * (256 – TH1))
Mode 2	1	0	Mode 2: 9-bit UART	Baud Rate = (SMOD+1) * ftimer_clk / 64
Mode 3	1	1	Mode 3: 9-bit UART	Baud Rate = (SMOD+1) * ftimer_clk / (32 * 2 * (256 – TH1))

(1) The ftimer_clk, is the frequency of the TIMER_CLK input (maximum = fcclk/2) and fcclk is the MCU clock frequency.

SM2 enables multi-processor communication over a single serial line and modifies the above. In Modes 2 and 3, if SM2 is set then the receive interrupt is not generated if the received ninth data bit is 0. In Mode 1, the receive interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

3.2.7.7.2 UART Data (SBUF)

This register is used for both transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the two paths are independent.

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- UART Data (SBUF) Not Bit Addressable

ESFR: 0x99 SBUF

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SBUF<7>	SBUF<6>	SBUF<5>	SBUF<4>	SBUF<3>	SBUF<2>	SBUF<1>	SBUF<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

3.2.7.8 Interrupt Registers

The 8051 core on the TPIC82000 device provides the four standard 8051-compatible Legacy interrupts. The standard interrupts have separate enable register bits associated with them, allowing software control. They can also have two levels of priority assigned to them.

The Standard Interrupts: The four standard interrupts are comprised of two timer overflow interrupts, an interrupt associated with the built-in serial interface for the core, and one external interrupt (referred to as Legacy external interrupts).

The Two Timer Overflow Interrupts: TF0 and TF1, are set whenever Timer 0 or Timer 1, respectively, roll-over to zero. The states of these interrupts are also stored in the TCON register. TF0 and TF1 are automatically cleared by hardware on entry to the corresponding interrupt service routine.

The Serial Interrupt: The serial interrupt source comprises the logical OR of the two serial interface status bits RI and TI in the register SCON. These are set automatically upon receipt or transmission of a data frame. These two bits are not cleared by hardware.

The Legacy External Interrupts: NINT0 is driven from input PORT3 (see). This interrupt may be either edge- or level-sensitive, depending on the settings within the TCON register. A further TCON register bit, IE0, acts as an interrupt flag. If the external interrupt is set to be edge-triggered, the corresponding register bit IE0 is set by a falling edge on NINT0 and cleared by hardware on entry to the corresponding interrupt service routine. If the interrupt is set to be level-sensitive, IE0 reflects the logic level on NINT0. (The TCON register is described in Section 3.2.7.6).

NOTE

1. All events on NINT0, whether level-triggered or edge-triggered, are detected by sampling the relevant interrupt line on the rising edge of SCLK at the end of phase 1 of every machine cycle. Where NINT0 is level-triggered, a response is made to the signal being sampled low and, to ensure detection, the external source needs to hold the line low until the resulting interrupt is generated. (It also needs to ensure that the request is deactivated before the end of the associated service routine). Where NINT0 is edge-triggered, the response is made to a transition on the signal from high to low between successive samples. This means that to ensure detection, NINT0 needs to be high for at least two clocks before it goes low and then needs to be held low for at least two clocks after this transition.
2. On a standard 8051, the second Legacy External Interrupt (NINT1) is supported. However, on the TPIC82000 device, this function is not supported.

   The nine Extended Interrupts (IE5 through IE13) on standard MCU8051 are also not supported on the TPIC82000 device.

3.2.7.8.1 Interrupt Flag Clear

If the Legacy External Interrupt (NINT0) is edge-triggered, the interrupt flag is cleared on vectoring to the service routine. If it is level-triggered, the flag is controlled by the external signal. Timer/counter flags are cleared on vectoring to the interrupt service routine but the serial interrupt flag is not affected by hardware. The serial interrupt flag should be cleared by software. Acknowledge signals are provided for clearing any registers used to source the nine additional interrupts.

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3.2.7.8.2 Priority Levels / Interrupt Vectors

One of two priority levels may be selected for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt and, if two interrupts of different priority occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed.

When an interrupt is serviced, a long call instruction is executed to one of the following locations, according to the interrupt source:

Source	Level	Description	Vector Address
IE0	1 (Highest)	External Interrupt 0	0x0003
TF0	2	Timer/Counter Interrupt 0	0x000B
IE1 (1)	3	External Interrupt 1	0x0013
TF1	4	Timer/Counter Interrupt 1	0x001B
RI+TI	5	Serial Interrupt	0x0023
IE5 (1)	6	External Interrupt 5	0x002B
IE6 (1)	7	External Interrupt 6	0x0033
IE7 (1)	8	External Interrupt 7	0x003B
IE8 (1)	9	External Interrupt 8	0x0043
IE9 (1)	10	External Interrupt 9	0x004B
IE10 (1)	11	External Interrupt 10	0x0053
IE11 (1)	12	External Interrupt 11	0x005B
IE12 (1)	13	External Interrupt 12	0x0063
IE13 (1)	14 (Lowest)	External Interrupt 13	0X006B

(1) The Internal Interrupt 1 (IE1) and Extended Interrupts (IE5 through IE13) are not supported on TPIC82000 and are not usable.

3.2.7.8.3 Interrupt Latency

The response time in a single interrupt system is between three and nine machine cycles.

3.2.7.8.4 Interrupt Enable Register 0 (IE)

■ Interrupt Enable Register 0 (IE) Bit Addressable

ESFR: 0xA8 IE

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	EA		–	ES	ET1	–	ET0	EX0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

For each bit in this register, a 1 enables the corresponding interrupt and a 0 disables it.

BIT7: EA	Enable or disable all interrupt bits
BIT5: EI5 (1)	Enable External Interrupt 5
BIT4: ES	Enable Serial Port interrupt
BIT3: ET1	Enable Timer 1 overflow interrupt
BIT2: EX1 (1)	Enable External Interrupt 1
BIT1: ET0	Enable Timer 0 overflow interrupt
BIT0: EX0	Enable External Interrupt 0

(1) On the TPIC82000 device, the External Interrupt 1 (IE1) and Extended Interrupts (IE5 to ID13) are not supported. Therefore, the EX1 and EI5 function assigned at bit 2 and bit 5, respectively, on this IE register are not usable. Also, the Interrupt Enable Register 1 (IE1) Register (0xE8) is not configured or supported.

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3.2.7.8.5 Interrupt Priority Register 0 (IP)

- Interrupt Priority Register 0 (IP) Bit Addressable

ESFR: 0xB8 IP

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	PS	PT1	–	PT0	PX0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	1	1	1	1	1	1	1	1
At Timer reset	1	1	1	1	1	1	1	1

For each bit in this register, a 1 selects high priority for the corresponding interrupt and a 0 selects low priority. The allocation of interrupts to bits is:

BIT5: PI5(1) Select priority for External Interrupt 5
BIT4: PS Select priority for Serial Port interrupt
BIT3: PT1 Select priority for Timer 1 overflow interrupt
BIT2: PX1(1) Select priority for External Interrupt 1
BIT1: PT0 Select priority for Timer 0 overflow interrupt
BIT0: PX0 Select priority for External Interrupt 0

While an interrupt is being serviced, it may only be interrupted by a higher priority interrupt.

(1) On the TPIC82000 device, the External Interrupt 1 (IE1) and Extended Interrupts (IE5 to ID13) are not supported. Therefore, the PX1 and PI5 functions assigned at bit 2 and bit 5, respectively, on this IE register are not usable. Also, the Interrupt Enable Register 1 (IE1) Register (0xE8) is not configured or supported.

3.2.7.9 Program Status Word (PSW)

- Program Status Word (PSW) Bit Addressable

ESFR: 0xD0 PSW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CY	AC	F0	RS1	RS0	OV	F1	P
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

This register contains status information resulting from CPU and ALU operation. The bit definitions are:

BIT7: CY ALU carry flag
BIT6: AC ALU auxiliary carry flag
BIT5: F0 General purpose user-definable flag
BIT4: RS1 Register Bank Select bit 1
BIT3: RS0 Register Bank Select bit 0
BIT2: OV ALU overflow flag
BIT1: F1 User-definable flag
BIT0: P Parity flag. Set each instruction cycle to indicate odd/even parity in the accumulator.

The Register Bank Select bits operate as shown in the following table:

RS1	RS0	Register Bank Select
0	0	RB0: Registers from 00 - 07 hex
0	1	RB1: Registers from 08 - 0F hex
1	0	RB2: Registers from 10 - 17 hex
1	1	RB3: Registers from 18 - 1F hex

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3.2.7.10 Accumulator (ACC)

This register provides one of the operands for most ALU operations. It is denoted as A in the instruction table.

- Accumulator (ACC) Bit Addressable

ESFR: 0xE0 ACC

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>	ACC<1>	ACC<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

3.2.7.11 B Register (B)

This register provides the second operand for multiply or divide instructions, otherwise it may be used as a scratch pad register.

- B Register (B) Bit Addressable

ESFR: 0xF0 B

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	B<7>	B<6>	B<5>	B<4>	B<3>	B<2>	B<1>	B<0>
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

3.2.8 Instruction Definitions

The MCU8051 Warp instruction set is shown in Table 3-2. Some of the features supported are outlined below.

3.2.8.1 Addressing Modes

The instruction set provides a variety of addressing modes, which are outlined below.

3.2.8.1.1 Direct Addressing

In direct addressing, the operand is specified by an 8-bit address field. Only internal data and SFRs may be accessed using this mode.

3.2.8.1.2 Indirect Addressing

In indirect addressing, the operand is specified by an address contained in a register. Two registers (R0 and R1) from the current bank or the Data Pointer may be used for addressing in this mode. Both internal and external data memory may be indirectly addressed.

3.2.8.1.3 Register Addressing

In register addressing, the operand is specified by the top 3 bits of the opcode, which selects one of the current bank of registers. Four banks of registers are available. The current bank is selected by bits 3 and 4 of the PSW.

3.2.8.1.4 Register Specific Addressing

Some instructions only operate on specific registers. This is defined by the opcode. In particular many accumulator operations and some Stack Pointer operations are defined in this manner.

3.2.8.1.5 Immediate Data

Instructions which use immediate data are 2 or 3 bytes long and the immediate operand is stored in program memory as part of the instruction.

3.2.8.1.6 Indexed Addressing

Only program memory may be addressed using indexed addressing. It is intended for simple implementation of look-up tables. A 16-bit base register (either the PC or the DPTR) is combined with an offset stored in the accumulator to access data in program memory.

3.2.8.2 Arithmetic Instructions

The M8051 Warp implements ADD, Add with Carry (ADDC), Subtract with Borrow (SUBB), Increment (INC) and Decrement (DEC) functions, which may be used in most addressing modes. There are three accumulator-specific instructions: Decimal Adjust A (DA A), Multiply A by B (MUL AB) and Divide A by B (DIV AB).

3.2.8.3 Logic Instructions

The M8051 Warp implements AND Logical (ANL), OR Logical (ORL), and Exclusive-OR Logical (XRL) functions, which again may be used in most addressing modes. There are seven accumulator-specific instructions, Clear A (CLR A), Complement A (CPL A), Rotate Left A (RL A), Rotate Left through Carry A (RLC A), Rotate Right A (RR A), Rotate Right through Carry A (RRC A), and Swap Nibbles of A (SWAP A).

3.2.8.4 Data Transfers

3.2.8.4.1 Internal Data Memory

Data may be moved from the accumulator to any internal data memory location, from any internal data memory location to the accumulator, and from any internal data memory location to any SFR or other internal data memory location.

3.2.8.4.2 External Data Memory

Accessing to the external data memory is not supported by the TPIC82000 device.

3.2.8.5 Jump Instructions

3.2.8.5.1 Unconditional Jumps

Four sorts of unconditional jump instructions are available. Short jumps (SJMP) are relative jumps (limited to –128 to +127 bytes), long jumps (LJMP) are absolute 16-bit jumps, and absolute jumps (AJMP) are absolute 11-bit jumps (in effect, within a 2K byte memory page). The last type is an Indexed jump (JMP @ A+DPTR) which jumps to a location contained in the DPTR register, and is offset by a value stored in the accumulator.

3.2.8.5.2 Subroutine Calls and Returns

There are only two sorts of subroutine calls, absolute calls (ACALL) and long calls (LCALL). Two return instructions are provided: RET and RETI (RETI is for interrupt service routines).

3.2.8.5.3 Conditional Jumps

Conditional jump instructions all use relative addressing, so they are also limited to the –128 to +127 byte range.

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3.2.8.6 Boolean Instructions

The bit-addressable registers in both direct and SFR space may be manipulated using boolean instructions. Logical functions are available which use the carry flag and an addressable bit as the operands and each addressable bit may be set, cleared, or tested in a jump instruction.

3.2.8.7 Flags

The following instructions affect flags generated by the ALU:

Table 3-1. Flags Instructions(1)

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	?	?	?	CLRC	0		
ADDC	?	?	?	CPLC	?		
SUBB	?	?	?	ANL C, bit	?		
MUL	0	?		ANL C, /bit	?		
DIV	0	?		ORL C, bit	?		
DA	?			ORL C, /bit	?		
RRC	?			MOV C, bit	?		
RLC	?			CJNE	?		
SETB C	1						

(1) In this table, a 0 means the flag is always cleared, a 1 means the flag is always set and a ? means that the state of the flag depends on the result of the operation. The flag specified as blank means that the state is unknown.

3.2.8.8 Instruction Table

Instructions are either 1, 2, or 3 bytes long, as listed in the Bytes column in Table 3-2.

Each instruction takes either one, two, or four machine cycles to execute as listed in Table 3-2. One machine cycle comprises two CCLK clock cycles.

Table 3-2. Instruction Table

Mnemonic	Description	Bytes	Cycles	Hex code
ARITHMETIC				
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4
LOGICAL				
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64

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Table 3-2. Instruction Table (continued)

Mnemonic	Description	Bytes	Cycles	Hex code
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13
DATA TRANSFER				
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri(1)	Move external data (A8) to A	1	2	E2-E3
MOVX A,@DPTR(1)	Move external data (A16) to A	1	2	E0
MOVX @Ri,A(1)	Move A to external data (A8)	1	2	F2-F3
MOVX @DPTR,A (1)	Move A to external data (A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7
BOOLEAN				
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82

(1) Since the accessing of External Memory is not supported on TPIC82000, the related instructions: MOVX A,@Ri, MOVX A, @DPTR, MOVX @Ri, A and MOVX `DPTR,A are not usable.

Table 3-2. Instruction Table (continued)

Mnemonic	Description	Bytes	Cycles	Hex code
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92
BRANCHING				
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠ 0	2	2	70
CJNE A,dir,rel	Compare A, direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A, immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5
MISCELLANEOUS				
NOP	No operation	1	1	00

In the Table 3-2, an entry such as E8-EF indicates a continuous block of hex opcodes used for eight different registers, the register numbers of which are defined by the lowest 3 bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, the top 3 bits of the code are used to store the top 3 bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

3.3 System Power Controller and Status Monitor

The system power block controls the power on/off of the MCU and peripheral blocks. The system power block consists of a power supply block, a system power control block to control the MCU operation, wake-up trigger detectors, and control registers.

The system can be awakened by one of the following trigger events: Power-on-Reset at the first time connection of the external power supply such as a lithium battery, LF receiver when the LF wake-up trigger signal is detected or Wake-up Timer which initiates the wake-up trigger signal periodically according to the preset interval timer value.

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3.3.1 System Power Block Diagram

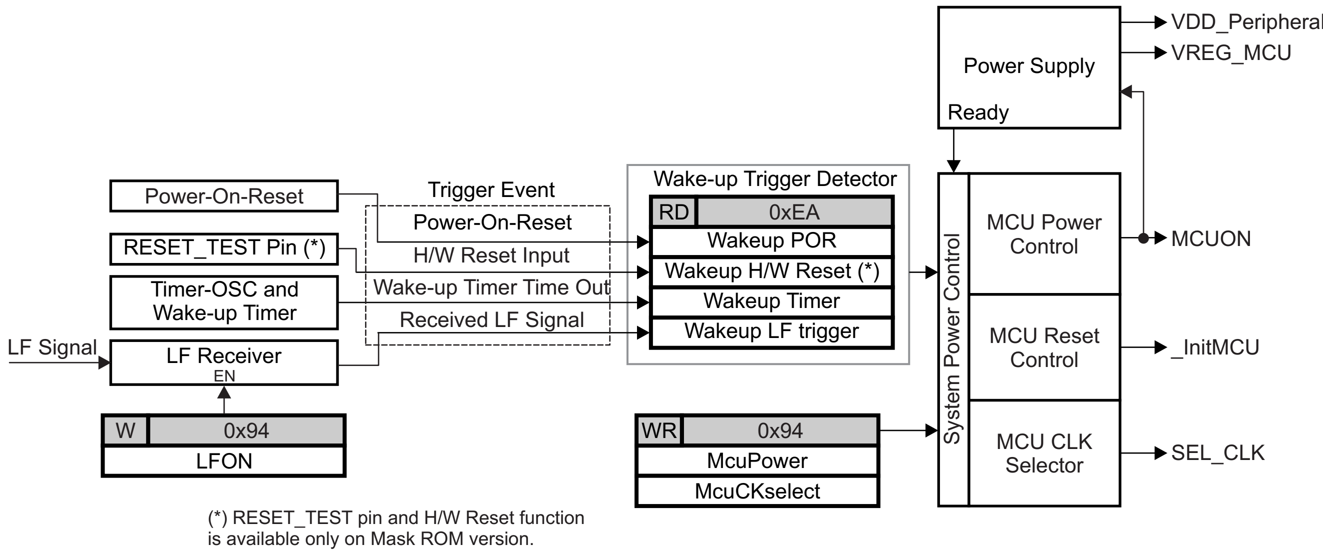

Figure 3-5. System Power Controller and Status Monitor

3.3.2 System Wake-up Operation

To minimize the power dissipation of the system, the device can be programmed to stay in sleep mode and then wake up periodically to measure and transmit the necessary data using either the internal ultra low power timer or by detecting the LF trigger signal from the external control units. All mode transitions are controlled by the software, and therefore, the total power dissipation of the system will depend on the user's application program. This section describes the basic device state sequences shown in Figure 3-7 and Figure 3-6.

Power-on-Reset: Just after the battery is attached, the device generates an internal Power_On_Reset signal to initialize the necessary blocks of the device. After the release of Power_On_Reset, the internal regulator starts up and then the internal clock system starts up following the Ready_VREG signal which indicates the regulator voltage is sufficient for system operation. Then, the MCU wakes up and starts the system initialization programs. After the completion of the system initialization sequence and necessary programs, the device enters into sleep mode, sets the appropriate registers and waits for the next wake-up timing signal from the internal timer.

Timer Wake-up: If the system is set to measure and transmit the necessary data periodically, the device will wake up automatically with the pre-programmed internal timer, complete each required program for the sensor measurements and data transmission, and to go into sleep mode again. Since no external trigger signals are required to wake up the device, this operation sequence may provide the simplest system configuration.

LF Wake-up: The device has an LF signal detection feature to wake up the device when the LF trigger command from the external system (Body Control ECU) is detected. This feature enables the device to sniff and compare the corresponding LF signals with the pre-configured internal logic circuit without waking up the MCU, which may consume more power for trigger event detection. Once the LF signal is detected and the ID and/or data pattern match is confirmed, the MCU wakes up and completes the required programmed operations.

G-Detect Wake-up: The device can also start the programmed operations after the detection of the accelerator signals. In this mode, the MCU needs to be awakened by the internal timer first to start the accelerometer output measurement. Then, if the accelerometer output exceeds the preset value, the device performs the programmed operations, otherwise it will return to sleep mode.

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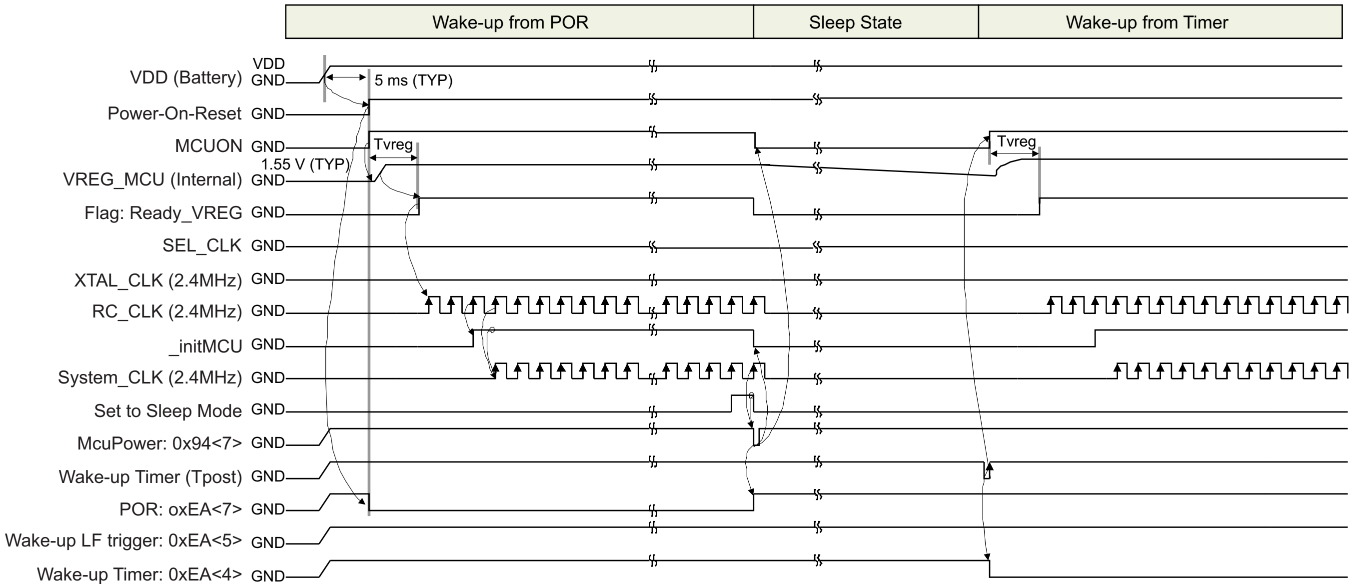

Figure 3-6. System Wake-up Timing

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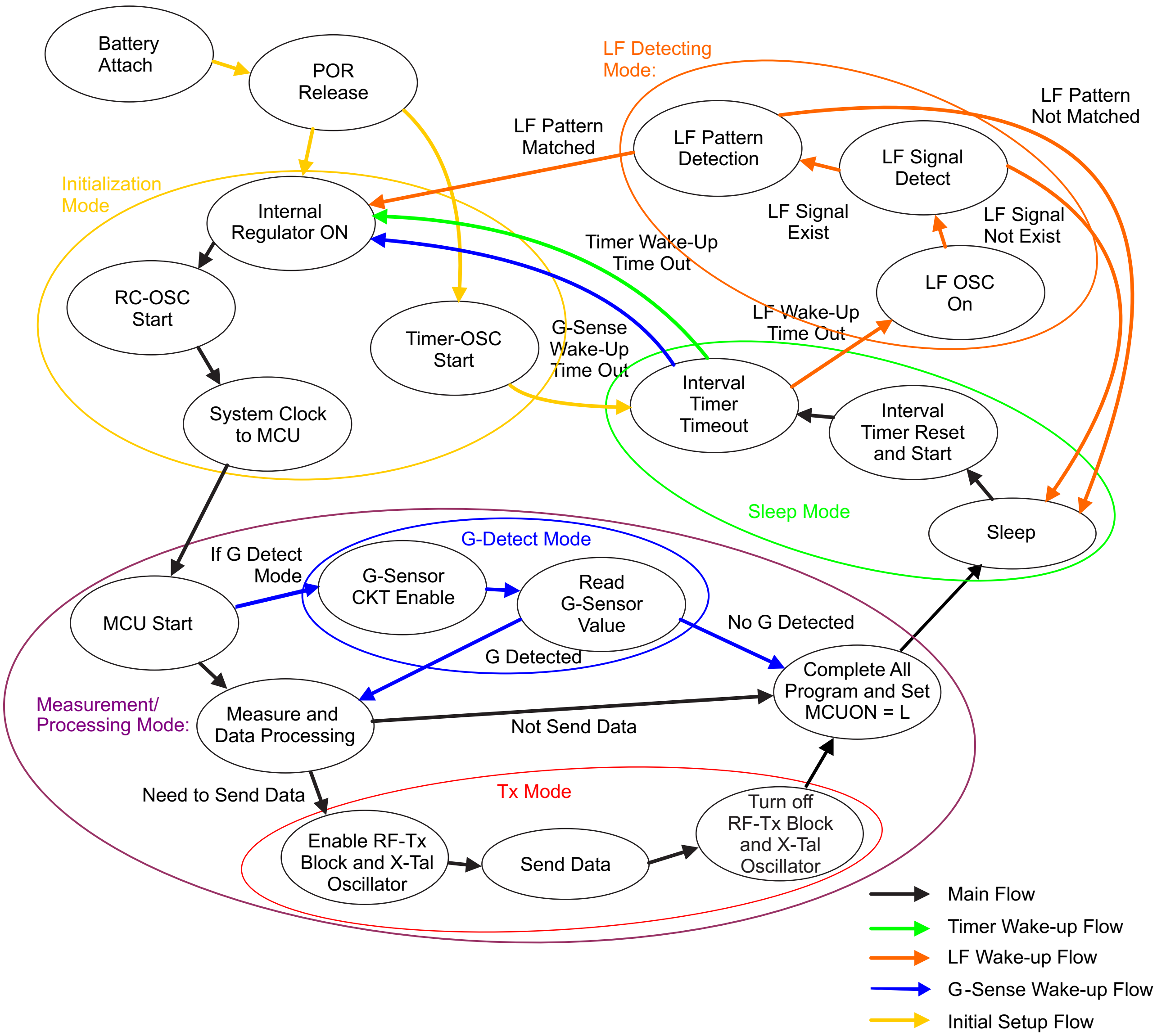

Figure 3-7. System Power On/Off State Diagram (Example)

3.3.3 System Power Control ESFR

- System Power control Register — Not Bit Addressable

ESFR: 0x94 — SystemPower

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	McuPower	McuCKselect	LFON	–	–	–	–	–
Access	w	w	w	–	–	–	–	–
At Power on reset	1	0	0	x	x	x	x	x
At Timer reset	1	0	0	x	x	x	x	x

McuPower — Main Power (for MCU and Peripheral Analog Function) Off Control:
To turn off the main power of the device and go into the sleep mode, set this bit to 0. At the following rising edge of the System Clock, the Power of the device is turned off. This bit is cleared (preset to 1) automatically by the internal logic circuit. The wake-up of the device is controlled by the Wakeup Events (POR, Timer, LF trigger) automatically.

McuCKselect — Main Clock (for MCU and Peripheral Analog Function) Select: XTAL-OSC (1), RC-OSC (0)

LFON — LF Receiver ON: ON (1), OFF (0) — Turn on the LF Receiver while the MCU is on.
(LF Receiver wakes up only one time when this bit is set to 1, and aborted if no LF signal is detected.)

- System state Register — Not Bit Addressable

ESFR: 0xEA — SystemState

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Wakeup POR	–	Wakeup LF trigger	Wakeup Timer-1	Wakeup H/W Reset	Flag Invalid	Wakeup Timer-2	FLAG Xtal clock
Access	r	–	r	r	r	r	r	r
At Power on reset	0	x	1	1	1	1	1	0
At Timer reset	1	x	D	D	1	D	D	0

Wakeup POR — Status Flag of Wakeup by POR — Active (0), Not Active (1)

Wakeup H/W Reset — Status Flag of Wakeup by H/W Reset — Active (0), Not Active (1) — (Valid for ROM version only)

FLAG Xtal clock — XTAL-OSC status: — Active (1), Not Active (0)

Bit 5 Wakeup LF Trigger	Bit 4 Wakeup Timer-1	Bit 2 Flag_Invalid	Bit 1 Wakeup Timer 2	Status	MCU Wakeup Status (When reading the System State just after MCU start up) (except status B)
0	1	1	1	A	Standard LF Wakeup (Need to check whether status B occurs or not before going into sleep mode) (1)
0	0	1	1	B	Timer Wakeup occurred after the standard LF Wakeup (Detect if this status is occurring or not before going into sleep mode) (1)
1	0	1	0	C	Standard Timer Wakeup
0	1	1	0	D	Timer Wakeup and LF Wakeup occurs almost at the same time. (2)(3)
0	0	1	0	E	
1	0	0	0	F	Timer Wakeup occurs twice while the MCU is on. (4)
0	0	0	0	G	Timer Wakeup occurs twice while the MCU on by LF trigger. (4)

(1) If the Timer Wakeup event occurs while processing LF command, the Timer Wakeup event won't affect the operation but the SystemState register bit 4 (Wakeup Timer-1) is set to 0. So, confirm the status of Wakeup Timer-1 after the completion of LF command processing and if the bit is set to 0, proceed with the Timer Wake-up operation. With this sequence, both LF Wakeup and Timer Wakeup functions are achieved at the same time without conflicts.

(2) If the reading of SystemState register is either D or E state, the LF Wakeup and Timer Wakeup occurs at almost the same time. In this case, make the application program process the LF Wakeup operation first and then complete the Timer Wakeup operation.

(3) The D status occurs when the LF Wakeup trigger is detected just after the down edge of the Timer Wakeup signal (before the MCU startup). And the E status occurs when the LF Wakeup trigger is detected just after the rising edge of the Timer Wake-up signal (before the MCU startup). In either case, the recommendation is to process the Timer Wakeup operation after the completion of the LF Wakeup command processes.

(4) The F and G status do not occur in normal application. They indicate that the MCU is not going into sleep mode properly and requires the Error Process by the application software. Status F indicates that the error condition is occuring while the MCU is on and status G indicates that the error condition occurs after the LF Wakeup.
In addition, no other status except A to G should occur in the system. Therefore, if such a condition is detected, proceed to the Error Process.

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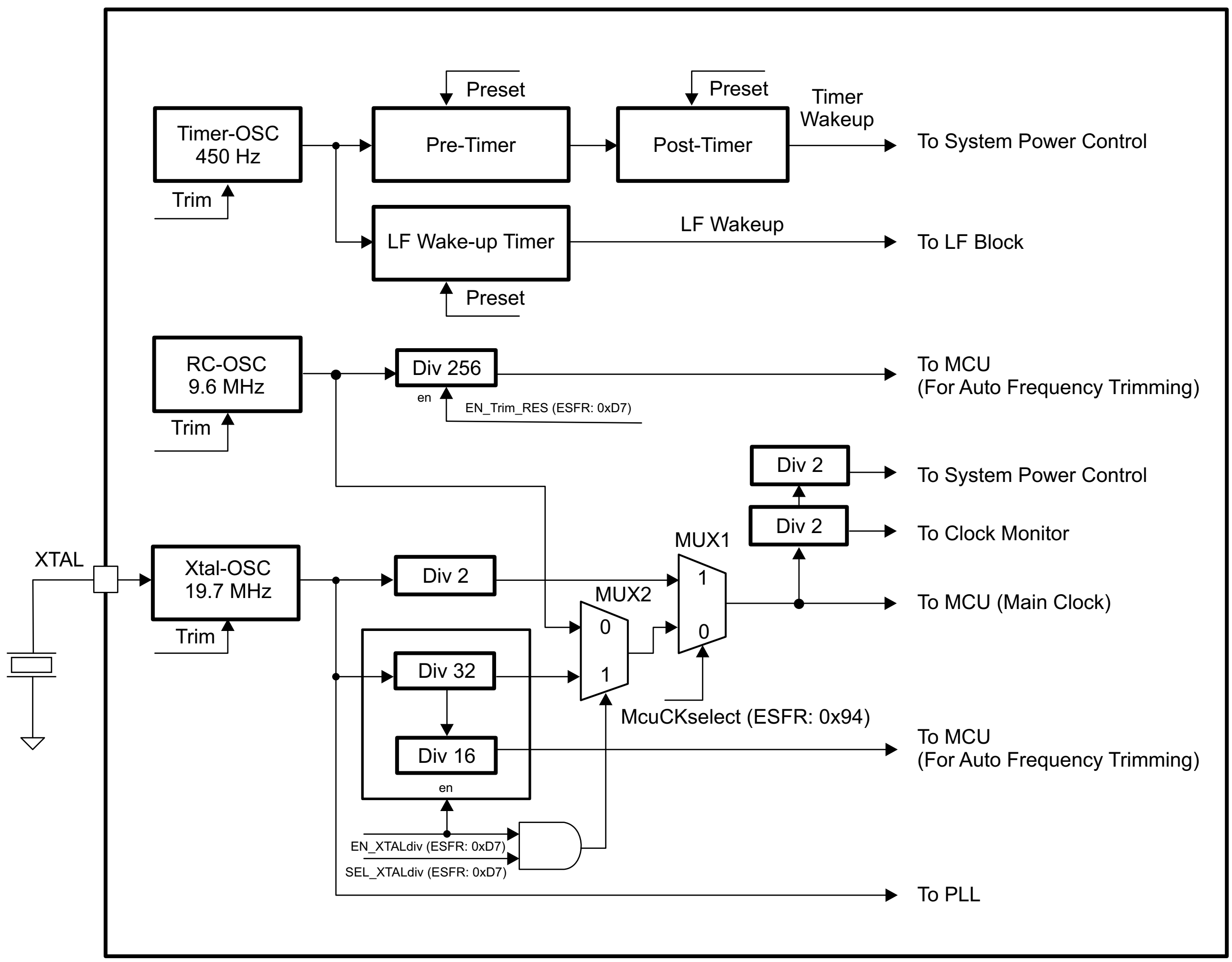
3.4 Internal Clocks System

The TPIC82000 device has three main oscillator/clock systems: timer oscillator (Timer-OSC), RC oscillator (RC-OSC), and crystal oscillator (Xtal-OSC). An ultra low power Timer-OSC is used for the interval count for the periodical wake up of the whole system. The RC-OSC is mainly used for the MCU clock when operating the sensor blocks and processing the normal program. The Xtal-OSC is used for the MCU clock when operating the RF transmitter block and also to trim the Timer-OSC and RC-OSC.

3.4.1 Internal Clock System Block Diagram

The Timer-OSC generates a 450 Hz (typical) clock for the interval time count of the system wake-up (Pre-Timer and Post-Timer) timing and LF Wakeup Timing. The RC-OSC generates a 9.6 MHz clock for the MCU main clock and sensor measurements. The Xtal-OSC generates a 19.7 MHz clock for the MCU main clock and for the RF data transmission. A multiplexor is used to select either the RC-OSC or the 1/2 divided Xtal-OSC outputs for the main clock of the MCU depending on the operation mode. In idle mode of the MCU, a 1/32 divided Xtal-OSC clock can be used at MCU for power savings.

The Xtal-OSC output will also be used for the calibration of the Timer-OSC and RC-OSC to ensure the accuracy of the clock system. This trimming function can be achieved by the software.



NOTE: The sequences below must be followed when switching the MCU clock source between RC-OSC and Xtal-OSC.

1)	**MCU Clock Source [RC-OSC → Xtal-OSC (Div 2)]:**		
a)	MUX1 (0): MUX2 (0)	: MCU is Running at RC-OSC	[McuCKselect = 0, EN_XTALdiv, SEL_XTALdiv = 0]
b)		: Start the Xtal-OSC and Standby	
c)	MUX1 (0 → 1)	: The MCU clock is switched to Xtal-OSC (Div 2).	[McuCKselect = 1]
2)	**MCU Clock Source [Xtal-OSC (Div 2) → RC-OSC]:**		
a)	MUX1 (1): MUX2 (0)	: MCU is Running at Xtal-OSC (Div 2)	[McuCKselect = 1, EN_XTALdiv, SEL_XTALdiv = 0]
b)	MUX1 (1 → 0)	: The MCU clock is switched to RC-OSC.	[McuCKselect = 0]
c)		: Power-OFF Xtal-OSC	
3)	**MCU Clock Source [RC-OSC → Xtal-OSC (Div 32)]:**		
a)	MUX1 (0): MUX2 (0)	: MCU is Running at RC-OSC.	[McuCKselect = 0, EN_XTALdiv, SEL_XTALdiv = 0]
b)		: Start the Xtal-OSC and Standby	
c)	MUX1 (0 → 1)	: The MCU clock is switched to Xtal-OSC (Div 2).	[McuCKselect = 1]
d)	MUX2 (0 → 1)	:	[EN_XTALdiv, SEL_XTALdiv = 1]
e)	MUX1 (0 → 0)	: The MCU clock is switched to Xtal-OSC (Div 32).	[McuCKselect = 0]
4)	**MCU Clock Source [Xtal-OSC (Div 32) → RC-OSC]:**		
a)	MUX1 (0): MUX2 (1)	: MCU is Running at Xtal-OSC (Div 32)	[McuCKselect = 0 , EN_XTALdiv, SEL_XTALdiv = 1]
b)	MUX1 (0 → 1)	: The MCU clock is switched to Xtal-OSC (Div 2).	[McuCKselect = 1]
c)	MUX2 (1 → 0)	:	[EN_XTALdiv, SEL_XTALdiv = 0]
d)	MUX1 (10 → 0)	: The MCU clock is switched to RC-OSC.	[McuCKselect = 0]
e)		: Power-OFF Xtal-OSC	

3.4.2 Timer Oscillator (Timer-OSC)

The Timer-OSC is used for periodical wake up and abort functions. Since the Timer-OSC always runs even if the MCU is in sleep mode, the Timer-OSC has low current consumption. The oscillation frequency of the Timer-OSC should be calibrated by using the Xtal-OSC periodically. A register of TimerOSC<3:0> (0x97), can control current and oscillation frequency of the Timer-OSC. A register of TimerOSC_DIV<2:0> (0x97), can also control the oscillation frequency of the Timer-OSC by changing a number of divider.

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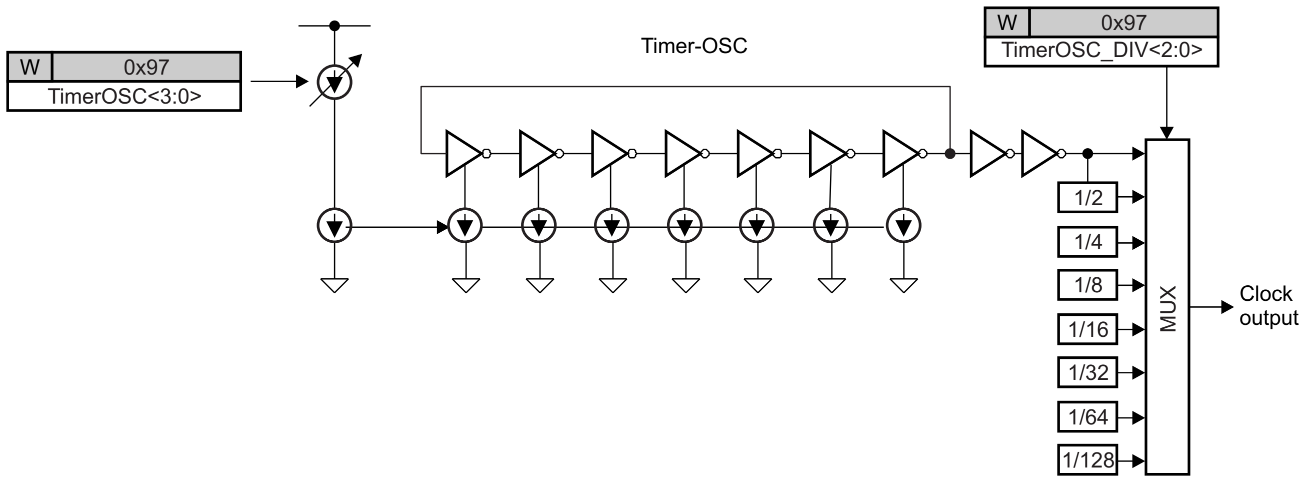


■ Timer-OSC Not Bit Addressable

ESFR: 0x97 TimerOSC

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TM	TimerOSC_DIV<2:0>			TimerOSC<3:0>			
Access	w	w	w	W	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	S	S	S	S	S	S	S

TM Test Mode. Always set to 0.

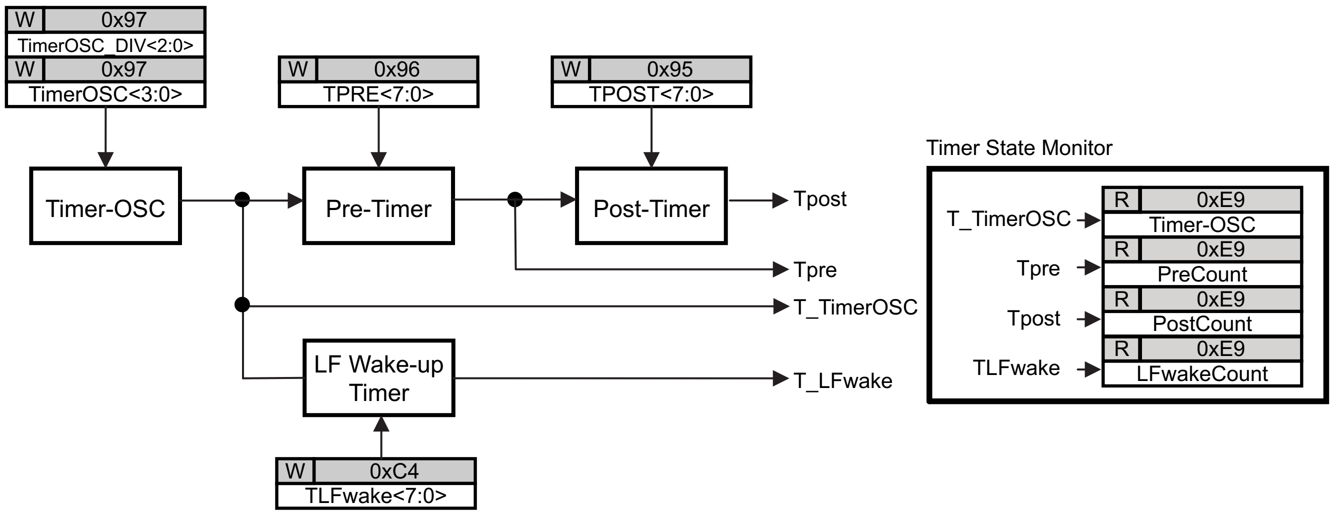
TimerOSC_DIV<2:0> Frequency divider setting of the Timer-OSC output.

TimerOSC_DIV<2>	TimerOSC_DIV<1>	TimerOSC_DIV<0>	DIV
1	1	1	1
1	1	0	1/2
1	0	1	1/4
1	0	0	1/8
0	1	1	1/16
0	1	0	1/32
0	0	1	1/64
0	0	0	1/128

TimerOSC<3:0> Bias current setting of the Timer-OSC. The oscillation frequency is proportional to the current.
TimerOSC<3:0> = F provides the maximum bias current and the fastest oscillation frequency
TimerOSC<3:0> = 0 provides the minimum bias current an the slowest oscillation frequency

3.4.2.1 Interval Timer

The interval timer consists of three dividers that are used to generate clocks that provide the required time period for several functions such as the wake-up interval time, and the LF wake-up interval. The clock period (dividing ratio) of the Pre-Timer, Post-Timer, and LF Wake-up Timer can be changed by using ESFRs: TimerPre (0x96: TPRE<7:0>), TimerPost (0x95: TPOST<7:0>) and TimerLFwake (0xC4: TLFwake<7:0>). The APIs are prepared to support this timer setting and can be called by the application software. For detail about the timer setting, refer to the SW Application manual.



■ Timer PreCounter Divider — Not Bit Addressable

ESFR: 0x96 — TimerPre

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TPRE<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	1	1	1	1	1	1	1	1
At Timer reset	S	S	S	S	S	S	S	S

TPRE<7:0> Timer Pre-Counter Divider ratio.

PreTimer Period:
Tpre = T_TimerOSC * (TPRE<7:0> +1)

■ Timer PostCounter Divider — Not Bit Addressable

ESFR: 0x95 — TimerPost

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TPOST<7:0>							
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	1	1	1	1	1	1	1	1
At Timer reset for r	D	D	D	D	D	D	D	D
At Timer reset for w	S	S	S	S	S	S	S	S

TPost<7:0> Timer Post-Counter Divider ratio.

PostTimer Period:
Tpost = Tpre * (TPOST<7:0> +1)

■ Timer LFwakeCounter Divider — Not Bit Addressable

ESFR: 0xC4 — TimerLFwake

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	TLFwake<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	1	1	1	1	1	1	1	1
At Timer reset	S	S	S	S	S	S	S	S

TLFwake<7:0> Timer LFwake-Counter Divider ratio.

LFwakeTimer Period:
TLFwake = T_TimerOSC * (TLFwake<7:0> +1)

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■ Timer State / RC-OSC State — Not Bit Addressable

ESFR: 0xE9 — TimerState

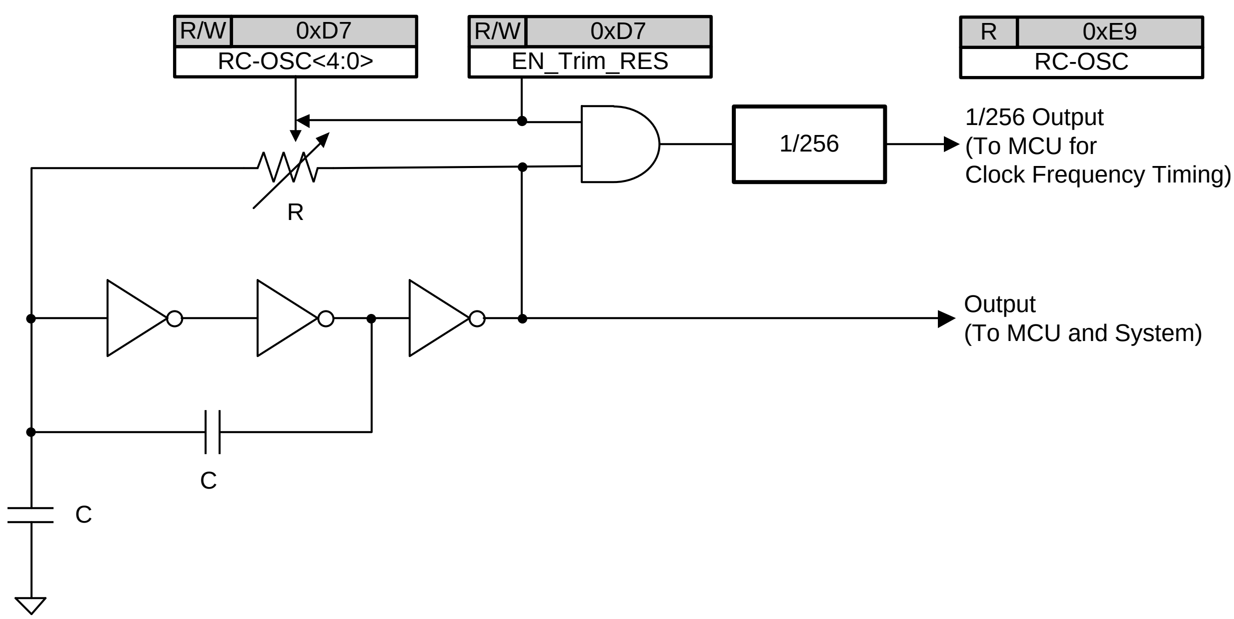
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RC-OSC	XTALosc			LFwakeCount	PostCount	PreCount	Timer-OSC
Access	r	r	–	–	r	r	r	r
At Power on reset	0	0	x	x	1	1	1	0
At Timer reset	0	0	x	x	D	D	D	D

RC-OSC	RC-OSC output monitor, RC-OSC output divided by 256 is monitored.	Refer to Section 3.4.3
XTALosc	XTALosc output monitor, Xtal-OSC output divided by 512 is monitored.	Refer to Section 3.4.4
LFwakeCount	Timer LFwake Counter output monitor	
PostCount	Timer Post-Counter output monitor	
PreCount	Timer Pre-Counter output monitor	
Timer-OSC	Timer-OSC output monitor	

3.4.3 RC Oscillator (RC-OSC)

The RC oscillator (RC-OSC) is used for generating an MCU clock of 2.4 MHz. Most of the operations use this clock because of the low current consumption and fast start up. The RC-OSC consists of a 3-stage ring oscillator and an RC low pass filter. A 5-bit variable resistor is used as a resistor of the low pass filter to control oscillation frequency of 9.6 MHz precisely. The 5-bit variable resistor can be controlled by using a register of RC-OSC<4:0> (0xD7:RC-OSC). The oscillation frequency can be monitored by using a register of RC-OSC (0xE9: TimerState). A register of EN_Trim_RES (0xD7:RC-OSC) is able to monitor the output of RC-OSC which is divided by 256 for the clock frequency tuning.

Since the oscillator has dependencies on the operation voltage and temperature, it is recommended to calibrate the oscillation frequency using the Xtal-OSC. The firmware is prepared to support this trimming function and can be called by the application software. For more details about the RC-OSC trimming, refer to the SW Application manual.



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- RC-OSC Not Bit Addressable

ESFR: 0xD7 RC-OSC

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	EN_XTALdiv	SEL_XTALdiv	EN_Trim_RES	RC-OSC<4:0>				
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
At Power on reset	0	0	0	0	1	1	1	0
At Timer reset	0	0	0	S	S	S	S	S

EN_XTALdiv	Enable the switch of the Xtal-OSC 1/32 and 1/16 divider: 0 = Divider Off 1 = Divider On (Enables both 1/32 and series connected 1/16 divider)	Refer to Section 3.4.4
SEL_XTALdiv	Select the Xtal-OSC output 1/2 divided or 1/32 divided: 0 = 1/2 divided (Default and Normal operation) 1 = 1/32 divided clock (Needs to be set with EN_XTALdiv=1)	Refer to Section 3.4.4
EN_Trim_RES	Enable RC-OSC trim: 0 = Disable RC-OSC Trim 1 = Enable RC-OSC Trim	
RC-OSC<4:0>	5-bit variable resister control: 1F = Maximum Resistance and generate Lowest Frequency 00 = Minimum Resistance and generate Fastest Frequency	

- Timer State / RC-OSC State Not Bit Addressable

ESFR: 0xE9 TimerState

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RC-OSC	XTALosc			LFwakeCount	PostCount	PreCount	Timer-OSC
Access	r	r	–	–	r	r	r	r
At Power on reset	0	0	x	x	1	1	1	0
At Timer reset	0	0	x	x	D	D	D	D

RC-OSC	RC-OSC output monitor, RC-OSC output divided by 256 is monitored.	
XTALosc	XTALosc output monitor, Xta Oscillator output divided by 512 is monitored.	Refer to Section 3.4.4
LFwakeCount	Timer LFwake Counter output monitor	Refer to Section 3.4.2.1
PostCount	Timer Post Counter output monitor	Refer to Section 3.4.2.1
PreCount	Timer Pre Counter output monitor	Refer to Section 3.4.2.1
Timer-OSC	Timer-OSC output monitor	Refer to Section 3.4.2.1

3.4.4 Crystal Oscillator

The crystal oscillator (Xtal-OSC) consists of the crystal driver, the clock dividers, and the selectors. A crystal with a resonant frequency around 19.7 MHz is required. Since the current consumption of the Xtal-OSC is larger than that of the RC-OSC, the Xtal-OSC is recommended only for use of the operations that require a precise clock such as RF transmitting and oscillator calibration (Timer-OSC, RC-OSC, and LF-OSC).

Bias current of the Xtal-OSC can be controlled by a register of XtalBIAS<3:0> (0x86) with a step of 20 µA. The state of the Xtal-OSC can be detected by monitoring a register of FLAG_XtalOSC (0xE3).

NOTE

Xtal frequency should be adjusted by the application, which may use a specific RF transmitting frequency. In this manual, the Tx frequency (433.920 MHz and 314.980 MHz) and other timing tuning adjustments are expected based on the crystal of 19.707894 MHz. If the Xtal frequency is changed, the Timer-OSC and RC-OSC trimming parameters must be tuned since they refer to the Xtal-OSC frequency.

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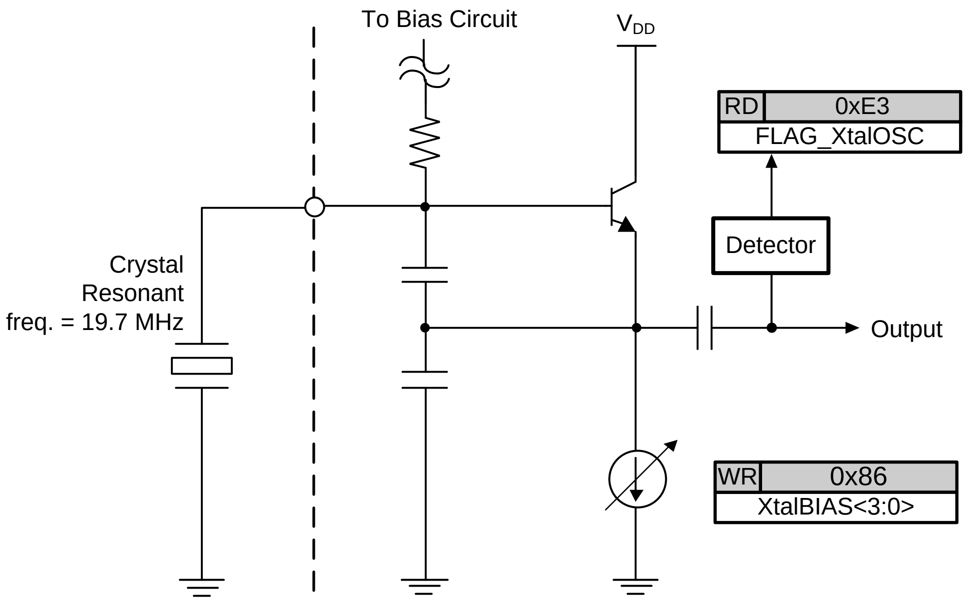

Figure 3-8. Crystal Oscillator Block Diagram

■ Xtal-OSC bias Control — Not Bit Addressable

ESFR: 0x86 — XtalBias

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	–	XtalBIAS< 3:0 >			
Access	–	–	–	–	w	w	w	W
At Power on reset	x	x	x	x	0	0	0	0
At Timer reset	x	x	x	x	0	0	0	0

XtalBIAS< 3:0> Bias current control of the Xtal-OSC

■ PLL local OSC State / RF trigger state — Not Bit Addressable

ESFR: 0xE3 — LocalState

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	FLAG_XtalOSC	VCOgain	FLAG_PLL LKD	Reserved	
Access	–	–	–	r	r	r	r	r
At Power on reset	x	x	x	0	0	0	0	0
At Timer reset	x	x	x	0	0	0	0	0

FLAG_XtalOSC Xtal-OSC: Oscillating (1), Not Oscillating (0)
VCOgain Higher (1), Lower(0)
FLAG_PLL_LKD Locked(1), Unlocked (0)

3.5 RF Transmitter

The RF transmitter offers 434 MHz and 315 MHz RF data transmission and consists of a Power Amplifier (PA) block, a PLL synthesizer block, and the baseband (BB) modulator block. External components such as the LC resonator load of PA, impedance matching circuit and antenna are required to complete the transmitter hardware. The external LC resonator components and the impedance matching circuit should be changed for 315 MHz and 434 MHz band operation, respectively.

- Key features of RF 315/434 MHz transmitter
  – RF 315/434 MHz dual band transmitter with one crystal oscillator
  – Variable transmit frequency around 315/434 MHz ± 700 kHz

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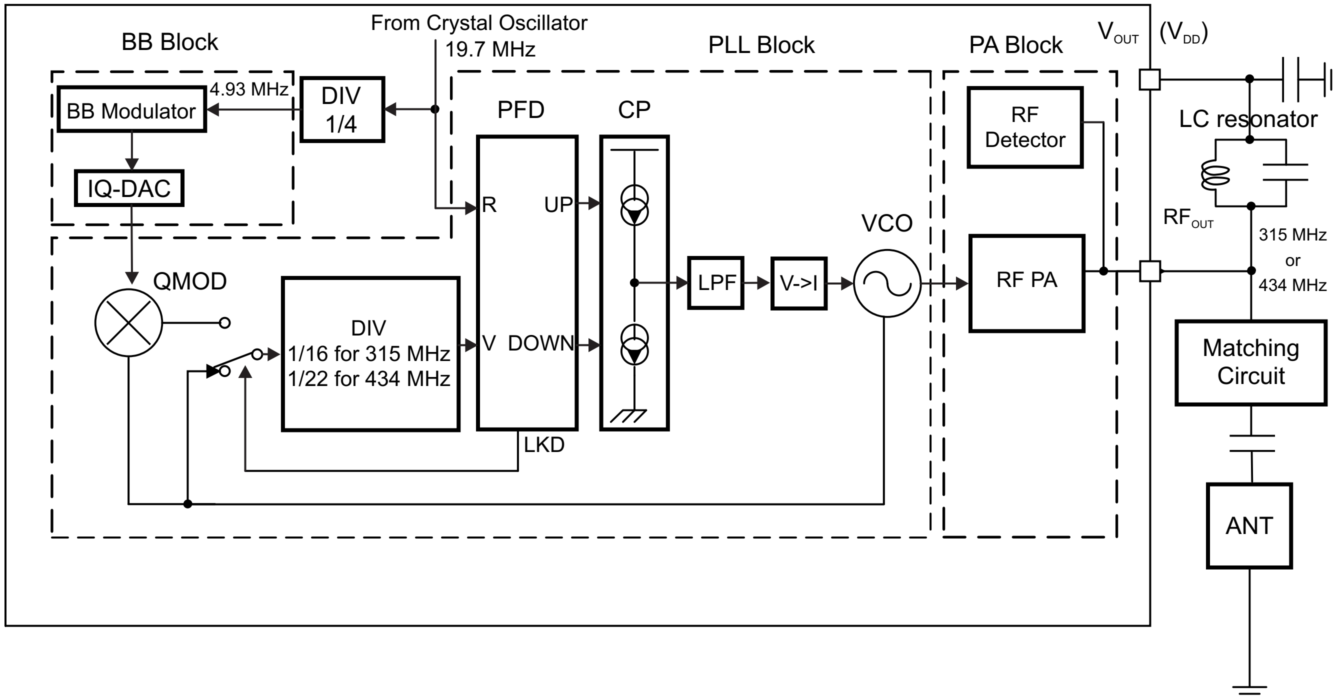

Figure 3-9. 315/434MHz Transmitter Block Diagram

3.5.1 RF Power Amplifier

The RF Power Amplifier amplifies the modulated output signal from the QMOD and drives the external antenna circuits. The LC resonator load, matching circuit, and an antenna are required externally to complete the transmitter circuits. RFpower at 0xF1: RFpower is used to turn the power supply (V_{DD}) on/off for the RF PA block. The output power can be set by register RFPAbias<7:0> at 0xF2: RFbias. PrePAbias<1:0> at 0xF1: RFpower controls the bias current of Pre-Amp for the 434 MHz and 315 MHz operation.

The RF output power can be adjusted in the OTP version while debugging. However, once the output power is fixed on the Mask ROM version, the output power is adjusted while in the TI final test. For more information about the output power adjustment, refer to the HW Application Note.

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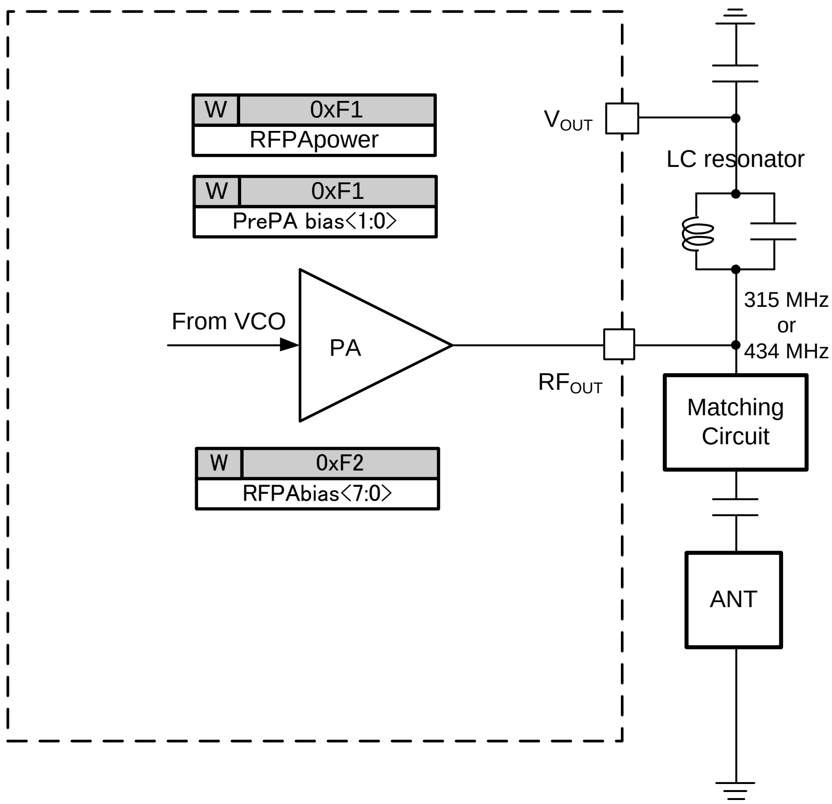

Figure 3-10. RF PA Block

- Tx RF-PA Control

Not Bit Addressable

ESFR: 0xF1 RFpower

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RFPApower	Reserved	PrePA bias<1>	Reserved				PrePA bias<0>
Access	W	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

RFPApower — RFPA Power:
1 = RFPA On
0 = RFPA Off

PrePA bias<1:0> — Current control of pre-PA stages:
(0, 0) = Lowest current, (0, 1) = Mid-low current
(1, 0) = Mid-high current, (1, 1) = Highest current

- Tx RF-PA bias

Not Bit Addressable

ESFR: 0xF2 RFbias

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RFPAbias<7:0>							
Access	W	w	w	w	w	w	w	W
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

RFPAbias<7:0> — RF-PA bias setting (Refer to HW Application Note for the relation between value and output Power).

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3.5.2 PLL Block

The PLL block consists of a Phase/Frequency Detector (PFD), a Charge Pump (CP), a Low Pass Filter (LPF), and a Voltage Controlled Oscillator (VCO). The PFD detects phase and frequency differences between the reference signal generated by the crystal oscillator and the 315 MHz or 434 MHz CCO signal divided by 16 or 22, respectively. The PFD output pulses drive two switched current sources of the CP to charge or discharge the capacitors of LPF. And the output voltage of the LPF controls the output frequency of the VCO.

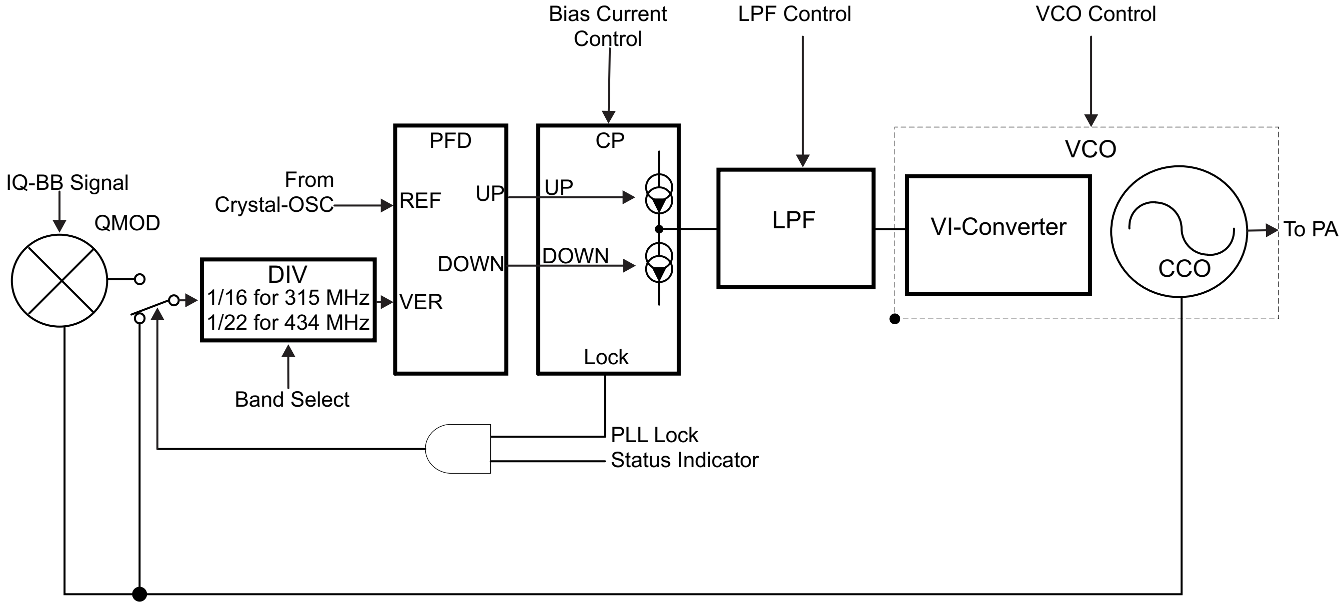
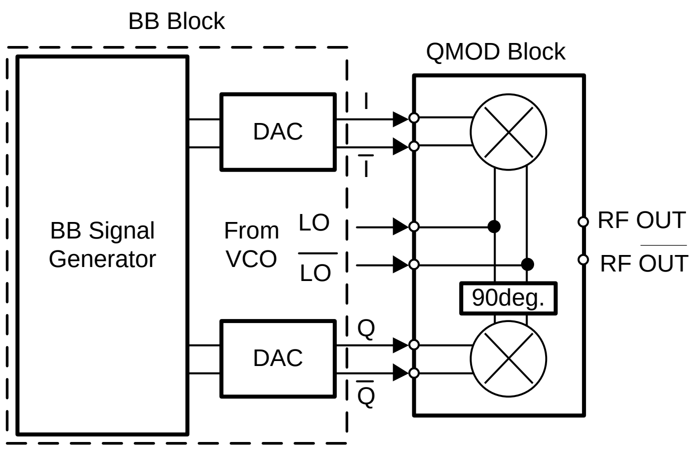


Figure 3-11. PLL Block

3.5.3 315/434MHz Dual-band Quadrature Modulator (QMOD)

The QMOD block consists of two double balanced mixers and a 315/434 MHz adjustable 90° phase-shifter. The 90° phase-shifter consists of an RC high/low pass filter. The capacitance of the LPF capacitor is configured using a MOS varactor to achieve a 90° phase shift for both 315 MHz and 434 MHz bands. The QMOD generates the desired differential RF signal by mixing the I/Q differential baseband signal and differential 315/434 MHz band local signal. In order to achieve low spurious performance, highly balanced 90° phase difference and equal amplitude of I/Q baseband and 315/434 MHz local signal are required. This QMOD can calibrate I/Q characteristics of the baseband and 315/434 MHz local signals, respectively.



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3.5.4 Baseband Block (BB block)

The BB block operates by synchronizing with 4.93 MHz double of the MCU system clock which is generated by the crystal oscillator (19.7MHz/ 4).

To activate baseband modulation, set the register bit (0xD3: EN_Modulation) to 1.

The 9-bit digital BB signal is generated using a 128-byte ROM data which stores sine and cosine waveforms for quarter period. The I and Q DACs convert this 9-bit digital BB signal to I and Q analog BB signals, respectively. The register, (0xD1: ModOffset<7:0>) controls BB signal frequency with Equation 1.

$$\text{BB Freq.(Hz)} = \frac{4 \times \text{ModOffset} < 7:0 > (\text{0xD1})}{4096} \times \text{BBclock(4.93MHz)}, \tag{1}$$

Where the BB clock is equal to the sampling clock and 4096 is the number of steps to count in one period.

From Equation 1, maximum and minimum BB frequencies are defined as 1227.7 kHz (at 0xD1: ModOffset<7:0> = 255) and 4.8 kHz (at 0xD1: ModOffset<7:0> = 1).

The FSK and ASK modulated signals can be generated using the data in the register (0xC9: ModRAMdata<7:0>) which stores the 64-byte Tx-RAM data based on the address the register (0xCA: ModRamAdd<5:0>) points to.

When using FSK modulation, the frequency deviation can be calculated with Equation 2.

$$\Delta\text{Freq. deviation of FSK(Hz)} = \frac{\text{ModRAMdata} < 7:0 > (\text{0xC9})}{4096} \times \text{BBclock(4.93MHz)}, \tag{2}$$

Where ModRAMData<7:0> (0xC9) is the data stored in the 64-byte RAM.

From Equation 2, the maximum and minimum frequency deviations of FSK modulation are defined as 306.9 kHz (at ModRAMdata<7:0> (0xC9) = 255) and 0.6 kHz (at ModRAMdata<7:0> (0xC9) = 1). The frequency deviation can be adjusted with 1.2 kHz steps.

For ASK modulation, register ModRAMdata<7:0> (0xC9) should be set as all the same value for constant BB frequency.

The bit rate is controlled by the registers (0xD2: ModScale<7:0>) and (0xCA: ModRamAdd<5:0>) with Equation 3.

$$\text{Bit rate (bps)} = \frac{1}{2} \times \frac{\text{BB clock(4.93MHz)}}{\text{ModScale} < 7:0 > (\text{0xD2})} \times \frac{1}{\text{ModRAMAdd} < 5:0 > (\text{0xCA})}, \tag{3}$$

Where ModRAMAdd<5:0> (0xCA) can set the number of addresses of 64-byte RAM for 1 bit, ModScale<7:0> (0xD2) can set the sampling speed of 64-byte RAM for 1 bit.

The FSK modulated signal frequency with BB signal can be described as the combination of BB frequency and frequency deviation using Equation 4.

$$\text{Modulated signal Freq.(Hz)} = \frac{\text{ModRAMData} < 7:0 > (\text{0xC9}) + 4 \times \text{ModOffset} < 7:0 > (\text{0xD1})}{4096} \times \text{BBclock} \tag{4}$$

The register bit (0xD3: Polarity) is assigned as a switch to change the BB signal phase between I and Q. This signal also defines whether to take the upper side or lower side frequency from the local carrier frequency (16x or 22x of Xtal-OSC frequency which is defined by register bit (0xC2: BAND)).

To select between FSK or ASK modes, set register (0xD3: Modulation mode). If this bit is set to 1, ASK mode is selected. FSK mode is selected if the bit is set to 0.

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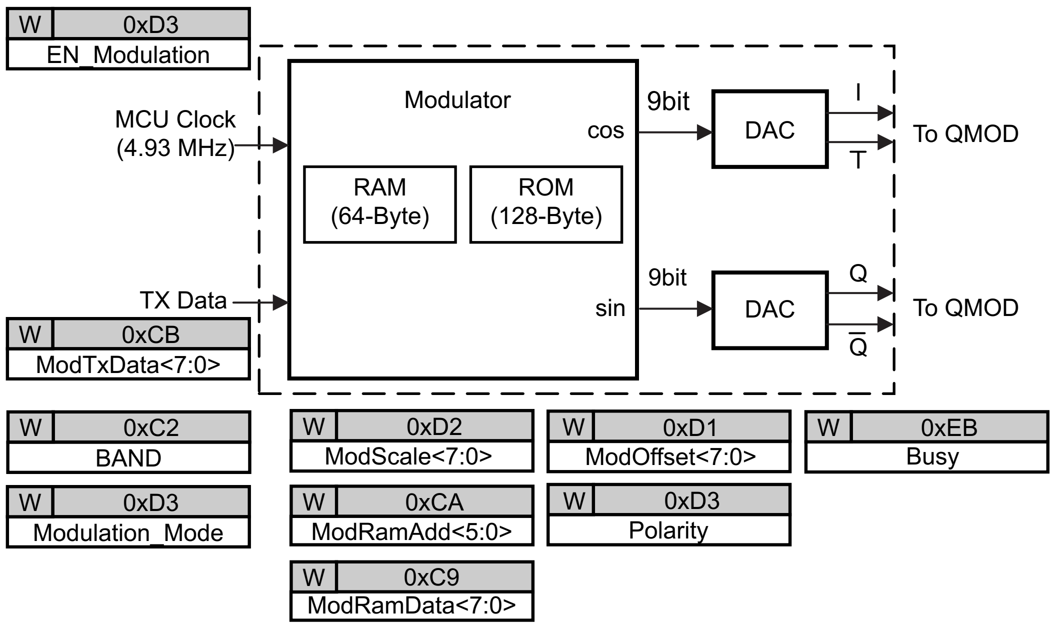

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- Setting Example
  - Xtal-OSC frequency: 19.707894 MHz
  - **Desired carrier frequency: 314.980 MHz**
    - ModRAMData<7:0> (0xC9) = 28, ModOffset<7:0> (0xD1) = 65

$$\text{Modulated signal Freq. (kHz)} = \frac{28 + 4 \times 65}{4096} \times \frac{19.707894\text{MHz}}{4} = 346.4\ \text{(kHz)}$$

$$\text{Carrier Freq. (MHz)} = 19.707894\text{MHz} \times 16 - 346.4\ \text{(kHz)} = 314.980\ \text{(MHz)}$$

Where Polarity (0xD3) = 1, select the lower side frequency from the local carrier frequency.
BAND (0xC2) = 1 (315 MHz).

  - **Desired carrier frequency: 433.920 MHz**
    - ModRAMData<7:0> (0xC9) = 28, ModOffset<7:0> (0xD1) = 65

$$\text{Modulated signal Freq. (kHz)} = \frac{28 + 4 \times 65}{4096} \times \frac{19.707894\text{MHz}}{4} = 346.4\ \text{(kHz)}$$

$$\text{Carrier Freq. (MHz)} = 19.707894\text{MHz} \times 22 - 346.4\ \text{(kHz)} = 433.920\ \text{(MHz)}$$

Where Polarity (0xD3) = 0, select the upper side Freq. from the Local Carrier Freq.
BAND (0xC2) = 0 (434 MHz).

  - **Frequency deviation of FSK: ±25 kHz**
    - ModRAMData<7:0> (0xC9) = 7, 28 (center), 49

$$\text{Freq. deviation of FSK (kHz)} = \frac{7}{4096} \times \frac{19.707894\text{MHz}}{4} = 8.42\ \text{(kHz)},\ \frac{28}{4096} \times \frac{19.707894\text{MHz}}{4} = 33.68\ \text{(kHz)},$$

$$\frac{49}{4096} \times \frac{19.707894\text{MHz}}{4} = 58.94\ \text{(kHz)}$$

  - **For bit rate: 4.8K bits/s** (ModScale<7:0> (0xD2) = 16, ModRAMAdd<5:0> (0xCA) = 32)

$$\text{Bit rate (bps)} = \frac{1}{2} \times \frac{19.707894\text{MHz}}{4} \times \frac{1}{16} \times \frac{1}{32} = 4.81\ \text{(kbps)}$$

  - **For bit rate: 9.6K bits/s** (ModScale<7:0> (0xD2) = 8, ModRAMAdd<5:0> (0xCA) = 32)

$$\text{Bit rate (bps)} = \frac{1}{2} \times \frac{19.707894\text{MHz}}{4} \times \frac{1}{8} \times \frac{1}{32} = 9.62\ \text{(kbps)}$$

  - **For bit rate: 19.2K bits/s** (ModScale<7:0> (0xD2) = 4, ModRAMAdd<5:0> (0xCA) = 32)

$$\text{Bit rate (bps)} = \frac{1}{2} \times \frac{19.707894\text{MHz}}{4} \times \frac{1}{4} \times \frac{1}{32} = 19.25\ \text{(kbps)}$$

  - **For bit rate: 10K bits/s** (ModScale<7:0> (0xD2) = 8, ModRAMAdd<5:0> (0xCA) = 31)

$$\text{Bit rate (bps)} = \frac{1}{2} \times \frac{19.707894\text{MHz}}{4} \times \frac{1}{8} \times \frac{1}{31} = 9.93\ \text{(kbps)}$$

  - **For bit rate: 20K bits/s** (ModScale<7:0> (0xD2) = 4, ModRAMAdd<5:0> (0xCA) = 31)

$$\text{Bit rate (bps)} = \frac{1}{2} \times \frac{19.707894\text{MHz}}{4} \times \frac{1}{4} \times \frac{1}{31} = 19.87\ \text{(kbps)}$$

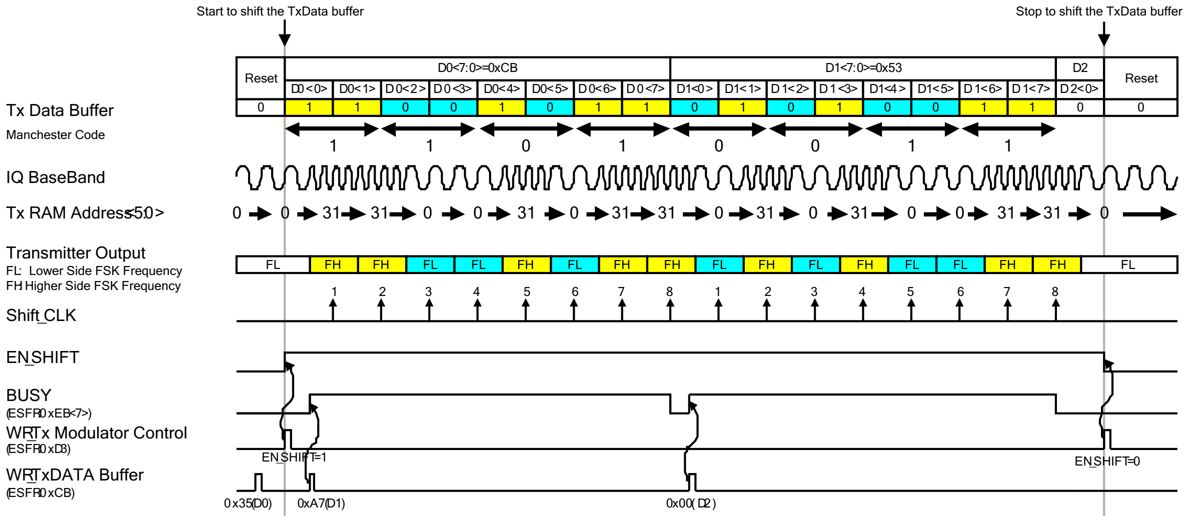

Figure 3-12. Timing Diagram of 1-Byte FSK Data Transmission

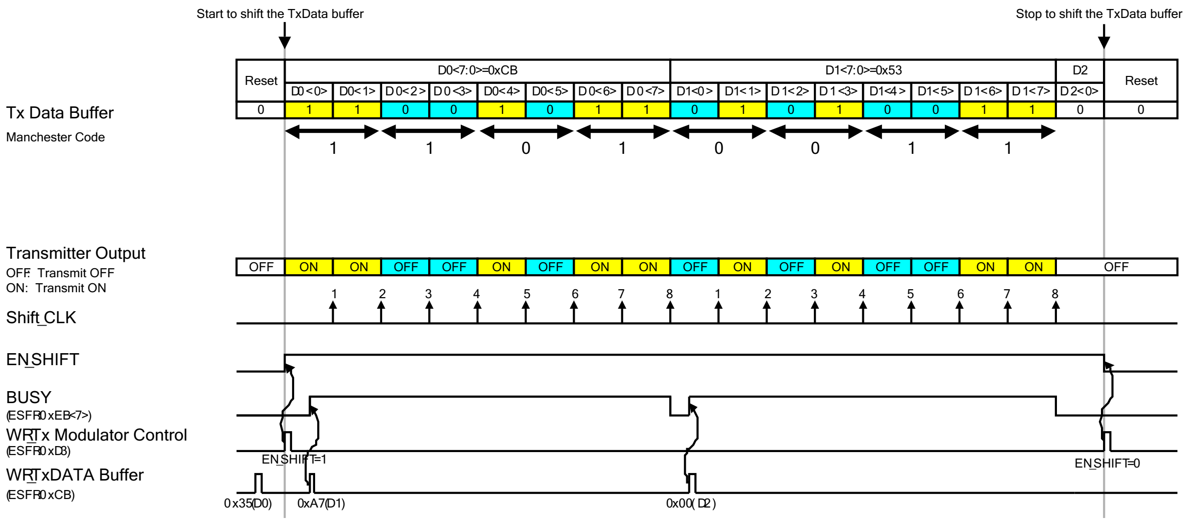

Figure 3-13. Timing Diagram of 1-Byte ASK Data Transmission

■ Tx DATA Buffer — Not Bit Addressable

ESFR: 0xCB — ModTxData

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ModTxData<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	U	U	U	U	U	U	U	U

ModTxData<7:0> Transmit Data Buffer

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- PLL Local OSC — Not Bit Addressable

ESFR: 0xC2 — PLLlocalOSC

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BAND	Reserved						
Access	w	w	w	w	w	w	w	w
At Power on reset	1	0	0	0	0	0	0	0
At Timer reset	1	0	0	0	0	0	0	0

BAND — VCO Frequency [dividing ratio] Selection:
0 = 434 MHz [1/22]
1 = 315 MHz [1/16]

- Tx Modulator Offset Frequency — Not Bit Addressable

ESFR: 0xD1 — ModOffset

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ModOffset<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	U	U	U	U	U	U	U	U

ModOffset<7:0> — BB Frequency setting parameter:
BB Freq. (Hz) = 4 * ModOffset<7:0> / 4096 * BB clock (4.93 MHz)

- Tx Modulator Scale — Not Bit Addressable

ESFR: 0xD2 — ModeScale

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ModScale<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	U	U	U	U	U	U	U	U

ModScale<7:0> — Sampling clock scaling factor of 64-byte TX-RAM
Bit rate (bps) = 1/2 * (BB clock (4.93 MHz) / (ModScale<7:0> * ModRAMAdd<5:0>))

- Tx Modulator Control — Not Bit Addressable

ESFR: 0xD3 — ModCONT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Reserved	–	Polarity	EN_Modulation	Modulation Mode	TxRAM Access	EN_SHIFT	Reserved
Access	w	–	w	w	w	w	w	w
At Power on reset	0	x	0	0	0	0	0	0
At Timer reset	0	x	0	0	0	0	0	0

Polarity — I/Q phase switch:
0 = Positive and select upper side freq. from local carrier freq.
1 = Negative and select lower side freq. from local carrier freq.

EN_Modulation — Modulation Active control
1 = Activate, 0 = Inactivate

Modulation_Mode — ASK/FSK modulation mode selector:
1 = ASK modulation, 0 = FSK modulation

TxRAM Access — TX RAM Access Mode Control
1 = TX R/W Access, 0 = Normal Modulation Mode

EN_SHIFT — Enable shift of 8bit Tx Data Buffer
1 = Enable the Shift, 0 = Disable the Shift

- Tx Modulator state — Not Bit Addressable

ESFR: 0xEB — ModState

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BUSY	Reserved	–	–	–	–	–	–
Access	r	r	–	–	–	–	–	–
At Power on reset	U	1	x	x	x	x	x	x
At Timer reset	U	1	x	x	x	x	x	x

BUSY — BUSY Flag of Tx Data Buffer:
1 = Busy
0 = Ready to load next Tx-data

- IQ BaseBand Tx RAM Data — Not Bit Addressable

ESFR: 0xC9 — ModRamData

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ModRamData<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	U	U	U	U	U	U	U	U

ModRamData<7:0> — 64-byte TX-RAM data setting — activate with TxRAM Access = 1 (ESFR: 0xD3)

- IQ BaseBand Tx RAM Address — Not Bit Addressable

ESFR: 0xCA — ModRamAdd

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	ModRamAdd<5:0>					
Access	–	–	w	w	w	w	w	w
At Power on reset	x	x	U	U	U	U	U	U
At Timer reset	x	x	U	U	U	U	U	U

ModRamAdd<5:0> — 64-byte TX-RAM address setting — activate with TxRAM Access = 1 (ESFR: 0xD3)

3.6 LF Receiver

An LF receiver is implemented on the device to trigger the wake-up of the device or to control the operation of the device externally. The LF receiver consists of an Analog Front-End (AFE) and a baseband processor block. External LF antenna circuits are required to complete the receiver system.

The LF receiver on the device can detect ASK modulated 125 kHz LF signals. To minimize the power dissipation of the device, this LF receiver wakes up periodically as defined by the (0xC4: TLFwake<7:0>) register in the interval timer block. The device can recognize four types of pre-fixed protocols (three Manchester coded patterns and one PWM coded pattern) without waking up the MCU.

3.6.1 LF AFE

The LF AFE consists of a variable capacitor and resistor (attenuator) for LF antenna Q tuning and LF signal gain control, Receiving Signal Strength Indicator (RSSI), data slicer for ASK signal demodulating, signal level detector, LF-OSC (300 kHz typically), and bias and timing control blocks. Each parameter such as RSSI gain, antenna tuning parameters, and the data slicer threshold, can be programmed via the appropriate registers.

NOTE

The variable capacitor and resistor (attenuator) are set to a default values and can be neglected as isolated from the LF input.

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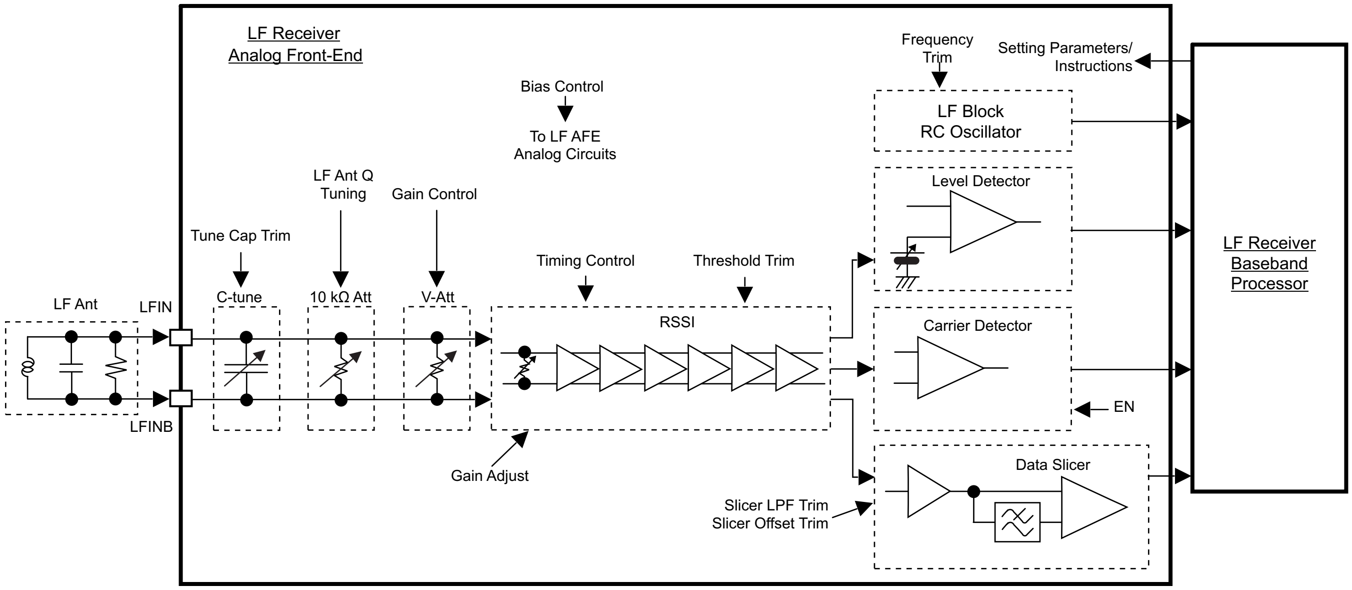
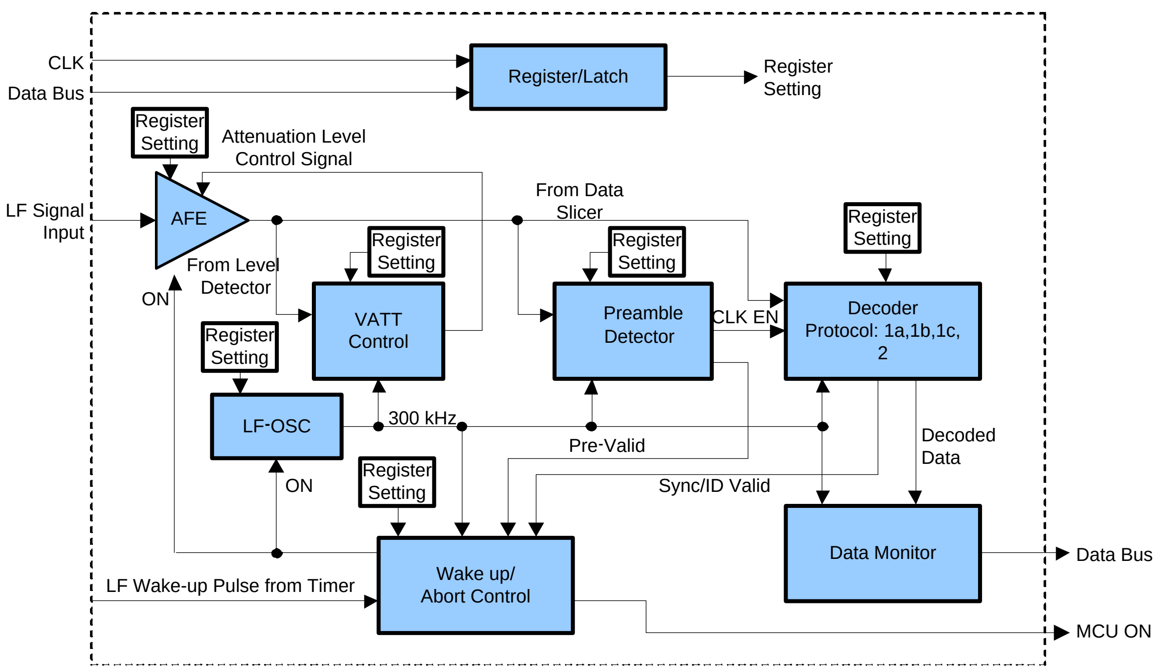


3.6.2 LF Baseband Processor

The LF baseband processor decodes the demodulated signal from the LF AFE and determines if the input pattern matches the ID, pattern, or commands from the remote controller. The device supports four types of LF patterns (three Manchester coded and one PWM coded). Once one of the basic protocols (1a,1b,1c, or 2) is programmed on the device, then the customer can define their own synchronization pattern, Wake-up ID, and MCU start program via the corresponding registers.



3.6.3 LF Pattern

The TPIC82000 device recognizes four types of LF patterns. Three of these LF patterns are Manchester coded patterns and one is a PWM coded pattern.

The user can select the LF protocol by setting the register (0xA4: LFprotocol<1:0>) in the application program. To ensure LF detection while minimizing the power dissipation of the device, the LF sniffing timing needs to be carefully considered. The user also can define the MCU wake-up timing after the corresponding synchronization pattern detection. This can be set by the register (0xA4: WakeupTiming<1:0>).

The following sections show the examples of different LF patterns and associated sniffing timings.

WakeupTiming<1>	WakeupTiming<0>	Operation mode
0	0	Not used (Not start)
0	1	MCU start after Sync pattern matching
1	0	MCU start after Wakeup_ID pattern matching
1	1	MCU start after the first Data pattern matching

LFprotocol<1>	LFprotocol<0>	Operation mode
0	0	Protocol pattern 2
0	1	Protocol pattern 1a
1	0	Protocol pattern 1b
1	1	Protocol pattern 1c

3.6.3.1 Protocol 1a

In Protocol 1a, the transmitted data frame consists of the preamble, synchronization pattern, Wake-up ID and command/data periods. The data frame begins with a pre-defined duration of the preamble pattern which indicates the data period ($1T_{BIT}$) with periodical On-Off LF signals, then the synchronization pattern which consists of 9 T_{BIT} length data is transmitted. Next, the Wake-up ID pattern consisting of 16 T_{BIT} length data is sent, and then the command or data consisting of 8 T_{BIT} x N length data should be transferred to the device. The Protocol 1a and the LF sniff example timing diagrams are shown in Figure 3-14 and Figure 3-15.

The device checks if the LF preamble signal exists or not by waking up the LF AFE and baseband block every period as defined by the LF timer setting. If no LF signals are detected while in $T_{SNIFF\text{-}ON}$ period, the device goes back into sleep mode and wakes up again at the next sniffing period. If LF signals are detected while in $T_{SNIFF\text{-}ON}$ period, the device continues to check if the LF patterns match with the synchronization pattern, Wake-up ID patterns, and/or first data pattern. When matching patterns are recognized, the device wakes up the MCU and the MCU starts the remaining data receiving process. The timing of the MCU wake-up can be selected by application software as after the preamble, the synchronization pattern, the Wake-up ID or the first data depending on user preference.

To ensure the detection of the LF patterns without fail even when one shot LF frame is applied, it is recommended to set the LF sniffing period to be shorter than the preamble period and the Sniffing-On duration ($T_{SNIFF\text{-}ON}$) to be longer than $T_{BIT}/2$. To minimize the power consumption in the LF signal detection, it is recommended to minimize the duty cycle of the sniff-on period. Even though, the device is designed so it is able to detect only 1 shot of the LF frame, it is recommended to repeat the entire LF frame a few times to ensure the communication.

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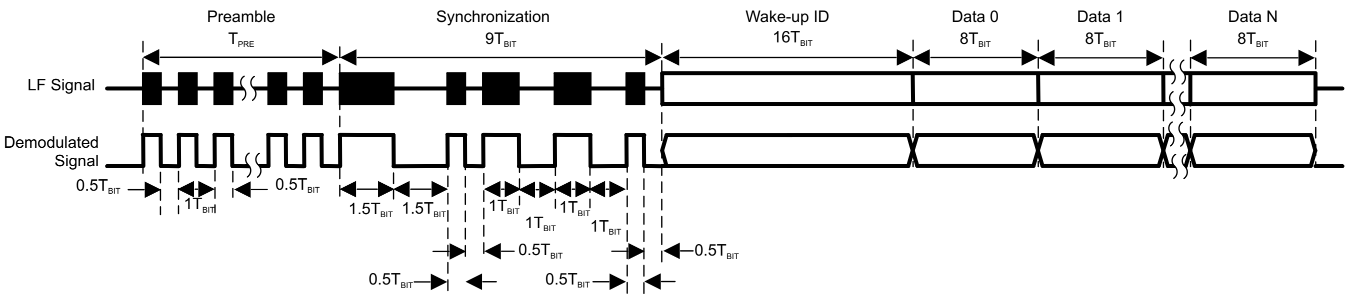

Figure 3-14. LF Protocol 1a Pattern Example

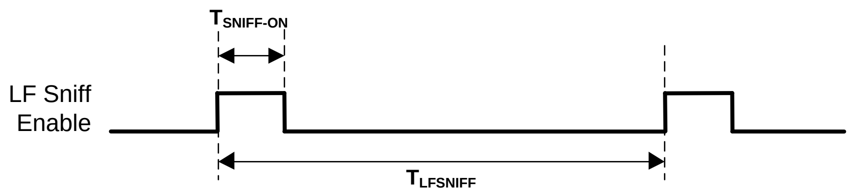

Figure 3-15. LF Sniffing Timing

Table 3-3. Protocol 1a (Manchester Coding) Timing Example

Symbol	Description	Timing Example
T_{PRE}	Preamble duration	4 mS (typical) (greater than 3mS)
T_{BIT}	Duration for 1bit	256 µS (typical)
f_{LF}	LF Carrier frequency	125 kHz (typical)
DR_{LF}	LF Data rate	3.906K bits/s (typical)
$T_{SNIFF-ON}$	LF Sniffing Period	300 µS (typical) (programmable) (1)
$T_{LFSNIFF}$	LF Sniffing Interval	2.2 mS (typical) (programmable) (2)

(1) The LF sniffing period is determined as the combination of the LF AMP set up time (typically 150 µS) and LF carrier detect time which is programmable in 16 steps with every 26.4 µS.
TSNIFF-ON = LF AMP Set Up Time + LF Carrier Detect Time
= 150 µs + (1+ LFcarrierDET<3:0>) * 8/F_LF-OSC, where F_LF-OSC is the frequency of LF-OSC.

(2) To change the LF sniffing interval, the Timer-OSC frequency needs to be trimmed. The specification of the trimmed Timer-OSC frequency is 400–500 Hz. (See Section 5.5) Set the register bits, TimerOSC<3:0> and TimerOSC_DIV<2:0>, in the TimerOSC register (0x97) to the appropriate value to achieve the fine adjusted sniffing interval. If any other blocks are using the Timer-OSC, the user needs to carefully confirm it won't affect any of these other functions.

3.6.3.2 Protocol 1b

Protocol 1b does not have the preamble signals from Protocol 1a but will repeat whole frames several times to ensure the signals and ID are detected. The transmission data frame consists of the synchronization pattern which consists of 9 T_{BIT} length data, Wake-up ID pattern which consists of 16 T_{BIT} length data and command or transmitting data consisting of 8 T_{BIT} x N length data. The Protocol 1b and the LF sniff example timing diagrams are shown in Figure 3-16 and Figure 3-17.

The device checks if the LF signal exists or not by waking up the LF AFE and the baseband block every period as defined by the LF timer setting. If no LF signals are detected while in $T_{SNIFF-ON}$ period, the device goes back into sleep mode and wakes up again at the next sniffing period. If the LF signals are detected while in $T_{SNIFF-ON}$ period, the device checks if the continuous five half-T_{BIT} pattern or T_{BIT} pattern is existing or not. If it detects the five consecutive patterns (five consecutive H and L changes of LF pattern), the device assumes it is the preamble signal and then determines the T_{BIT} width with the following two T_{BIT} signal (H–L or L–H pattern of LF signal). Then the device checks the synchronization pattern, Wake-up ID patterns, and/or first data pattern. When matching patterns are recognized, the device wakes up the MCU and the MCU starts the remaining data receiving process. The timing of the MCU wake-up can be selected by application software as after the preamble, the synchronization pattern, the Wake-up ID or the first data depending on user preference.

Due to the lack of the preamble pattern, the device may need the sniff-on duration to be at least one whole frame length to ensure the detection of the LF pattern without fail. Also, to minimize the power consumption in LF signal detection, it is recommended to send more than 10 times whole frames to reduce the duty of sniff-on period.

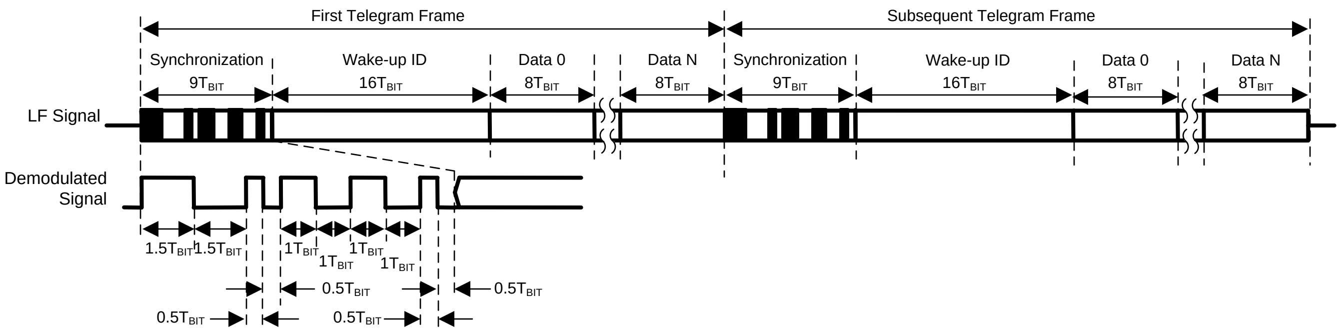

Figure 3-16. Protocol 1b Pattern Example

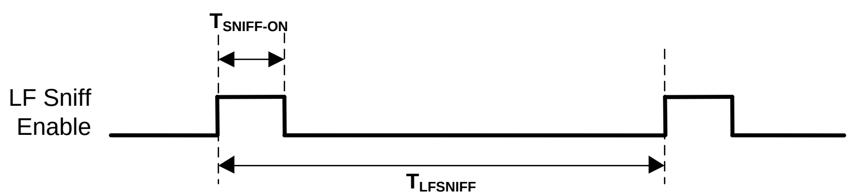

Figure 3-17. LF Sniffing Timing

Table 3-4. Protocol 1b (Manchester Coding) Timing Example

Symbol	Description	Timing Example
T_{BIT}	Duration for 1bit	256 µS (typical)
f_{LF}	LF Carrier frequency	125 kHz (typical)
DR_{LF}	LF Data rate	3.906K bits/s (typical)
Nframe	Data Frame repeat	> 3 (recommended more than 10)
$T_{SNIFF-ON}$	LF Sniffing Period	PREAMBLEabort<2:0> * 128 * 4/F_LF-OSC (programmable) (1) where F_LF-OSC is the frequency of LF-OSC
$T_{LFSNIFF}$	LF Sniffing Interval	< (Nframe-1)*Tframe – $T_{SNIFF-ON}$ (programmable) (2)

(1) The device can set the sniff-on duration in 7 steps with 1.7 mS intervals by setting the PREAMBLEabort<2:0> bit in the LFabort register (0xDC).
Tframe: Time period of one Telegram Frame [Synchronizing pattern + Wake-up ID + Data0+ … +Data N].
Nframe = N (The repeated LF frame number) * Tframe

(2) To change LF sniffing interval, set the TLFwake<7:0> in TimerLFwake register (0xC4) to the appropriate value. Since the LF sniffing interval is much longer than Timer-OSC frequency (typically 450 Hz), there is no need to preadjust the register bits, TimerOSC<3:0> and TimerOSC_DIV<2:0>, in the TimerOSC register (0x97).

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3.6.3.3 Protocol 1c

Protocol 1c is similar to that of Protocol 1a but there is a leading start marker (burst signal) before the preamble pattern. After the certain duration of the start mark, the preamble pattern which indicates the data period ($1T_{BIT}$) with periodical On-Off LF signals is sent, then the synchronization pattern which consists of 9 T_{BIT} length data is transmitted. Next, the Wake-up ID pattern consisting of 16 T_{BIT} length data is sent and then the command or transmitting data which consists of 8 T_{BIT} x N length data should be transferred to the device. The Protocol 1c and the LF sniff example timing diagrams are shown in Figure 3-18 and Figure 3-19.

The device checks if the LF signal is existing or not by waking up the LF AFE and baseband block in every certain period. If no LF signal is detected while in $T_{SNIFF-ON}$ period, the device goes into sleep and wakes up again at the next sniffing period. If LF signal is detected while in $T_{SNIFF-ON}$ period, the device continues to check if the continuous five half-T_{BIT} pattern is existing or not. If it detects the five consecutive half-T_{BIT} pattern (five consecutive H and L changes of LF pattern with same pulse width), the device assumes it is the preamble signal and determines the T_{BIT} width with the following two half T_{BIT} signal (H–L or L–H pattern of LF signal). Then, the device checks synchronization pattern, Wake-up ID patterns and/or first data pattern. When the matching patterns are recognized, the device wakes up the MCU and the MCU starts the remaining data receiving. The timing of the MCU wake-up can be selected by the application software as after the preamble, the synchronization pattern, the Wake-up ID or the first data depending on user preference.

Even though the device is designed to be able to detect only 1 shot of the LF frame, it is recommended to repeat the entire LF frame a few times to ensure the communication.

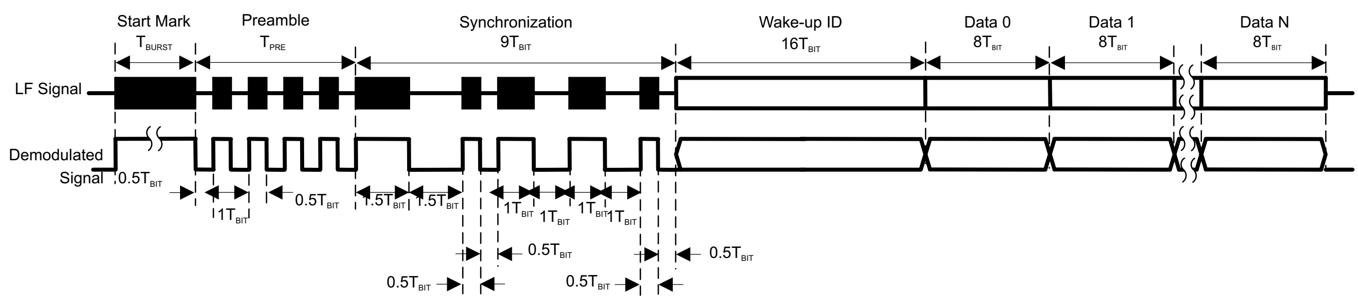

Figure 3-18. Protocol 1c Pattern Example

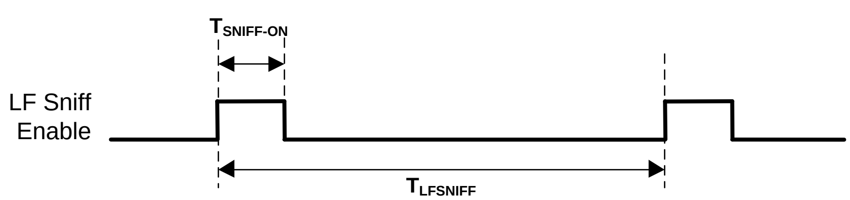

Figure 3-19. LF Sniffing Timing

Table 3-5. Protocol 1c (Manchester Coding) Timing Example

Symbol	Description	Timing Example
T_{BURST}	Start Mark (Burst) signal width	> 3 mS
T_{PRE}	Preamble duration	> T_{BIT} * 5
T_{BIT}	Duration for 1bit	256 µS (typical)
f_{LF}	LF Carrier frequency	125 kHz (typical)
DR_{LF}	LF Data rate	3.906K bits/s (typical)
$T_{SNIFF-ON}$	LF Sniffing Period	150 µS (Programmable) (1)
$T_{LFSNIFF}$	LF Sniffing Interval	2.2 mS < (T_{BURST}–$T_{SNIFF-ON}$) (Programmable) (2)

(1) Minimum LF sniffing period is determined as the LF AMP set up time (typically 150 µS).
(2) To change LF sniffing interval, the Timer-OSC frequency needs to be trimmed. The specification of the trimmed Timer-OSC frequency is 400–500 Hz. (See Section 5.5) Set the register bits, TimerOSC<3:0> and TimerOSC_DIV<2:0>, in the TimerOSC register (0x97) to the appropriate value to achieve the fine adjusted sniffing interval. If any other blocks are using the Timer-OSC, the user needs to carefully confirm it will not affect any of these other functions.

3.6.3.4 Protocol 1 Total Sniffing Abort Time

To prevent the continuous LF sniff-on situation, the device has the ability to set a total time limit for the LF sniffing. It can be defined by setting the register bits, LFabort<7:3>, in the LFabort register (0xDC). The time limit can be adjusted using 31 steps with a 6.8 mS interval.

3.6.3.5 Protocol 1 Data Pattern Setting

Synchronization Pattern:
The device can compare up to 17x0.5T_{BIT} synchronization pattern. Since the synchronization pattern may have a special pulse pattern which should not occur in normal Manchester coded communication, the device enables defining the matching pattern with each 0.5T_{BIT}. This can be achieved by setting the SYNC<7:0> and SYNC<14:8> register bits in the LFsync0 (0xAD) and LFsync1 (0xAE) registers. An example of the synchronization pattern is shown in Figure 3-20.

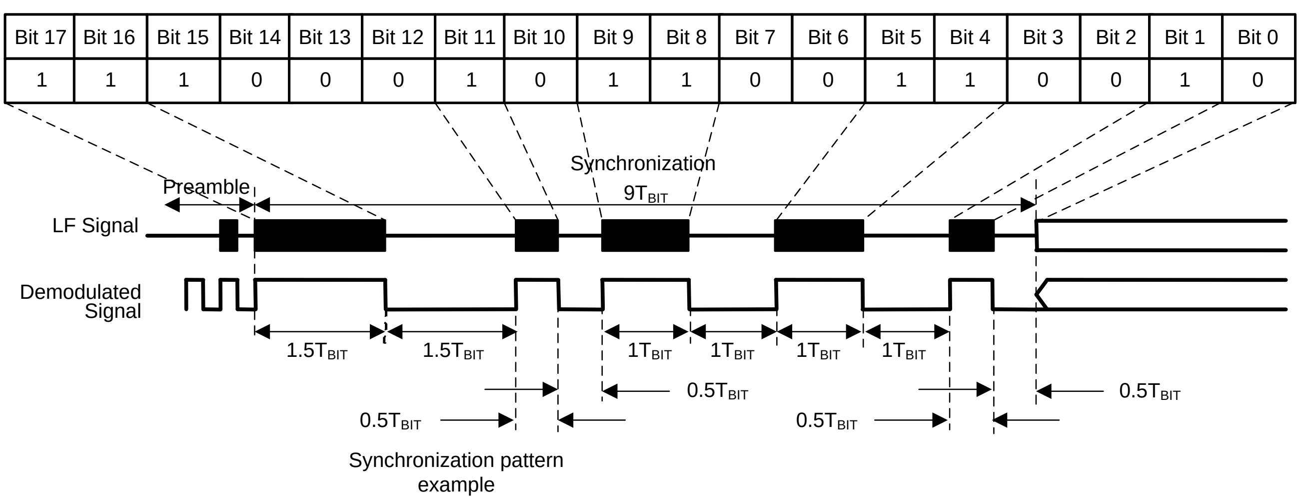

Figure 3-20. Synchronization Pattern Example

Wake-up ID:
The device can recognize up to a 16-bit length Wake-up ID. The matching pattern can be defined for each 1-bit (1 T_{BIT}) by setting the WAKE0<7:0> and WAKE0<15:8> register bits in the LFwake0L (0xAF) and LFwake0H (0xB1) registers, respectively. An example of the Wake-up ID is shown in Figure 3-21.

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Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	0	1	1	0	0	1	1	1	0	1	0	1	0

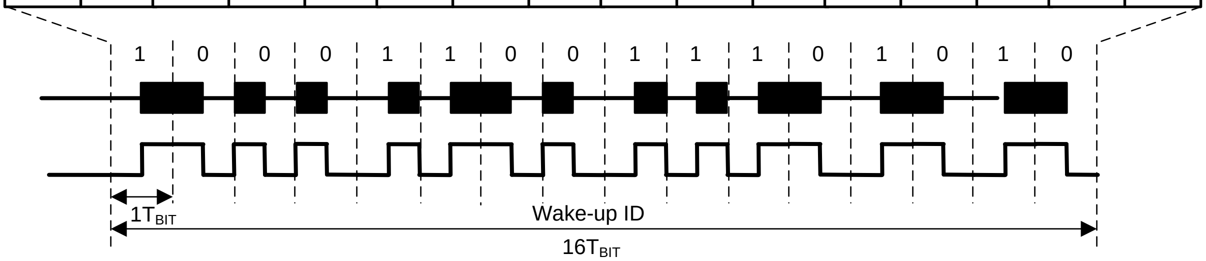

Figure 3-21. Wake-up ID Pattern Example

Command Data:

The device can define the first 8-bit or 16-bit length data as either a command data, normal transmitting data, or a part of the initial Wake-up ID/command. The matching pattern for this data portion can be defined for each 1-bit (1 T_{BIT}) by setting the bits WAKE1<7:0> in LFwake1L (0xCC) and WAKE1<15:8> in LFwake1H (0xCD).

3.6.3.6 Protocol 2

Protocol 2 supports PWM coded data streams. The data frame consists of the wake-up signal (burst signal), pause and preamble periods, and data periods.

Once the device detects the LF signal while in the sniff-on (T_{SNIFF}) period, the device wakes up the MCU. After the MCU start-up, all decisions for unit pulse width and data decoding is determined by the MCU and application programs.

The application program needs to determine the data unit pulse width (T_{UNIT}) from the pause and preamble period. Then it must decide the data code (1 or 0) by comparing the data pulse length with the unit pulse width. If the data pulse width is longer than T_{UNIT}, the device recognizes it as 1. If the data pulse length is shorter than T_{UNIT}, the device recognizes it as 0. Each data needs to be separated with a pause period. Figure 3-22 and Figure 3-23 show the Protocol 2 and the LF sniff example timing diagrams.

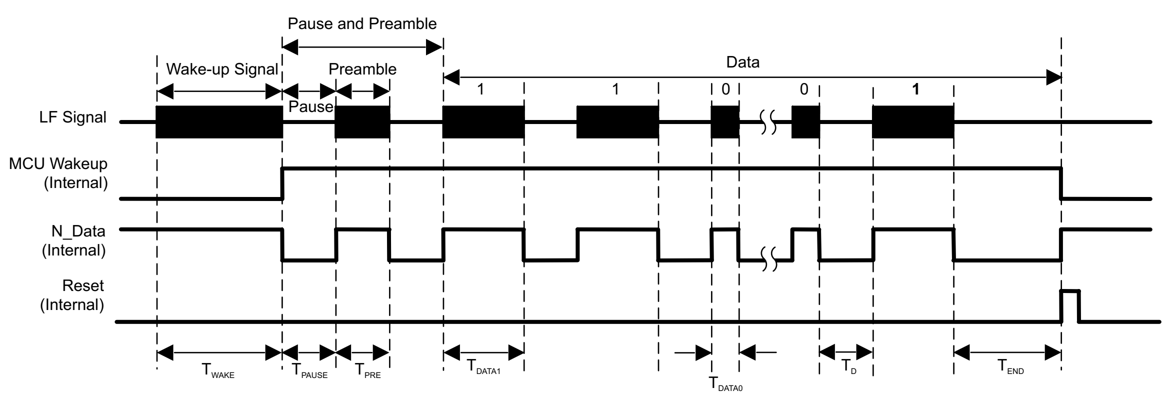

Figure 3-22. Protocol 2 Example

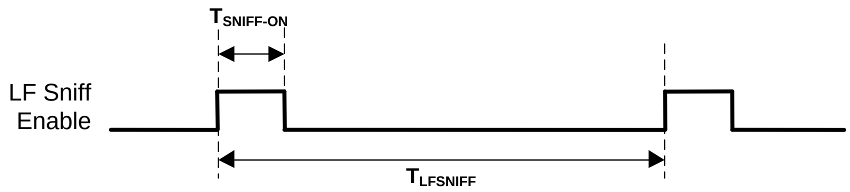

Figure 3-23. LF Sniffing Timing

Table 3-6. Protocol 2 (PWM) Timing Example

Symbol	Description	Timing Example
T_{WAKE}	Wake up time (include LF detection and AGC)	> 5 mS
T_{PAUSE} (1)	LF Pause	1 mS ±25%
T_{PRE} (1)	Preamble Signal (Decision time reference for data demodulation)	1mS ±25%
T_{DATA1} (1)	LF Presence (LF Data duration for data 1)	1.5 mS ±25% ($T_{DATA1} > T_{PRE}$)
T_{DATA0} (1)	LF Presence (LF Data duration for data 0)	0.5 mS ±25% ($T_{DATA0} < T_{PRE}$)
f_{LF}	LF Carrier frequency	125 kHz (typical) (119 kHz–131 kHz)
DR_{LF}	LF Data rate	0.5K bits/s (typical)
T_{END}	Time out for end transmission detection	> 3x T_{PRE}
$T_{SNIFF-ON}$	LF Sniffing Period	150 µS (programmable) (2)
$T_{LFSINFF}$	LF Sniffing Interval	2.2 mS < (T_{WAKE}–$T_{SNIFF-ON}$) (programmable) (3)

(1) Each timing variation of **T_{PAUSE}, T_{PRE}, T_{DATA1}, T_{DATA0}** has the same polarity and value of the variation. For example, if **T_{PAUSE}** has +25% variation, the others also have the +25% variation.
(2) Minimum LF sniffing period is determined as the LF Amp set up time (typically 150 µS).
(3) To change LF sniffing interval, Timer-OSC frequency needs to be trimmed. Set the register bits, TimerOSC<3:0> and TimerOSC_DIV<2:0>, in the Timer-OSC register (0x97) to the appropriate value to achieve the fine adjusted sniffing interval. If any other blocks are using the Timer-OSC, the user needs to carefully confirm it won't affect any of these other functions.

- LF ANT Tuning CAP Value — Not Bit Addressable

ESFR: 0xB2 — LFANT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LF_Test<1:0>		LFANT<5:0>					
Access	w	w	w	w	w	w	W	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LF_Test<1:0> — LF test monitor selector

LFANT<5:0> — LF antenna tuning capacitor setting — Can be updated with LFmode<6> = 1

LF_Test< 1 >	LF_Test< 0 >	Operation mode
0	0	Test mode Disabled
0	1	Test Monitor of LF sampling clock monitor (RC-OSC 300 kHz)
1	0	Test Monitor of LF ASK carrier
1	1	Test Monitor of LF RSSI ASK discriminator Output

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■ LF AGC Control — Not Bit Addressable

ESFR: 0xC6 LFagcSET

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	AGCenable	–	agcSET<3:0>			
Access	–	–	r/w	–	r/w	r/w	r/w	r/w
At Power on reset for r/w	x	x	0/U	–	0/U	0/U	0/U	0/U
At Timer reset for r/w	x	x	D/S	–	D/S	D/S	D/S	D/S
At Reset	–	–	0	–	0	0	0	0

AGCenable — LF input variable attenuator setting: ON (1), OFF (0)

agcSET<3:0> — LF input variable attenuator setting
agcSET<3:0> = 0x0 → Open (highest gain)
agcSET<3:0> = 0xF → Short (lowest gain)

■ LF Mode Control — Not Bit Addressable

ESFR: 0xA4 LFmode

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LFload	LDregister	Purge&AMPpower	LF_AMPpower	WakeupTiming<1:0>		LFprotocol<1:0>	
Access	w	w	w	w	w	w	W	w
At Power on reset	0	U	U	U	U	U	U	U
At Timer reset	0	S	S	S	S	S	S	S

LFload — LDregister setting: enable (1), disable (0)

LDregister — LF register setting: enable (1), disable (0). Can be updated with LFload = 1.
Load signal for LFANT, LFbias, LFdelay, LFpLT, LFpUT, LFsync0, LFsync1, LFwake0L, LFwake0H, LFwake1L, LFwake1H, SLoffset, LFcont, LFOSC
1: For LF trim (except for slicer dc-offset trim)
0: For slicer dc-offset trim

Purge&AMPpower — LF detector register purge and Disable AMP power. Can be updated with bit7(LFload) = 1.

LF_AMPpower — LF AMP power control: Continuously ON (1) TimerInterval ON (0). Can be updated with bit7(LFload) = 1.

WakeupTiming<1:0> — MCU Wake up timing select. Can be updated with bit7(LFload) = 1.

LFprotocol<1:0> — LF Rx Protocol select. Can be updated with bit7(LFload) = 1.

WakeupTiming<1>	WakeupTiming<0>	Operation mode
0	0	Not used (Not start)
0	1	MCU start after Sync pattern matching
1	0	MCU start after Wakeup_ID pattern matching
1	1	MCU start after the first Data pattern matching

LFprotocol<1>	LFprotocol<0>	Operation mode
0	0	Protocol pattern 2
0	1	Protocol pattern 1a
1	0	Protocol pattern 1b
1	1	Protocol pattern 1c

- LF Bias Trim Control — Not Bit Addressable

ESFR: 0xA5 — LFbias

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LF_RSSIdisc<2:0>			LFBIAS<4:0>				
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LF_RSSIdisc<2:0>	LF slicer LPF trim	Can be updated with LFmode<6> = 1
LFBIAS<4:0>	LF AFE bias control	Can be updated with LFmode<6> = 1

- LF AMP Setup Delay timer Trim — Not Bit Addressable

ESFR: 0xA6 — LFdelay

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LFdelay<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LFdelay<7:6>	Delay Timer Value Trim: A	Can be updated with LFmode<6> = 1
LFdelay<5:0>	Delay Timer Value Trim: B	Can be updated with LFmode<6> = 1

- LF-OSC (300 kHz) — Not Bit Addressable

ESFR: 0xA7 — LFOSC

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LFOSC<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LFOSC<7:0>	Bias current setting of the LF-OSC to Trim	Can be updated with LFmode<6> = 1

- LF AMP RSSI Threshold voltage setting — Not Bit Addressable

ESFR: 0xAA — LFrssiVT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LFrssiVT<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LFrssiVT<7:0>	RSSI Threshold Voltage Setting	Can be updated with LFmode<6> = 1

- Slicer Offset Trim Setting 0 to 4 — Not Bit Addressable

ESFR: 0xED — SLoffset

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	SLoffset<4:0>				
Access	–	–	–	w	w	w	w	w
At Power on reset	x	x	x	U	U	U	U	U
At Timer reset	x	x	x	S	S	S	S	S

SLoffset<4:0>	Slicer offset trim setting	Can be updated with LFmode<6> = 1

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■ LF Control — Not Bit Addressable

ESFR: 0xEC — LFcont

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	VATT<3:0>				Slicer_shunt	Carrier AMP on	VT monitor	Bias monitor
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

VATT <3:0>	10 kΩ shunt resistor between LFIN and LFINB trimming 0.5 kΩ step, 6 kΩ at VATT<3:0> = 1111, Open at VATT<3:0> = 0000	Can be updated with LFmode<6> = 1
Slicer_shunt	Slicer input shunt switch for dc-offset trimming ON (1): Slicer dc-offset trimming OFF (0): At LF slicer LPF trimming (LFbias<2:0>) At LF Receiver operation	Can be updated with LFmode<6> = 1
Carrier AMP on	LF carrier out AMP: ON (1), OFF (0) switch	Can be updated with LFmode<6> = 1
VT monitor	RSSI VT reference voltage monitor	Can be updated with LFmode<6> = 1
Bias monitor	LF bias setting voltage monitor	Can be updated with LFmode<6> = 1

■ LF RSSI mode Control — Not Bit Addressable

ESFR: 0xC7 — LFmodeRSSI

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	loadregister	loadRSSIVT	loadAGCset	Abortdisable	loadDataC	LF AMPGain	–	–
Access	w	w	w	w	w	W	–	–
At Power on reset	0	U	U	U	U	U	x	x
At Timer reset	0	S	S	S	S	S	x	x
At Reset	0	0	0	0	–	–	–	–

loadregister	LFmode RSSI register setting	Can be updated with bit7 (loadregister) = 1
loadRSSIVT	LFrssiVT register setting	Can be updated with bit7 (loadregister) = 1
loadAGCset	AGC (input variable attenuator) register setting	Can be updated with bit7 (loadregister) = 1
AbortDisable	Abort function enable (0), disable (1)	Can be updated with bit7 (loadregister) = 1
loadDataC	LFdataC register setting	Can be updated with bit7 (loadregister) = 1
LF_AMPgain	LF AMP Gain setting: High gain (1)/ Low gain (0)	Can be updated with bit7 (loadregister) = 1

■ LF Data width count — Not Bit Addressable

ESFR: 0xC5 — LFdataC

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	dataCEN	DataCount<6:0>						
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

dataCEN	LF data count setting: Auto (0), Fixed (1)	Can be updated with LFmodeRSSI<3> = 1
DataCount<6:0>	LF data width count<6:0>. Active with dataCEN = 1	Can be updated with LFmodeRSSI<3> = 1

■ LF PreAmble Width UpperTimeLimit — Not Bit Addressable

ESFR: 0xAB — LFpUT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LFpUT<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LFpUT<7:0>	PreAmble Cycle count Upper Time Limit: LFpUT<7:0>	Can be updated with LFmode<6> = 1

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- LF PreAmble Width LowerTimeLimit — Not Bit Addressable

ESFR: 0xAC — LFpLT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	LFpLT<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

LFpLT<7:0> PreAmble Cycle count LowerTime Limit: LFpLT<7:0> Can be updated with LFmode<6> = 1

- LF SYNC Tail pattern — Not Bit Addressable

ESFR: 0xAD — LFsync0

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SYNC<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

SYNC<7:0> SYNC Tail Pattern Can be updated with LFmode<6> = 1

- LF SYNC Head pattern — Not Bit Addressable

ESFR: 0xAE — LFsync1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SYNC<14:8>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	U	U	U	U	U	U	U
At Timer reset	x	S	S	S	S	S	S	S

SYNC<14:8> SYNC Head Pattern Can be updated with LFmode<6> = 1

- LF Wake ID #0 Tail pattern — Not Bit Addressable

ESFR: 0xAF — LFwake0L

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	WAKE0<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

WAKE0<7:0> WAKE ID Tail Pattern Can be updated with LFmode<6> = 1

- LF Wake ID #0 Head pattern — Not Bit Addressable

ESFR: 0xB1 — LFwake0H

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	WAKE0<15:8>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

WAKE0<15:8> WAKE ID Head Pattern Can be updated with LFmode<6> = 1

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- LF Wake ID #1 Tail pattern — Not Bit Addressable

ESFR: 0xCC — LFwake1L

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	WAKE1<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	S	S	S	S	S	S	S	S

WAKE1<7:0> WAKE ID Tail Pattern — Can be updated with LFmode<6> = 1

- LF Wake ID #1 Head pattern — Not Bit Addressable

ESFR: 0xCD — LFwake1H

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	WAKE1<15:8>							
Access	w	w	w	w	w	w	w	w
At Power on reset	U	U	U	U	U	U	U	U
S	S	S	S	S	S	S	S	S

WAKE1<15:8> WAKE ID Head Pattern — Can be updated with LFmode<6> = 1

- LF Receiver State — Not Bit Addressable

ESFR: 0xC8 — LFstate

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Ready Rx	DATA Valid	ID Valid	SYNC Valid	SYNC Head_Valid	Preamble Valid	Abort	LF-OSC/32
Access	r	r	r	r	r	r	r	r
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	D	D	D	D	D	D	D	D

Ready Rx	Rxdata Ready
Data Valid	Data (Sync, Wakeup ID, Data) matching flag: 1 when matched
ID Valid	Valid Wake-ID detection
SYNC Valid	Valid SYNC pattern detection
SYNC Head Valid	Valid SYNC head 111 pattern
Preamble Valid	Valid Preamble Detection
Abort	LF Receiver abort flag
LF-OSC/32	LF-OSC output divided by 32

- LF Analog FrontEnd Status — Bit Addressable

ESFR: 0xE1 — LFanalogFE

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Ready_AMP	Monitor_BIAS	RSSI by VT	RSSI by average	LF Carrier OUT	LF-OSC	Sample	BIT0
Access	r	r	r	r	r	r	r	r
At Power on reset	U	U	U	U	U	U	U	U
At Timer reset	D	D	D	D	D	D	D	D

Ready AMP	LF AMP Ready Flag	
Monitor BIAS	Bias Current TRIM Monitor	
RSSI by VT	RSSI Threshold Comparator output	
RSSI by average	RSSI Average Slicer output	At Slicer offset trim, LFmode<BIT6> = 0 At Slicer LPF trim, LFmode<BIT6> = 1
LF Carrier OUT	LF AMP Carrier output	
LF-OSC	LF-OSC (300 kHz) clock output	
Sample	Sample timing	
BIT0	Incoming Data BIT0 monitor	

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- LF RX data buffer — Not Bit Addressable

ESFR: 0xE2 — LFrxData

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RxData<7:0>							
Access	r	r	r	r	r	r	r	r
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	D	D	D	D	D	D	D	D

RxData<7:0> LF Rx Data

- LF data count — Not Bit Addressable

ESFR: 0xEC — LFdataCount

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Wake-ID	LFdataCount<6:0>						
Access	r	r	r	r	r	r	r	r
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	D	D	D	D	D	D	D	D

Wake-ID Wake-ID indicator

LFdataCount<7:0> 1bit Data width counted by 300 kHz OSC

- LF Abort Timing — Not Bit Addressable

ESFR: 0xDC — LFabort

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OVERALLabort<4:0>					PREAMBLEabort<2:0>		
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	D	D	D	D	D	D	D	D

OVERALLabort<4:0> LF Sniffing overall time limit setting: Time = (OVERALLabort<4:0> * 512 + 257) * 4 * 3.3 µs

PREAMBLEabort<2:0> Preamble detecting time limit setting: Time = PREAMBLEabort<2:0> * 128 * 4 * 3.3 µs
If PREAMBLEabort<2:0> = 0, do not abort preamble detection

- LF Carrier Detect — Not Bit Addressable

ESFR: 0xDD — LFCarrierDET

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	PreVALID	LFcarrierDET<3:0>			
Access	x	x	x	w	w	w	w	w
At Power on reset	x	x	x	0	0	0	0	0
At Timer reset	x	x	x	D	D	D	D	D

PreVALID Prevalid signal timing select: 1 = 3 continuous preamble signal
0 = 5 continuous preamble signal

LFcarrierDET<3:0> Carrier Signal detection time (for Protocol 1a): Time = (1+LFcarrierDET<3:0>)* 8 * 3.3 µS
Protocol 1b, 1c, and 2, should be set to LFcarrierDE<3:0> = 0

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3.7 Sensor

The basic architecture of the sensor block is shown in Figure 3-24. All measurements of pressure, acceleration, temperature and battery voltage are achieved with the comparison of the capacitance (or electric charges stored in the capacitor) between the reference capacitor and the sensing capacitor.

First, the sensing bias point (VS) is biased at the neutral voltage by closing the switch of sense amp. At the same time, the other side of sensing capacitor (C_{sense}) and reference capacitor (C_{ref}) are biased at the low side and high side of the reference pulse driver output voltage, respectively. After opening the switch, the polarity of the pulse input for each capacitor is changed to the opposite side. If the capacitances of C_{sense} and C_{ref} are the same, the sensing output voltage (VS) will not change. If the capacitances are different, the output of the sense amp falls into H or L. The sensor capacitance is determined by finding the neutral point when changing the reference capacitor value.

The measurements are processed automatically by the internal sequencer just after setting the reference capacitor value with the appropriate registers. With this configuration and calibration, the sensor ADC achieves 13-bit equivalent performance.

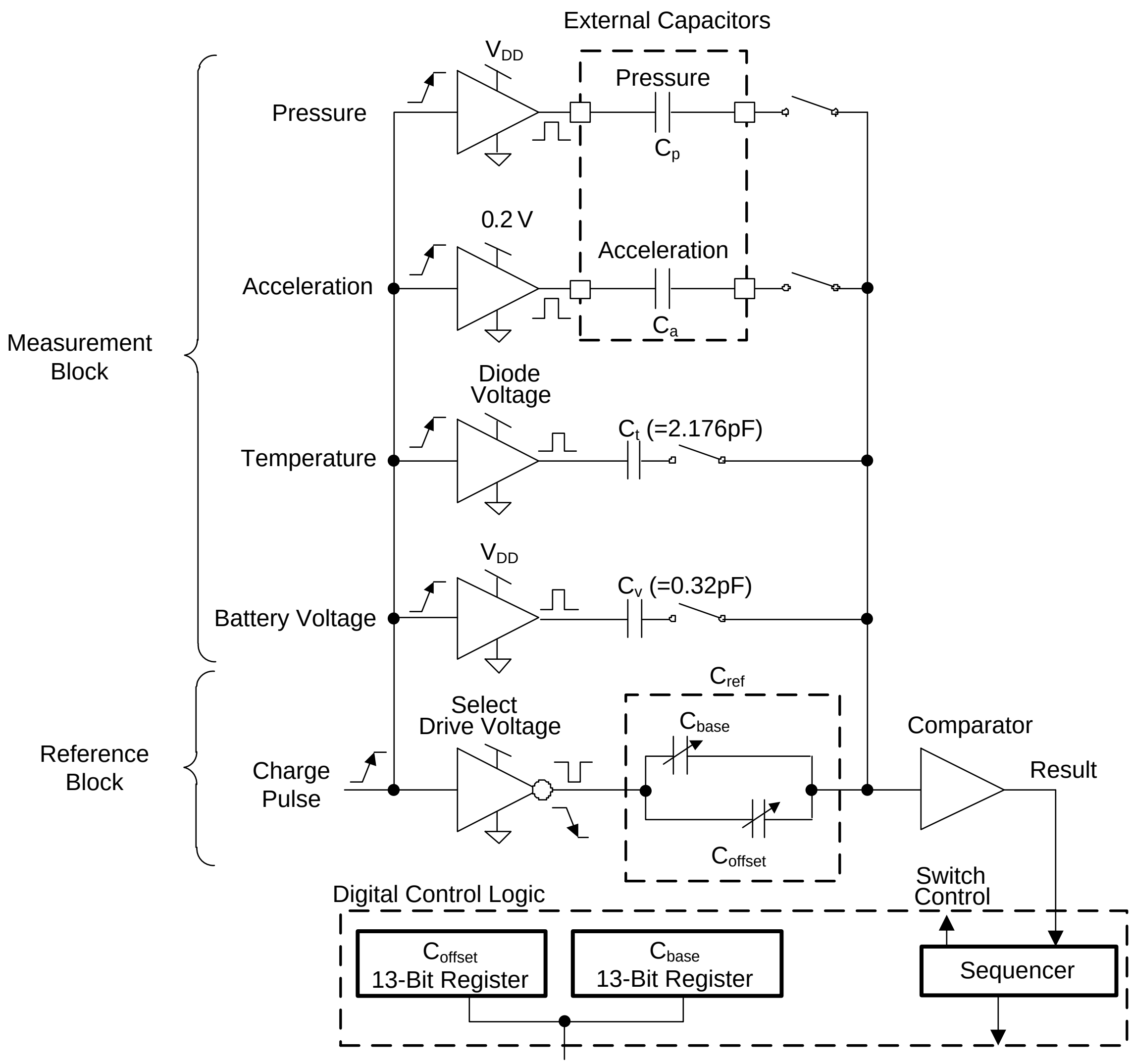

Figure 3-24. 13-bit SAR-ADC Sensor Block Diagram

The following describes the measurement techniques used for each sensor elements:

1. **Pressure measurement:** Tire pressure can be measured by comparing the capacitance of the

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diaphragm (C_p) on the ceramic package and the capacitance of the internal 13-bit reference capacitors, C_{ref}. At pressure measurement, C_{ref} is charged by the battery voltage. The LSB of the C_{ref} capacitor is 0.5 fF.

2. **Acceleration measurement:** Tire acceleration can be measured by comparing the capacitance of the external accelerator capacitor (C_a) and the capacitance of the internal 13-bit reference capacitors, C_{ref}. At acceleration measurement C_{ref} is charged by 0.2 V. The external acceleration capacitor module has two capacitors to detect two acceleration directions.
3. **Temperature measurement:** Tire temperature can be measured by comparing the capacitance of an internal capacitor charged by using PN junction diode (C_t) and the capacitance of the internal 13-bit reference capacitors, C_{ref}. At temperature measurement, C_{ref} is charged by using band gap reference voltage which is independent to temperature. Since PN junction has temperature characteristics of –2 mV/°C, the temperature can be detected from the charged voltage of the reference block, the ratio of the measured capacitance, and C_t of 2.176 pF. The designed measurable temperature resolution is 0.05°C in typical condition.
4. **Battery voltage measurement:** Battery voltage can be measured by comparing the capacitance (C_v) of the internal capacitor charged by supply voltage and the capacitance of the internal 13-bit reference capacitors, C_{ref}. At battery voltage measurement, C_{ref} is charged by using band gap reference voltage, which is independent to battery voltage. The battery voltage can be detected from the charged voltage of the reference block and the ratio of the measured capacitance and C_v of 0.32 pF. The designed measurable voltage resolution is 0.625 mV under typical conditions.

Most of the measurement functions and adjustment parameters are pre-fixed by hardware and firmware. Therefore, the user can obtain the measured value by calling the APIs. For the detail of usage of APIs, refer to the Software Application Note.

■ Sensor Control — Not Bit Addressable

ESFR: 0xB3 — SensorCONT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Power	SMODE<2:0>			PostWait<1:0>		PreWait<1:0>	
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

Power	Power Control ON(1) OFF(0)
SMODE<2:0>	Sensor Mode Control
PostWait<1:0>	Sensor Wait Time
PreWait<1:0>	Sensor Wait Time

SMODE<2>	SMODE<1>	SMODE<0>	Operation
1	1	1	Calibration Mode
1	1	0	Do not use this mode. (Pressure Reference Measurement mode)
1	0	1	Pressure Measurement mode
1	0	0	Acceleration 2 Measurement
0	1	1	Acceleration 1 Measurement
0	1	0	Temperature Measurement
0	0	1	Do not use this mode. (Shock Sensor Measurement)
0	0	0	BATT voltage Measurement

PreWait<1>	PreWait<0>	Operation(
1	1	10 clock cycle
1	0	6 clock cycle
0	1	4 clock cycle

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PreWait<1>	PreWait<0>	Operation(
0	0	3 clock cycle

PostWait<1>	PostWait<0>	Operation(
1	1	16 clock cycle
1	0	8 clock cycle
0	1	4 clock cycle
0	0	2 clock cycle

- Sensor OffsetL — Not Bit Addressable

ESFR: 0xB4 — SensorOffsetL

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SensorOffset<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

SensorOffset<7:0> SensorOffset lower Value

- Sensor OffsetH — Not Bit Addressable

ESFR: 0xB5 — SensorOffsetH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	EN AnalogOUT	SensorOffset<12:8>				
Access	–	–	w	w	w	w	w	w
At Power on reset	x	x	0	0	0	0	0	0
At Timer reset	x	x	0	0	0	0	0	0

EN AnalogOUT Enable (1), Disable (0)
SensorOffset<12:8> SensorOffset higher Value

PreWait< 0 >	Operation [1]
1	Test Monitor of 0.40 V Internal Voltage Reference to DO terminal
0	Test Monitor of 1.24 V Internal Voltage Reference to DO terminal

(1) Valid with EN_AnalogOUT = H, the check byte signal that comes from SPI is lost during this mode.

- Sensor BaseL — Not Bit Addressable

ESFR: 0xB6 — SensorBaseL

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SensorBase<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

SensorBase<7:0> SensorBase lower Value

- Sensor BaseH — Not Bit Addressable

ESFR: 0xB7 — SensorBase H

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	–	SensorBase<12:8>				
Access	–	–	–	w	w	w	w	w
At Power on reset	x	x	x	0	0	0	0	0
At Timer reset	x	x	x	0	0	0	0	0

SensorBase<12:8> SensorBase higher Value

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■ Sensor Compensation BIT6 Not Bit Addressable

ESFR: 0xB9 SensorDC0

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SensorDC0<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

SensorDC0<6:0> Compensation for BIT6 of SensorOffset<12:0> for TEST. Do not use for the Sensor Measurement.

■ Sensor Compensation BIT7 Not Bit Addressable

ESFR: 0xBA SensorDC1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SensorDC1<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

SensorDC1<6:0> Compensation for BIT7 of SensorOffset<12:0> for TEST. Do not use for the Sensor Measurement.

■ Sensor Compensation BIT8 Not Bit Addressable

ESFR: 0xBB SensorDC2

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SensorDC2<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

SensorDC2<6:0> Compensation for BIT8 of SensorOffset<12:0> for TEST. Do not use for the Measurement.

■ Sensor Compensation BIT9 Not Bit Addressable

ESFR: 0xBC SensorDC3

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SensorDC3<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

SensorDC3<6:0> Compensation for BIT9 of SensorOffset<12:0> for TEST. Do not use for the Measurement.

■ Sensor Compensation BIT10 Not Bit Addressable

ESFR: 0xBD SensorDC4

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SensorDC4<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

3

SensorDC4<6:0> Compensation for BIT10 of SensorOffset<12:0> for TEST. Do not use for the Measurement.

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- Sensor Compensation BIT11 — Not Bit Addressable

ESFR: 0xBE — SensorDC5

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	SensorDC5<6:0>						
Access	–	w	w	w	w	w	w	w
At Power on reset	x	0	0	0	0	0	0	0
At Timer reset	x	0	0	0	0	0	0	0

SensorDC5<6:0> Compensation for BIT11 of SensorOffset<12:0> for TEST. Do not use for the Measurement.

- Sensor Compensation BIT12 — Not Bit Addressable

ESFR: 0xBF — SensorDC6

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Activate_SensorDC	SensorDC6<6:0>						
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

Activate_SensorDC Activate to add Sensor Compensation Data (SensorDC6-SensorDC0): Enable (1), Disable (0), must be set to SensorDC6<6:0> = 0 when Disable (0).

SensorDC6<6:0> Compensation for BIT12 of SensorOffset<12:0> for TEST. Do not use for the Measurement.

- Sensor State — Not Bit Addressable

ESFR: 0xC0 — SensorState

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Ready BG	BUSY Conversion	Result_A/D	–	–	–	–	–
Access	r	r	r	–	–	–	–	–
At Power on reset	0	0	U	x	x	x	x	x
At Timer reset	0	0	U	x	x	x	x	x

Ready_BG Ready Flag of Bandgap Reference Regulator

BUSY Conversion Status Flag of A/D Conversion

Result_A/D A/D conversion Result

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3.8 Debug Mode

3.8.1 ESFR

- TEST Mode control0 Not Bit Addressable

ESFR: 0x84 TESTmux0

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	EN UART	Reserved	EN_Interrupt	EN BP Interrupt	Reserved			
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

EN UART	Enable UART debug interface	
EN_Interrupt	Interrupt IE0 from RESET_TEST	0: Disable, 1: Enable
EN BP Interrupt	Interrupt IE0 from RESET TEST	0: Disable, 1: Enable

- TEST Mode Control Not Bit Addressable

ESFR: 0x91 TESTvector

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Reserved		TestVector<5:0>					
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

TestVector<5:0> To be used as a TEST Vector when Micro restarts

- Upper Breakpoint Register Not Bit Addressable

ESFR: 0x92 BPU

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	–	–	BPU<5:0>					
Access	–	–	w	w	w	w	w	w
At Power on reset	x	x	0	0	0	0	0	0
At Timer reset	x	x	0	0	0	0	0	0

- Lower Breakpoint Register Not Bit Addressable

ESFR: 0x93 BPL

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BPL<7:0>							
Access	w	w	w	w	w	w	w	w
At Power on reset	0	0	0	0	0	0	0	0
At Timer reset	0	0	0	0	0	0	0	0

BPU<5:0>	Upper Breakpoint Register
BPL<7:0>	Lower Breakpoint Register
	BreakPoint Address BP<13:0> = BPU<5:0> * 256 + BPL<7:0>

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4 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

(T_A = –40°C to 125°C, unless otherwise specified)(1) (2)

				MIN	TYP	MAX	UNIT
V_{DD}	VDD–GND	Supply Voltage		–0.3		3.6	V
	RESET_ TEST			–0.3		7	V
PP1 PP2	Diaphragm	Pressure Sensor Input Pressure (Absolute)		0		1100	kPa
V_I	DI	Input Voltage Range		–0.3		V_{DD}+0.3	V
	XTAL			–0.3		V_{DD}+0.3	
	RFOUT			–0.3		V_{DD}+0.3	
V_{ILD}	LD			–0.3		V_{DD}+0.3	
V_{ICK}	CK			–0.3		V_{DD}+0.3	
I_{OST}	RFOUT	Output Current				20	mA
	DO					10	
	TVO					10	
As		Static Acceleration Mechanical shock	Diaphragm Direction (z)			2000	G
Adc			Package-side Direction (x, y)			100	
Adp		Dynamic Acceleration Mechanical shock	Any Direction (< 10 mS)			7000	G
T_J		Operating Junction Temperature Range		–40		150	°C
T_A		Operating Ambient Temperature Range		–40		125	°C
T_{stg}		Storage Temperature Range		–65		150	°C
	All pins	Lead Temperature (Soldering, 10 s)				260	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) Note all voltage values are with respect to GND.

4.2 Recommended Operating Conditions(1)

(T_A = –40ºC to 125°C, V_{DD} = 1.5 V to 3.5 V, unless otherwise specified)

				MIN	TYP	MAX	UNIT
V_{DD}	VDD–GND	Supply Voltage		1.5	3	3.5	V
PP1	Diaphragm	Input Pressure Range (for Section 5.1.1)	After software adjustment	50		635	kPa
PP2	Diaphragm	Input pressure range (for Section 5.1.2)	After software adjustment	50		635	kPa
MM	Accelerometer	Input Acceleration Range	Measurement	–2		10	G
			Withstand	–1600		1600	
V_{IH}	CK, LD, DI	H Level Input Voltage Range		0.8×V_{DD}		V_{DD}	V
	RESET_TEST			V_{DD}+3		6.9	
V_{IL}	CK, LD, DI	L Level Input Voltage Range		0		0.2×V_{DD}	V
	RESET_TEST			0		V_{DD}+0.8	
F_{CLK}	CK	Input Frequency				10	MHz
F_{XTAL}	XTAL			19.68	19.70	19.72	
F_{CLF}	LFIN			120	125	130	kHz
T_A		Operating Ambient Temperature Range		–40	25	125	°C

(1) The accelerometer characteristic is applied only for TPIC8201XX.

Figure 4-1 shows the relationship between the package diaphragm side and the accelerator measurement direction.

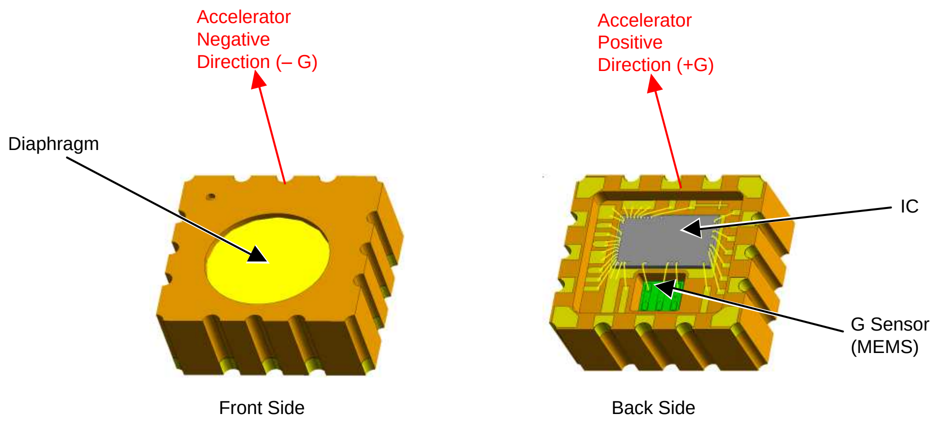

Figure 4-1. Relationship Between Package Diaphragm Side and Accelerator Measurement Direction

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5 ELECTRICAL CHARACTERISTICS

5.1 Sensor

There are two specifications available at the TEST (selection A and B) of the same pressure sensor shown in Section 5.1.1, Section 5.1.2, Figure 5-1 and Figure 5-2.

5.1.1 Pressure Sensor (Selection A) for (50 kPa to 635 kPa Range)

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PSR1	Pressure Measurement Resolution	PPS = 50 kPa to 635 kPa		0.86		kPa
PSA1	Pressure Measurement Accuracy (After Software Compensation)	200 kPa ≤ PPS < 450 kPa –30°C ≤ T_A < 100°C	–7		7	kPa
		200 kPa ≤ PPS < 450 kPa –40°C ≤ T_A < –30°C 100°C ≤ T_A < 120°C	–10		10	kPa
		100 kPa ≤ PPS < 200 kPa –40°C ≤ T_A < 120°C	–15		15	kPa
		Other than above	–20		20	kPa

5.1.2 Pressure Sensor (Selection B) for (50 kPa to 635 kPa Range)

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PSR2	Pressure Measurement Resolution	PPS = 50 kPa to 635 kPa		0.86		kPa
PSA2	Pressure Measurement Accuracy (After Software Compensation)	100 kPa ≤ PPS < 450 kPa –40°C ≤ T_A < 0°C	–15		15	kPa
		100 kPa ≤ PPS < 450 kPa 0°C ≤ T_A < 50°C	–8		8	kPa
		100 kPa ≤ PPS < 450 kPa 50°C ≤ T_A < 125°C	–15		15	kPa
		Other than above	–20		20	kPa

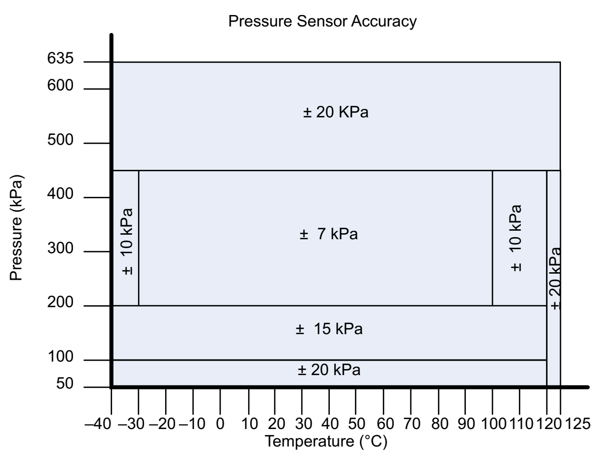

Figure 5-1. Pressure Sensor (Selection A)

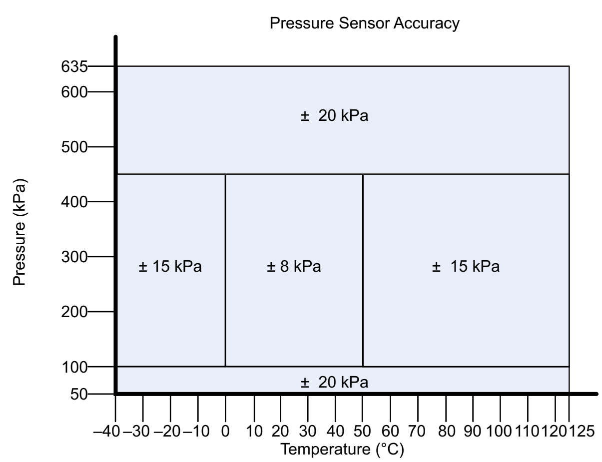

Figure 5-2. Pressure Sensor (Selection B)

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5.1.3 Temperature / Voltage / Acceleration Sensor

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSR	Temperature Measurement Resolution	TTS = –40°C to 125°C		0.05		°C
TSA	Temperature Measurement Accuracy	–40°C ≤ T_A < –20°C	–5		5	°C
		–20°C ≤ T_A < 70°C	–3		3	
		70°C ≤ T_A ≤ 125°C	–5		5	
VSR	Voltage Measurement Resolution			0.625		mV
VSA	Voltage Measurement Accuracy		–0.1×V_{DD}		0.1×V_{DD}	V
GSR	Acceleration Measurement Resolution(1)			0.0625		G
GSA	Acceleration Measurement Accuracy(1)	Detection of acceleration at 5 G	–3		3	G

(1) The accelerometer characteristic is applied only for TPIC8201XX.

5.2 Power Supply

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Consumption Current	VDD	Standby Timer-OSC only (T_A = 25°C, V_{DD} = 3 V)		0.1	0.4	µA
			Standby with LF receiving LF AMP + Carrier detection (T_A = 25°C, V_{DD} = 3 V) For Protocol 1a,1c,2		4.5	12	µA
			Standby with LF receiving LF AMP + Pattern detection (T_A = 25°C, V_{DD} = 3 V) For Protocol-1b		11	18	µA
			Measurement State (T_A = 25°C, V_{DD} = 3 V)		1.53		mA
			Measurement State		1.53	2.1	mA
			MCU Power On mode with Xtal-OSC(1) (T_A = 25°C, V_{DD} = 3 V)		1.3	1.6	mA
			MCU Power On mode with Xtal-OSC (1)			2.9	mA
			315 MHz Transmitting State, Po = 5 dBm (T_A = 25°C, V_{DD} = 3 V)		9	10	mA
			315 MHz Transmitting State, Po = 5 dBm		9	12	mA
			434 MHz Transmitting State, Po = 5 dBm (T_A = 25°C, V_{DD} = 3 V)		10.5	11.5	mA
			434 MHz Transmitting State, Po = 5 dBm		10.5	14	mA

(1) Xtal-OSC bias <3:0> = 8

5.3 Xtal-OSC

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal}	Oscillation Frequency	XTAL	KYOCERA CX3225SA XTAL = 19.707894 MHz, ESR(CI) = 30 Ω		19.70789		MHz
F_{start}	Oscillation Start-up time(1)	XTAL				4	ms
F_{margin}	Oscillation Margin	XTAL	KYOCERA CX3225SA XTAL = 19.707894MHz, ESR(CI) = 30 Ω	10			Times
C_{xtal}	XTAL Input Capacitance(2)	XTAL		5	6.7	10	pF

(1) Reference data
(2) Included package capacitance. Design specified.

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5.4 PLL

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V, except 25°C < T_A< 125°C, 1.75 V ≥ V_{DD} (unless otherwise specified)

PARAMETER			PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{lock}	Lock up time		RFOUT			10	100	µs
PN	Phase Noise		RFOUT	10 kHz offset		–80	–60	dBc/Hz
				100 kHz offset		–80	–70	
				1 MHz offset		–90	–80	
F_{vcomin}	Minimum VCO Oscillation Frequency (1)		RFOUT				150	MHz
F_{vcomax}	Maximum VCO Oscillation Frequency (1)	315 MHz (2)	RFOUT	25°C < T_A < 125°C, 1.75 V ≤ V_{DD}	350			MHz
		434 MHz (3)			450			

(1) Design specified
(2) The 315 MHz characteristic is applied for TPIC820XX3.
(3) The 434 MHz characteristic is applied for TPIC820XX4.

5.5 Timer-OSC

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{tm}	Oscillation Frequency (1)		After software adjustment	400	450	500	Hz
F_{tmeror}	Oscillation Frequency Adjustment Error		After software adjustment	–10%		10%	
$F_{tmdrift}$	Oscillation Frequency Temperature Drift		⊿t = 20°C 80°C T_A ≤ 125°C			2	%/°C
			⊿t = 20°C –40°C ≤ T_A ≤ 80°C		0.5	1	

(1) LF sniffing interval is determined by oscillation frequency. For LF pattern Protocol 1a and 1c, use LF sniffing interval including variation (should be trimmed shorter than preamble period).

5.6 9.6 MHz RC-OSC

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V, (unless otherwise specified)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{rco}	Oscillation Frequency		After software adjustment	7.68	9.6	11.52	MHz

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5.7 BB Modulator and RF PA

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V, except 25°C < T_A< 125°C, 1.75 V ≥ V_{DD} (unless otherwise specified)

PARAMETERS(1)			PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{TXC1}	Carrier Frequency (FSK Center Frequency)	315 MHz	RFOUT	fXTAL = 19.707894 MHz, DIV = 1/16(2)	314.977	314.980	314.983	MHz
f_{TXC2}		434 MHz	RFOUT	fXTAL = 19.707894 MHz, DIV = 1/22(2)	433.917	433.920	433.923	
f_{OF1}	Minimum Carrier Offset Adjustment Frequency	315 MHz	RFOUT	fXTAL = 19.707894 MHz			–700	kHz
f_{OF2}	Maximum Carrier Offset Adjustment Frequency	434 MHz	RFOUT	fXTAL = 19.707894 MHz	700			kHz
P_{out}	Output Power (After adjustment to 5 dBm)		RFOUT	T_A = 25°C, V_{DD} = 3 V, Load = 50 Ω	4	5	6	dBm
		315 MHz		Load = 50 Ω	1(3)	5	7	dBm
		434 MHz			0.5(3)	5	7	dBm
F_{dr}	Frequency Deviation Range		RFOUT	fXTAL = 19.707894 MHz, FSK mode	–150		150	kHz
F_{da}	Frequency Deviation Accuracy		RFOUT		–3		3	kHz
F_{dstep}	Frequency Shift Adjustment Step		RFOUT	fXTAL = 19.707894 MHz		1.2		kHz
F_{speed}	Data Speed		RFOUT	fXTAL = 19.707894 MHz, At register setting: ModScale <7:0> = 8, ModRAMAdd <5:0> = 31, FSK/ASK mode	9.62	9.93	10.26	K bits/s
				fXTAL = 19.707894 MHz, At register setting : ModScale <7:0> = 4, ModRAMAdd <5:0> = 31 FSK mode only	19.25	19.87	20.53	
F_{obw}	Occupied Bandwidth		RFOUT	TA = 25°C, V_{DD} = 3 V, Load = 50 Ω, Span = 3 MHz, 99%, RBW = 30 kHz			400	kHz
ETXS	Spurious	315 MHz	RFOUT	F < 315.25 MHz, On the test board, T_A = 25°C, V_{DD} = 3 V, Load = 50 Ω			–25	dBc
ETXS			RFOUT	f > 315.25 MHz, On the test board, T_A = 25°C, V_{DD} = 3 V, Load = 50Ω			–30	
ETXS		434 MHz	RFOUT	On the test board, T_A = 25°C, V_{DD} = 3 V, Load = 50 Ω			–25	

(1) For the electrical characteristic of the BB modulator and RF PA:
The 315 MHz characteristic is applied for TPIC820XX3.
The 434 MHz characteristic is applied for TPIC820XX4.
(2) With register setting: ModRAMData <7:0> (0xC9) = 28, ModOffset <7:0> (0xD1) = 65 at 315 MHz band, 65 at 434 MHz band.
(3) 25°C < T_A < 125°C, 1.75 V ≤ V_{DD}

5.8 LF Receiver

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETERS		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{LF}	Carrier Frequency	LFIN	T_A = 25ºC, V_{DD} = 3 V	120	125	130	kHz
ModASK	AM Modulation Degree(1)	LFIN		50%		100%	
Strig1a	Minimum Input Sensitivity1	LFIN	For Protocol 1b		0.5	1.2	mVpp
Strig1b	Minimum Input Sensitivity2	LFIN	For Protocol 1a, 1c, 2		0.7	1.7	mVpp
Strig2	Maximum Input Sensitivity	LFIN	For Protocol 1a, 1b, 1c, 2	303			mVpp
LF_{osc}	LF Oscillator Frequency		After Software Adjustment	285	300	360	kHz
LFsn	Signal-to-noise ratio(1)	LFIN	T_A = 25ºC, V_{DD} = 3 V	6			dB

(1) Design specified

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T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETERS			PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNITS
T1a	LF Sniffing Interval (2)	Protocol 1a	LFIN	T_A = 25ºC, V_{DD} = 3 V		2.2		ms
T1b		Protocol 1b	LFIN	T_A = 25ºC, V_{DD} = 3 V		205		ms
T1c		Protocol 1c	LFIN	T_A = 25ºC, V_{DD} = 3 V		2.2		ms
T2		Protocol 2	LFIN	T_A = 25ºC, V_{DD} = 3 V, T_{WAKE} = 5 mS		2.2		ms
TW1a	LF Sniff-On Period (2)	Protocol 1a	LFIN	T_A = 25ºC, V_{DD} = 3 V	280		450	µs
TW1b		Protocol 1b	LFIN	T_A = 25ºC, V_{DD} = 3 V		7		mS
TW1c		Protocol 1c	LFIN	T_A = 25ºC, V_{DD} = 3 V	150		270	µs
TW2		Protocol 2	LFIN	T_A = 25ºC, V_{DD} = 3 V	150		270	µs
f_{LFp1}	Data Speed	Protocol 1a, 1b, 1c	LFIN	T_A = 25ºC, V_{DD} = 3 V	3.8	3.9	4	kbits/s
f_{LFp2}		Protocol 2	LFIN	T_A = 25ºC, V_{DD} = 3 V		100		bps
L_{Frin}	Input Resistance (1)		LFIN	T_A = 25ºC, V_{DD} = 3 V	1000			kΩ
C_I	Input Capacitance (1)		LFIN		1.6	2	2.4	pF

(2) Refer to each timing example of Protocol 1a (see Section 3.6.3.1), 1b (see Section 3.6.3.2), 1c (see Section 3.6.3.3), and 2 (see Section 3.6.3.6).

5.9 Voltage Regulator (VREG)

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified) (1) (2)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{reg}	VREG Output Voltage	VREG	I_{Load} = 0 mA, C_L = 0.1 µF ±10% (3)	1.45	1.55	1.65	V
T_{vreg}	VREG Startup Time	VREG	I_{Load} = 0 mA, C_L = 0.1 µF ±10% (3)			0.5	ms
I_{peak}	Peak current at VREG Startup	V_{DD}	I_{Load} = 0 mA, C_L = 0.1 µF ±10% (3)			5	mA

(1) This voltage regulator is only for the supply voltage of the internal circuit. It is not designed to be the power supply source of any external circuitry.
(2) Recommended decoupling capacitor: 0.1 µF,
Capacitor tolerance: max ±10%
Temperature variation: max ±15% over T_A = –40ºC to 125ºC,
ESR: max 1 Ω
(3) C_L (Decoupling capacitor) should be connected between the VREG pin and GND.

5.10 Power-on-Reset and Hardware Reset

T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V (unless otherwise specified)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tr-VDD	Rising time of V_{DD}	VDD				1	ms
off-VDD	Interval of V_{DD} power on	VDD		8			ms
tW-RST	Reset Pulse width	RESET-TEST		1			µs
	Pull-down resistance	RESET-TEST	V_{IN} (RESET-TEST) = 1 V	30	50	80	kΩ

Figure 5-3 shows the Power-on-Reset and the Hardware Reset.

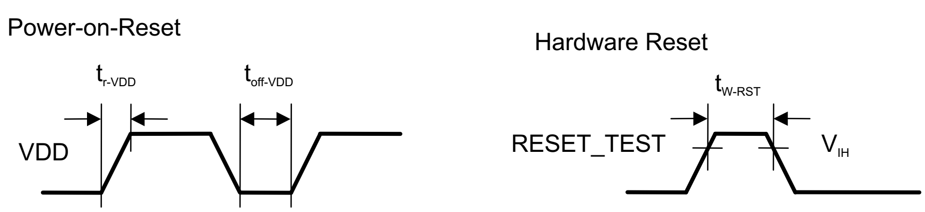

Figure 5-3. Power-on-Reset and Hardware Reset

5.11 EEPROM

Read: T_A = –40°C to 125°C, V_{DD} = 1.5 V to 3.5 V: **Program:** T_A = 0°C to 50°C, V_{DD} = 2.5 V to 3.5 V (unless otherwise specified)

PARAMETER		PIN NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VPP	Program voltage			12	12.4	14	V
T_{eeprom}	Program time			10	20	100	ms
N_{eeprom}	Number of Program times			10			times
L_{eeprom}	Storage life time			10			years

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC82000FFE	PREVIEW	LCCC	FFE	16	416	TBD	Call TI	Call TI	-40 to 125		
TPIC82000FFER	PREVIEW	LCCC	FFE	16	1000	TBD	Call TI	Call TI	-40 to 125		
TPIC82010FFE	PREVIEW	LCCC	FFE	16	416	TBD	Call TI	Call TI	-40 to 125		
TPIC82010FFER	ACTIVE	LCCC	FFE	16		TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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