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Features

- Antenna Driver Stage with Adjustable Antenna Peak Current for up to 1.5A
- Frequency Tuning Range from 100 kHz to 150 kHz
- Automatic Antenna Peak Current Regulation
- Self-tuning Oscillator for Antenna Resonant Frequency Adaption
- Capable of Driving a High-Q Antenna
- Integrated 5V Regulator for External Load up to 10 mA
- Bi-directional Single Wire Interface for Microcontroller or ECU
- LF Baud Rates up to 4 kbaud and Amplitude Shift Keying (ASK) Modulation
- Low Power Standby Mode < 50 μ A
- Antenna Driver Diagnosis: Peak Current, Antenna Frequency and Battery Voltage Monitoring
- Power Supply Range 8V to 24V Direct Battery Input
- Load Dump Protection
- Operation at Temperature -40°C to $+105^{\circ}\text{C}$
- EMI and ESD According to Automotive Requirements
- Highly Integrated, Fewer External Components Required
- Overtemperature Protection

Applications

- Tire Pressure Measurement (TPM)

Benefits

- Self Tuning Capability to Antenna Resonance Frequency
- Adjustable Antenna Peak Current Value
- Highest Integration Level for Embedded Automotive Systems

Electrostatic sensitive device.

Observe precautions for handling.



1. Description

The ATA5275 is an integrated 1.5A peak current BCDMOS antenna driver IC dedicated as a 125 kHz wake-up channel transmitter for TPM applications.

It includes the full functionality to generate a magnetic LF field in conjunction with an antenna coil to transmit data and power to a receiver. The transmission can be controlled via a one wire I/O-interface by an external unit.

The smart power IC is delivered in a QFN20 power package with heat slug.



**125 kHz
Transmitter IC
for TPM**

ATA5275

Rev. 4739I-AUTO-01/06



2. General Description

The ATA5275 is a 125-kHz transmitter IC. It is dedicated to driving 125 kHz LC antenna tanks, specifically for the wake-up channel in Tire Pressure Measurement (TPM) applications.

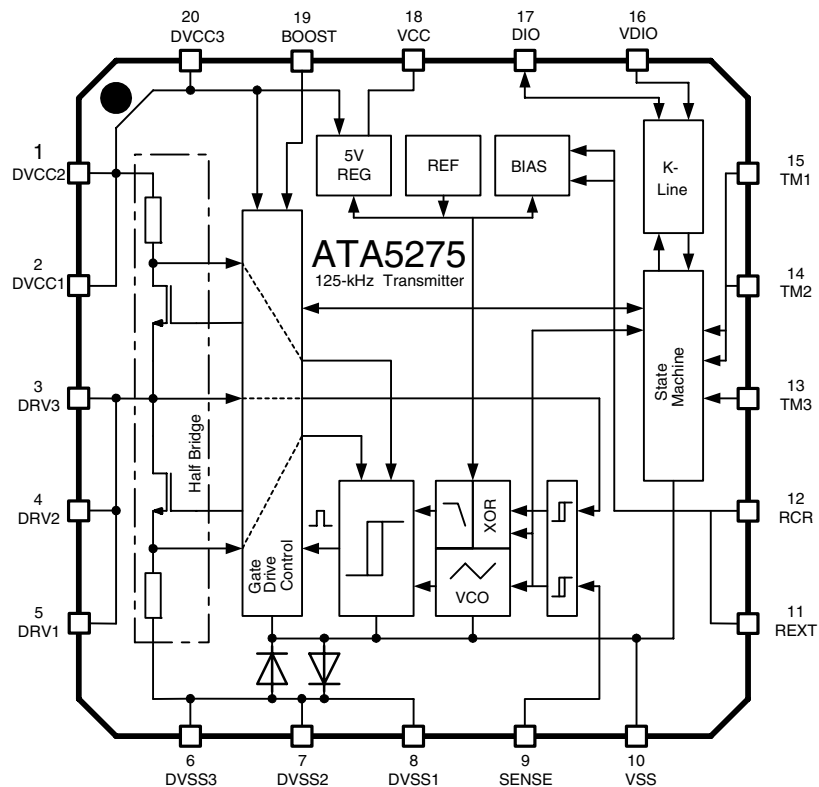
It includes a control logic with VCO which generates the 125 kHz signal for the output driver stage. A phase lock circuit regulates the driver output frequency on the antenna resonance frequency, achieving a maximum field strength on the antenna. The driver duty cycle is regulated and stabilizes the antenna current for a wide supply voltage range.

The IC can be controlled by a microcontroller or ECU via the one wire bi-directional interface. It is used for the data transmission and to indicate errors. For the data transmission ASK modulation is used. The antenna signal is modulated by the DIO interface line.

The IC has a build in diagnosis function and detects detuning and broken or short wire of the antenna circuitry. If a failure is detected the IC indicates it by an error signal via the DIO line.

The integrated 5V regulator can be used externally for a load up to 10 mA.

Figure 2-1. Block Diagram



3. Pin Configuration

Figure 3-1. Pinning QFN20

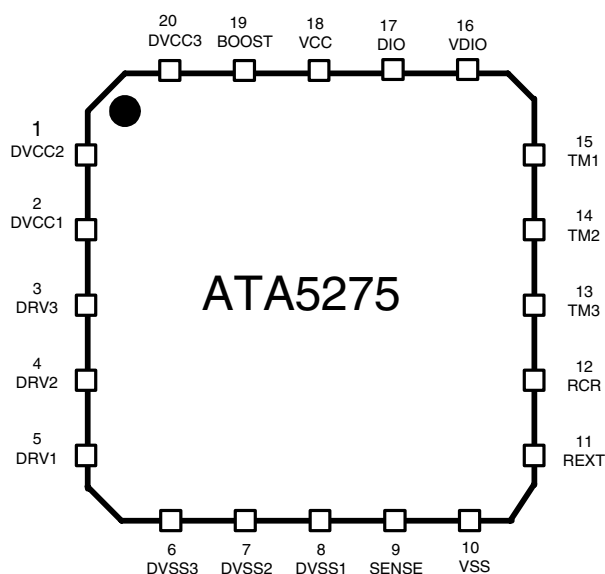


Table 3-1. Pin Description

| Pin ⁽¹⁾ | Symbol | Function |
|--------------------|--------|--|
| 1 | DVCC2 | Battery supply input |
| 2 | DVCC1 | Battery supply input |
| 3 | DRV3 | Antenna driver stage output |
| 4 | DRV2 | Antenna driver stage output |
| 5 | DRV1 | Antenna driver stage output |
| 6 | DVSS3 | Power supply ground |
| 7 | DVSS2 | Power supply ground |
| 8 | DVSS1 | Power supply ground |
| 9 | SENSE | Current zero crossing sense input |
| 10 | VSS | Analog and digital ground |
| 11 | REXT | External reference current input |
| 12 | RCR | External reference for antenna peak current |
| 13 | TM3 | For test purposes only |
| 14 | TM2 | For test purposes only |
| 15 | TM1 | For test purposes only |
| 16 | VDIO | DIO line interface voltage selection |
| 17 | DIO | One-wire serial interface line |
| 18 | VCC | 5V supply output (for external storage capacitor only) |
| 19 | BOOST | External bootstrap cap |
| 20 | DVCC3 | Battery supply input |

Note: 1. Pin numbers valid for all revisions of the ATA5275

4. Functional Description

4.1 Operation Modes

There are two different operation modes for the ATA5275:

- Standby mode
- Transmission mode

4.2 Standby Mode and Wake-up

After power-on-reset, the ATA5275 is in standby mode. For minimum power consumption, only the internal 5V supply and the DIO line interface are active. The IC can be activated by the external control unit via the serial interface. The DIO line is called logic high if it is pulled up to the VDIO voltage level. The DIO line is called logic low if it is pulled down to the VSS voltage level. A low signal at the DIO line wakes-up the IC.

The circuit enters the standby mode if either of these three conditions are fulfilled:

1. After power-on-reset and the DIO is high (see [Figure 4-1](#))
2. After a time out of $T_{OUTL}^{(1)}$ during which DIO is permanently low (see [Figure 4-3 on page 5](#))
3. After a time out of $T_{OUTH}^{(2)}$ during which DIO is permanently high and an acknowledge time $T_{ACK}/T_{ERR}^{(1)}$ (see [Figure 4-2](#))

Notes: 1. Time does not depend on the antenna resonance frequency.
2. Time depends on the antenna resonance frequency.

Figure 4-1. STBY After POR

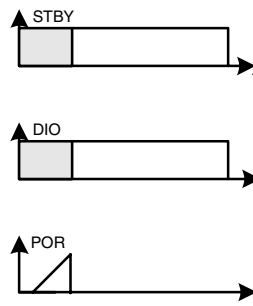


Figure 4-2. STBY After DIO = H

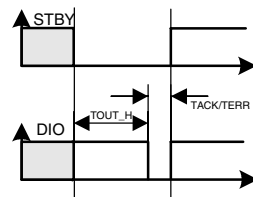
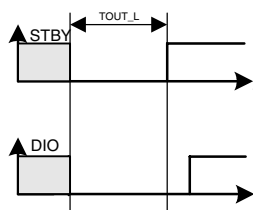


Figure 4-3. STBY After DIO = L

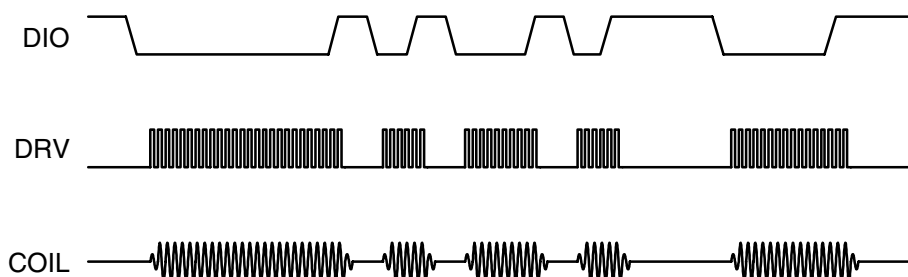


4.3 Transmission Mode

4.3.1 ASK Modulation

For the transmission of a wake-up signal or data to a receiver, the ATA5275 generates an antenna resonance synchronized signal at the antenna driver output (DRV pin). A connected LC antenna radiates a magnetic field. For the data transmission the field can be 100% amplitude modulated by the DIO interface input. If a low level signal is applied at the DIO pin, the driver generates a square wave signal DRV for the antenna. If a high level signal is applied at the DIO pin the driver is stopped and switched to ground. In this way ASK modulated data can be transmitted (see Figure 4-4).

Figure 4-4. Data Transmission



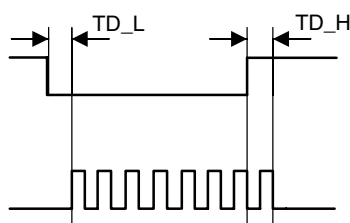
4.3.2 Anti-bouncing Filter in Transmission Mode

The DIO input signal is delayed for an anti-bouncing time.

The driver is switched on after a delay time of T_{DL} (typically 64 μ s) if the DIO is pulled to a low level continuously. The driver is switched-off after a delay time of T_{DH} if the DIO is pulled to high level.

The T_{DH} time depends on the antenna resonance frequency, suppressing short disturbance pulses from the DIO Line.

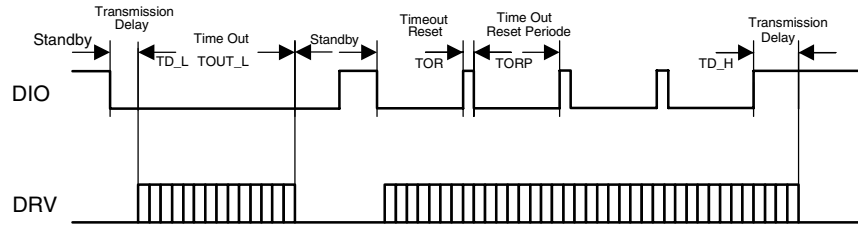
Figure 4-5. Anti-bouncing



4.3.3 Time Out and Time Out Reset

The IC has a time out supervisor for the interface line to avoid unintended continuous transmission in case of line errors. The time out timer runs if the DIO pin is pulled to a low level. If the DIO pin is permanently low for more than the time T_{OUTL} the driver is switched off and the IC enters the standby mode. This avoids the discharging of the supply battery if the DIO line has a failure like a body contact or another permanent low level failure. The time T_{OUTL} depends on the antenna resonance frequency.

Figure 4-6. Time Out and Time Out Reset Protocol



For continuous transmission periods the internal time out timer must be reset within the time out reset period T_{ORP} with a short high pulse of length T_{OR} at DIO. Any transmission time periods can be made by cyclical resetting of the time out timer (see [Figure 4-6](#)). The time T_{ORP} and T_{OR} depends on the antenna resonance frequency.

4.3.4 Transmission Acknowledge and Error Signal

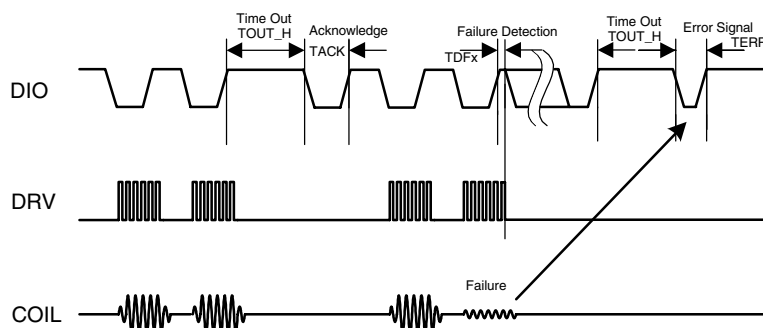
If no failure is detected during a transmission sequence the IC acknowledges the transmission by pulling the DIO line to low level for time T_{ACK} (typically 256 μ s). The acknowledge signal is generated at the end of a transmission sequence if the DIO line was high for the time T_{OUTH} (typically 16 ms).

There are two types of error detection (see section [“Diagnosis and Protection” on page 8](#)):

- Immediate switch-off of the driver stage
- The failure is indicated through the DIO line based on transmission acknowledge and Error signal

At the end of transmission the IC indicates the failure by an error signal by pulling the DIO line to a low level for time T_{ERR} (typically 128 μ s) instead of T_{ACK} .

With the acknowledge and the error signal a connected microcontroller is able to recognize failures of the IC or the antenna module as well as DIO line failures like a broken wire or a short circuit.

Figure 4-7. Transmission Acknowledge and Error Signal

The various failure types are monitored during transmission in time TFDx (see section “[Diagnosis and Protection](#)” on page 8). The time TFDx depends on the antenna resonance frequency.

4.4 Internal Voltage Regulator and POR

The IC contains a 5-V regulator. It is used for the supply voltage V_{CC} of the logic circuits and the low voltage analog circuits. Additionally, the V_{CC} can be used externally for loads up to 10 mA. The stabilized voltage is available at pin VCC and must be buffered with an external capacitor.

4.4.1 Reset

After power on or after a voltage breakdown the power-on-reset circuit of the IC generates a reset pulse which sets the logic circuit to a defined initial state. A RESET is generated if the VCC is below the reset threshold voltage V_{POR} and after power on.

4.4.2 DIO Interface

The interface can be operated either as a 5-V microcontroller interface or as automotive K-line interface with the car battery voltage. In which mode it operates must be selected with the VDIO pin. If it is connected to 5V the DIO pin operates as microcontroller interface and if it is connected with the battery voltage it operates as automotive interface according to the K-line specification.

4.5 Oscillator and Carrier Frequency Generation

A Voltage Controlled Oscillator (VCO) is used to clock the interface logic and the gate driver logic. The antenna driver output signal DRV is derived from this clock. The VCO operates in two modes: the self-oscillation mode with clock CLK_{SO} and the resonance tracking mode with clock CLK_{RT} .

4.5.1 Self-oscillating Mode

If the antenna half-bridge is not activated the VCO is in self-oscillating mode. It runs at a center frequency CLK_{SO} of typically 125 kHz with an accuracy of $\pm 8\%$. For that purpose, an external reference resistor has to be applied to pin REXT. The resistor at pin REXT determines the VCO frequency proportionally. The recommended value is 100 k Ω achieving 125 kHz oscillator frequency.

4.5.2 Resonance Tracking Mode

In case the antenna half-bridge is activated the VCO is tracked by the antenna current by means of its zero crossing detection. The VCO runs at the antenna resonance frequency stationary. The clock CLK_{RT} deviates $\pm 1.4\%$ from the antenna resonance frequency, depending on the antenna quality and resonance frequency (see section [“Application Hints” on page 14](#)). For that purpose, an antenna current shunt resistor has to be applied to the SENSE pin. The shunt resistance is used internally for the zero crossing detection of the antenna current only.

By this feature the antenna operates with the maximum voltage, current and field strength. It is recommended specially for systems with high antenna Q-factors and low LC tolerances.

4.6 Coil Driver Output and Antenna Peak Current Control

The driver circuit consists on a DMOS half-bridge designed for 1.5A peak current with low on-resistance $R_{DS(on)}$. It is short-circuit and overtemperature protected (see section [“Diagnosis and Protection” on page 8](#)). The half-bridge is switched on by a low level signal at DIO and generates a square wave voltage for the antenna RLC circuitry.

A very useful function of the driver stage is the build-in antenna current control loop. The IC senses the current through the antenna internally and controls the peak value $I_{A_{PEAK}}$ by controlling the duty cycle DC_{DRV} of the driver output.

So the antenna can be designed for maximum antenna current with the typical or even the minimum supply voltage. For higher supply voltages the current is controlled by reducing the driver duty cycle. The reference value for the antenna current $I_{A_{PEAK}}$ can be adjusted externally with a resistor R_{CR} at the RCR pin.

$$I_{A_{PEAK}} = 750 \text{ mA} \times \frac{50 \text{ k}\Omega}{R_{CR}}$$

Note: Applying the formula above, the right driver current for the antenna has to be adjusted for the worst supply voltage case. The IC operates from 14% up to 86% duty cycle for that case and reduces the duty cycle for higher voltages (for the definition of the duty cycle DC_{DRV} , see [“Application Hints” on page 14](#)).

This feature allows the user to operate the IC in a wide field of operational voltage field and protects the driver stage and the antenna from antenna overcurrent.

The driver out square wave starts with a duty cycle of 50%. After three or four cycles the duty cycle can reach its maximum. As far as the peak current will stay smaller than $I_{A_{peak}}$ this duty cycle maximum is really 100%. If during the ramp up of the antenna current the envelope of the peak current will be greater than $I_{A_{peak}} + 20\%$ a pulse skipping function will suppress the next driver output pulse to minimize the antenna current overshoot.

4.7 Diagnosis and Protection

The IC supervises several parameters of IC operation for transmission diagnosis and circuit protection.

In any case of circuit protection mode or error detection the IC indicates this states according to the transmission protocol via the DIO line (see section [“Transmission Acknowledge and Error Signal” on page 6](#)).

4.7.1 Circuit Protection Cases

The circuit protection is activated in normal mode, i.e., if the antenna circuit is driven to the oscillation with its own frequency. It is switched off in standby mode. Between the end of the transmission and the acknowledge signal the low side driver is switched on. In case a protection switch-off occurs the half-bridge is set in tri-state mode.

For all cases, there is a filter implemented to debounce half-bridge switch-off for a time of T_{DEB} (typically 20 μ s). This debounce filter is activated in case the half-bridge is activated.

These are the following circuit protection cases:

1. Load dump protection: In case the voltage at DVCC exceeds a voltage V_{BAT_LD} (typically 31V).
2. Overtemperature protection: In case the junction temperature exceeds a value of TSD (typically 165°C).
- 3.

4.7.2 Error Diagnosis

During the transmission the diagnosis function of the IC supervises the antenna current and frequency and the half-driver bridge supply voltage. If any error is detected at the end of the transmission cycle the error indication is set (as in circuit protection case).

There are the following diagnosis cases:

1. Under-voltage detection: Monitors if DVCC is below V_{BAT_UV} (typically 6.5V).
2. Antenna frequency error: Diagnosis if the oscillation frequency during transmission is outside the typical tracking range 90 kHz to 160 kHz.
3. Antenna peak current error: Diagnosis if the peak current is greater than the adjusted $I_{A_PEAK} + 15\%$ typically.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Max. | Unit |
|---|------------------------|------|-------------------------|------|
| Ground | VSS | 0 | 0 | V |
| Power ground | DVSS1,2,3 | -0.3 | +0.3 | V |
| Reverse protected battery voltage | DVCC1,2,3 | -0.3 | +44 | V |
| Half-bridge driver output | DRV1,2,3 | -0.3 | DVCC + 0.3 | V |
| Bootstrap | BOOST | -0.3 | DVCC + 6 ⁽²⁾ | V |
| 5-V regulator output | VCC | -0.3 | +7 | V |
| Analog reference input | REXT | -0.3 | VCC + 0.3 | V |
| | RCR | -0.3 | VCC + 0.3 | V |
| Digital test mode | TM1,2,3 | -0.3 | VCC + 0.3 | V |
| DIO interface supply | VDIO | -0.3 | DVCC + 0.3 | V |
| DIO interface | DIO | -0.3 | DVCC + 0.3 | V |
| Zero crossing analog input | SENSE | -2 | DVCC + 0.3 | V |
| Electromagnetic Interference | EMI | | 250 | V/M |
| Minimum ESD protection (100 pF through 1.5 kΩ) | | | 1 (on PCB) | kV |
| Power dissipation | P _{tot} | | 2 ⁽¹⁾ | W |
| Junction temperature | ϑ _j | | 150 | °C |
| Storage temperature | ϑ _{STORE} | -55 | +125 | °C |
| Ambient temperature range under bias | ϑ _{ambient} | -40 | +105 | °C |
| Soldering temperature (10s) | ϑ _{SOLDERING} | | 260 +0/-5 | °C |

Notes: 1. May be limited by external thermal resistance.

2. If the low side driver is switched on, it is not allowed to connect a voltage source to pin BOOST.

6. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|--------------------------------------|-------------------|-------|------|
| Thermal resistance, junction ambient | R _{thJA} | 35 | K/W |

7. Operating Range

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied if not otherwise stated explicitly.

| Parameters | Symbol | Value | Unit |
|-----------------------------|--------------------|-------------|------|
| Operating supply voltage | V _{VBAT1} | 8 to 24 | V |
| Operating temperature range | ϑ _{amb} | -40 to +105 | °C |

8. Noise and Surge Immunity

| Parameter | Test Conditions | Value |
|-------------------------|-----------------|------------------------|
| Conducted interferences | ISO 7637-1 | Level 4 ⁽¹⁾ |

Note: 1. Test pulse 5: $V_{smax} = 45V$

9. Electrical Characteristics⁽¹⁾

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|---|-----------|----------------|------|------|------|-------------|-------|
| 1 | Power Supply | | | | | | | | |
| 1.1 | Main supply voltage | I(VCC) = 10 mA, including load and line regulation | VCC | V_{CC} | 4.7 | 5.0 | 5.3 | V | A |
| 1.2 | Supply current | without antenna load | DVCC | I_{SUPP} | 2 | 10 | 20 | mA | A |
| 1.3 | Standby current | Pin DVCC = 13.5V, $T_{amb} = 90^{\circ}C$ | DVCC | I_{STBY} | 20 | 35 | 60 | μA | B |
| 1.4 | Power-on-reset threshold voltage | | VCC | V_{POR} | 3.5 | 4 | 4.5 | V | A |
| 1.5 | Load dump protection voltage | | DVCC | $VBAT_{LD}$ | 29 | 31 | 35 | V | A |
| 1.6 | Under voltage detection | | DVCC | $VBAT_{UV}$ | 6.0 | 6.5 | 7.0 | V | A |
| 1.7 | Thermal shut down | | | TSD | 150 | 165 | 180 | $^{\circ}C$ | B |
| 1.8 | Protection debounce filter | | | T_{DEB} | 10 | 15 | 25 | μs | A |
| 2 | Half-bridge Driver Stage | | | | | | | | |
| 2.1 | Coil driver resistance low side driver | | DRV, DVSS | RDS_{ONL} | | 0.3 | 0.7 | Ω | A |
| 2.2 | Coil driver resistance high side driver | | DVCC, DRV | RDS_{ONH} | | 0.3 | 0.7 | Ω | A |
| 2.3 | Driver output rise time | 10% to 90% slope time, 0% = DVSS, 100% = DVCC DVCC = 12V (smooth edges) | DRV | $T_{DRV,RISE}$ | 50 | 100 | 150 | ns | D |
| 2.4 | Driver output fall time | 10% to 90% slope time, 0% = DVSS, 100% = DVCC DVCC = 12V (smooth edges) | DRV | $T_{DRV,FALL}$ | 50 | 100 | 150 | ns | D |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. $8V < V(DVCC) < 24V$; $-40^{\circ}C < \vartheta_{amb} < 105^{\circ}C$, unless otherwise specified; all values refer to GND

2. Definition of DC_{DRV} see "Application Hints" on page 14

3. $I_{VDIO, stby} = 7.5 \mu A$ at $T_{amb} = 90^{\circ}C$

9. Electrical Characteristics⁽¹⁾ (Continued)

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|---|------------|------------------|------|-------|------|---------------|-------|
| 3 | Antenna Peak Current Control | | | | | | | | |
| 3.1 | Duty cycle control range | | DRV | $DC_{DRV}^{(2)}$ | 15 | | 85 | % | B |
| 3.2 | Peak current control reference | | RCR | V_{RCR} | 1.15 | 1.215 | 1.28 | V | A |
| 3.3 | Peak current control accuracy | $R_{CR} = 25\text{ k}\Omega$ | | $I_{A_{peak}}$ | 1.0 | 1.3 | 1.8 | A | B |
| 3.4 | Antenna peak under current threshold | 0% NOM value = $I_{A_{acc}}$ $R_{CR} = 25\text{ k}\Omega$ | | $I_{A_{UC}}$ | -30 | -20 | -10 | % | A |
| 3.5 | Antenna peak overcurrent threshold | 0% NOM value = $I_{A_{acc}}$ $R_{CR} = 25\text{ k}\Omega$ | | $I_{A_{OV}}$ | 30 | 20 | 10 | % | A |
| 4 | Oscillator and Phase Control | | | | | | | | |
| 4.1 | VCO initial frequency | Self oscillating mode = half-bridge not activated | | CLK_{SO} | 115 | 125 | 135 | kHz | A |
| 4.2 | VCO frequency tracking range | Tracking frequency mode = half-bridge activated | | CLK_{TR} | 80 | | 200 | kHz | B |
| 4.3 | Phase shift between voltage at DRV and zero crossing of current through SENSE | Antenna resonance frequency range = 100 kHz to 150 kHz, antenna quality = 5 to 50 | DRV, SENSE | ϕ_A | -120 | 0 | +120 | ns | B |
| 4.4 | Phase control set-up time | $-240\text{ ns} \leq \phi_A \leq +240\text{ ns}$ | DRV, SENSE | T_{setup} | | | 160 | μs | D |
| 4.5 | High frequency failure threshold | | DRV | f_{VCOH} | 150 | 160 | 200 | kHz | A |
| 4.6 | Low frequency failure threshold | | DRV | f_{VCOL} | 80 | 90 | 105 | kHz | A |
| 5 | DIO Interface | | | | | | | | |
| 5.1 | VDIO leakage current | Pin VDIO = 13.5V, Pin DIO = 13.5V $T_{amb} \leq 27^\circ\text{C}^{(3)}$ | VDIO | $I_{VDIO,STBY}$ | 2 | 4 | 5 | μA | A |
| 5.2 | DIO leakage current | Pin VDIO = 13.5V, Pin DIO = 13.5V $T_{amb} = 90^\circ\text{C}$ | DIO | $I_{DIO,LEAK}$ | 2 | 4 | 200 | μA | A |
| 5.3 | DIO sink current | | DIO | $I_{DIO,LIMIT}$ | 36 | 44 | 52 | mA | A |
| 5.4 | Output low level | $I_{DIO} = 20\text{ mA}$ | DIO | $V_{DIO,L}$ | | 1.2 | 1.5 | V | A |
| 5.5 | Input low level threshold | 100% = DVCC | DIO | $V_{DIO,THL}$ | 30 | 45 | 70 | %V (VDIO) | A |
| 5.6 | Input high level threshold | 100% = DVCC | DIO | $V_{DIO,TLH}$ | 30 | 50 | 70 | %V (VDIO) | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. $8\text{V} < V(\text{DVCC}) < 24\text{V}$; $-40^\circ\text{C} < \vartheta_{amb} < 105^\circ\text{C}$, unless otherwise specified; all values refer to GND

2. Definition of DC_{DRV} see "Application Hints" on page 14

3. $I_{VDIO,STBY} = 7.5\text{ }\mu\text{A}$ at $T_{amb} = 90^\circ\text{C}$

9. Electrical Characteristics⁽¹⁾ (Continued)

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|--|--|-----|-------------------|------|------|------|--------|-------|
| 6 | Transmission Protocol | | | | | | | | |
| 6.1 | LF data baud rate | | | Bd _{RF} | | 1 | 4 | kbit/s | C, D |
| 6.2 | Anti-bouncing time for activate half-bridge | DIO = H → L, for f _{VCO} = 125 kHz | | T _{DL} | | 64 | | μs | B |
| 6.3 | Anti-bouncing time for de-activate half-bridge | DIO = L → H, for f _{VCO} = 125 kHz | | T _{DH} | | 64 | | μs | B |
| 6.4 | Acknowledge pulse width | | | T _{ACK} | | 256 | | μs | B |
| 6.5 | Error signal pulse width | | | T _{ERR} | | 128 | | μs | B |
| 6.6 | Transmission time out de-activated half-bridge | | | T _{OUTL} | | 16 | | ms | B |
| 6.7 | Transmission time out activated half-bridge | | | T _{OUTH} | | 16 | | ms | |
| 6.8 | Time out reset pulse width | | | T _{OR} | | 32 | | μs | |
| 6.9 | Time out reset pulse period | | | T _{ORP} | | 15 | | ms | |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. $8V < V(DVCC) < 24V$; $-40^{\circ}C < \vartheta_{amb} < 105^{\circ}C$, unless otherwise specified; all values refer to GND

2. Definition of DC_{DRV} see "Application Hints" on page 14

3. I_{V_{DIO},stby} = 7.5 μA at T_{amb} = 90°C

10. External Components

The following external components have to be applied to the circuit for functional operation (see Figure 11-1 on page 15).

| Component | Pin | Min. | Typ. | Max. | Unit |
|--|----------------------|--------------------|---------|------|------|
| C1 | DVCC | | 100/50 | | μF/V |
| D1 standard diode | | | 1.5/50 | | A/V |
| R _{EXT} | REXT | | 100 | | kΩ |
| R _{CR} | RCR ⁽³⁾ | 25 | | 200 | kΩ |
| C3 | VCC | | 10 | | μF |
| C2 | BOOST | 0.68 | 1 | 2 | nF |
| R _{SENSE} | SENSE ⁽¹⁾ | 0.1 ⁽²⁾ | 0.5 | 1 | Ω |
| R _{DIO} | DIO | 0.6 | 1 | 6 | kΩ |
| L _{ANT} antenna inductance | | | 345/2.5 | | μH/Ω |
| R _{ANT} Q-factor adjuster | | | 10 | | Ω |
| C _{ANT} resonant-frequency adjuster | | | 4.7/400 | | nF/V |

Notes: 1. Sensitivity at input SENSE is proportional to resistor R_s times antenna peak current.

2. For antenna peak value 1.5A.

3. Recommended range: R_{CR} = 25 to 100 kΩ

11. Application Hints

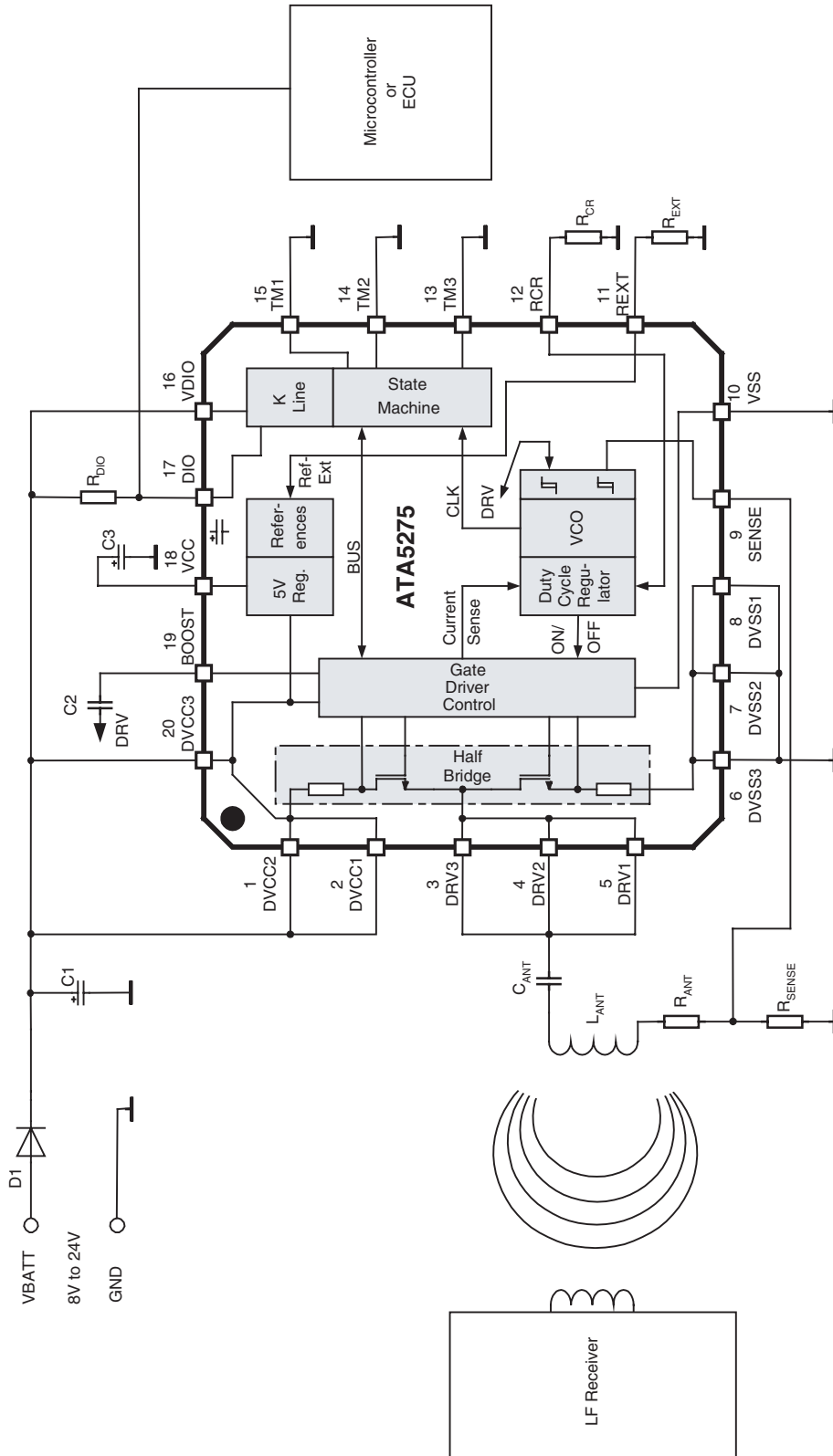
A typical application of ATA5275 is shown in [Figure 11-1 on page 15](#). The peak value of the antenna current can be estimated by the formula:

$$\hat{I}_A = \frac{2}{\pi} \times \frac{V_{DVCC}}{R_A} \times \sin\left(\frac{\pi}{2} \times DC_{DRV}\right) \times \cos\phi_A$$

Here R_A denotes the equivalent series resistance of the driver load, i.e., the external coil series resistance in series with the shunt resistance and the internal drain-source-on-resistance of the NDMOS. The duty cycle DC_{DRV} is the ratio of the driver high-side on-time with respect to the half of the oscillation period.

The phase difference ϕ_A is measured as the time difference between the point of mass of V_{DRV} and the peak value of the antenna current.

Figure 11-1. Application Circuit



Note: For the typical values of the external components, see table "External Components" on page 13.

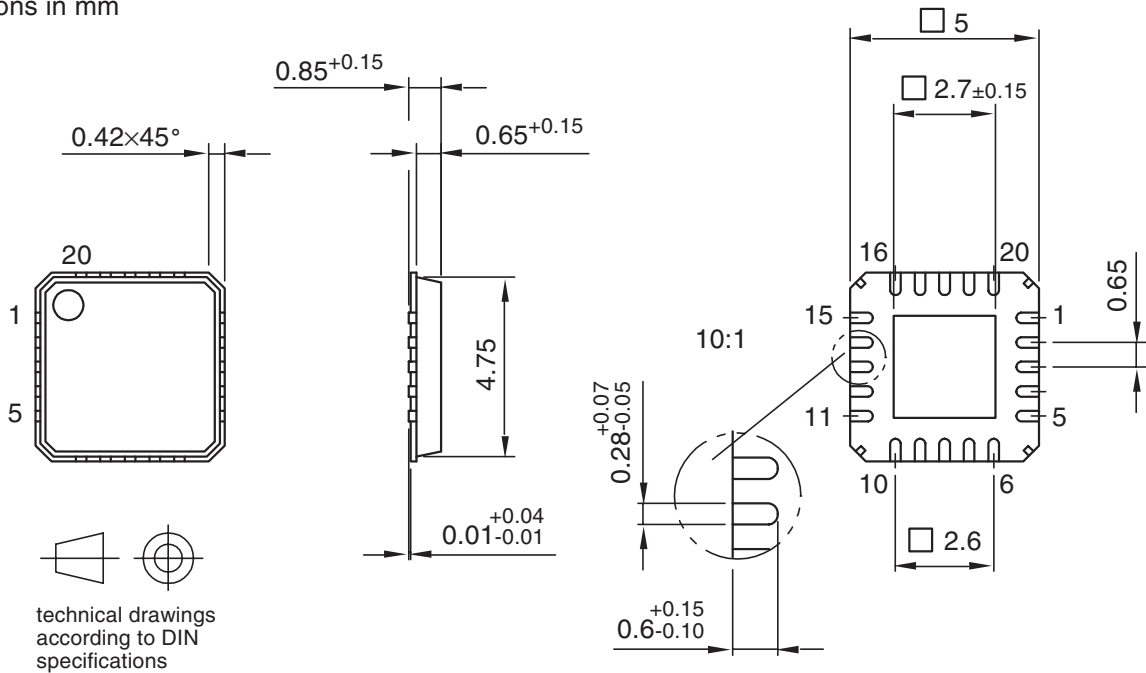
12. Ordering Information

| Extended Type Number | Package | Remarks | Minimum Order Quantity |
|----------------------|--------------------|---------------------------|------------------------|
| ATA5275-PGQI | QFN20, 5 mm × 5 mm | Pb-free, Taped and reeled | 6,000 |
| ATA5275-PGPI | QFN20, 5 mm × 5 mm | Pb-free, Taped and reeled | 1,500 |

13. Package Information

Package: QFN 20 - 5 x 5
 Exposed pad 2.7 x 2.7
 (acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm



Drawing-No.: 6.543-5069.01-4

Issue: 3; 24.01.03

14. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|------------------|--|
| 4739I-AUTO-12/05 | <ul style="list-style-type: none"> Page 1: Pb-free logo deleted Page 15: Application Circuit changed |
| 4739H-AUTO-11/05 | <ul style="list-style-type: none"> Table "Ordering Information" on page 16 changed |
| 4739G-AUTO-09/05 | <ul style="list-style-type: none"> Table "Absolute Maximum Ratings" on page 10 changed |



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