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# AK4127

## 192kHz / 24Bit High Performance Asynchronous SRC

### GENERAL DESCRIPTION

The AK4127 is a stereo digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 216kHz. The output sample rate is from 8kHz to 216kHz. The system can take very simple configuration because the AK4127 has an internal PLL and does not need any master clock at slave mode. The AK4127 is suitable for the application interfacing to different sample rates such as high-end Car Audio and DVD recorder.

### FEATURES

#### 1. SRC

- Asynchronous Sample Rate Converter
- Input Sample Rate Range (fsi): 8kHz ~ 216kHz
- Output Sample Rate (fso): 8kHz ~ 216kHz
- Input to Output Sample Rate Ratio: 1/6 to 6
- THD+N: -130dB
- Dynamic Range: 140dB (A-weighted)
- I/F format: MSB justified, LSB justified, I<sup>2</sup>S compatible and TDM
- PLL for Internal Operation Clock
- Clock for Master mode: 128/192/256/384/512/768fsi, 128/256/384/512/768fso
- SRC Bypass mode (Master/Slave)
- Soft Mute Function

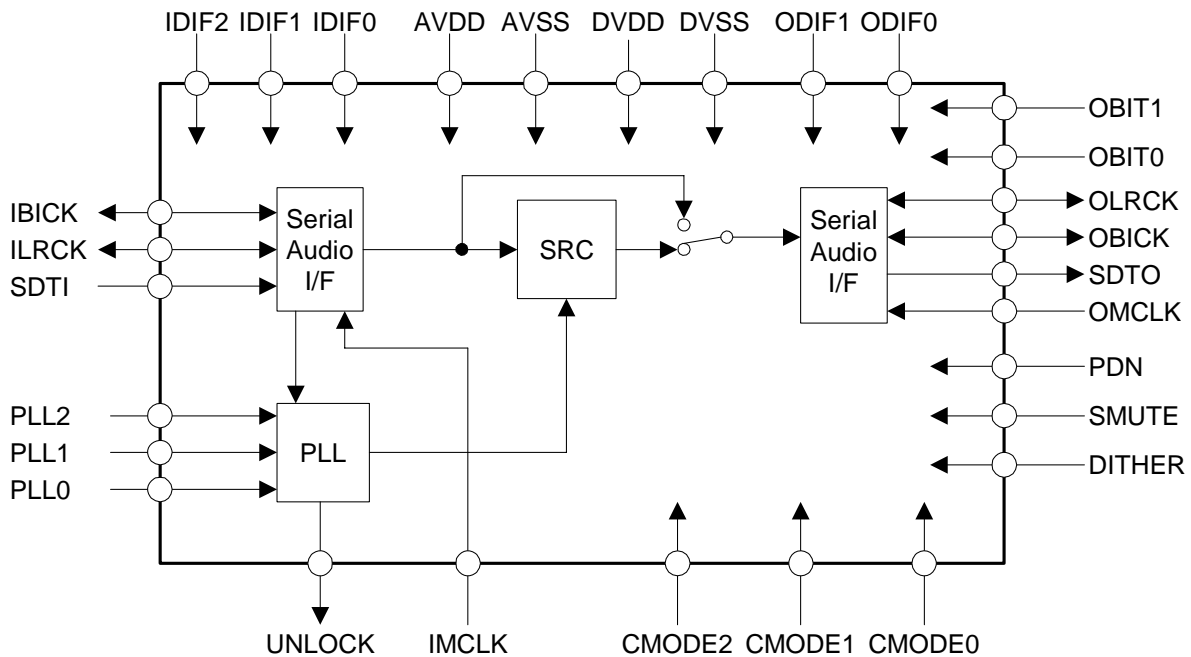
#### 2. Power Supply

- AVDD, DVDD: 3.0 ~ 3.6V (typ. 3.3V)

#### 3. Ta = -40 ~ 85°C

#### 4. Package: 30pin VSOP

#### 5. AK4124/5 Pin-compatible



|                          |
|--------------------------|
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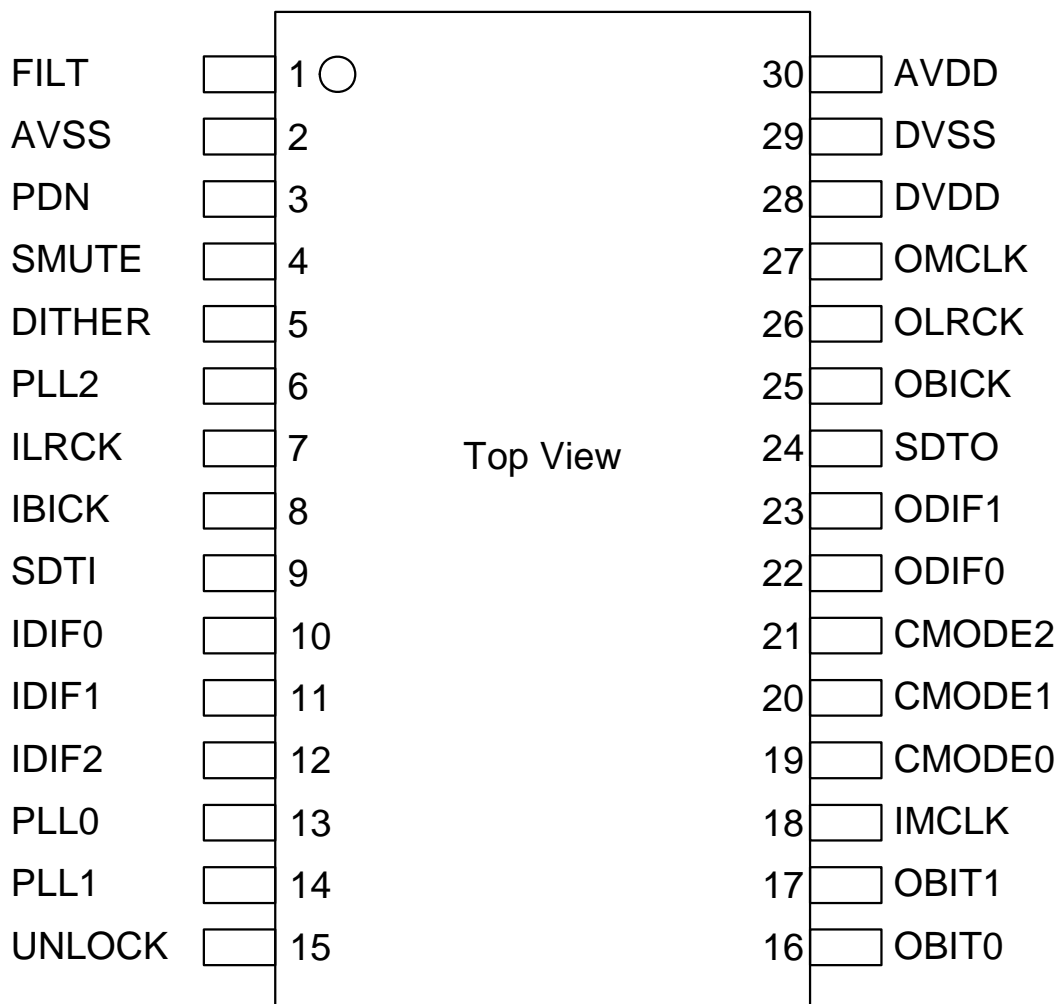
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■ **Ordering Guide**

AK4127VF  
AKD4127

-40 ~ +85°C                      30pin VSOP (0.65mm pitch)  
Evaluation Board for AK4127

■ **Pin Layout**



## ■ Compatibility with AK4125

| Item   | AK4125 | AK4127                                |
|--|--------|---------------------------------------|
| TDM Mode   | -      | X                                     |
| Slave Mode at Bypass Mode                        | -      | X                                     |
| OMCLK pin  | OMCLK  | Normal Mode: OMCLK<br>TDM Mode: TDMIN |
| OMCLK=192fso for Output PORT<br>(at Master Mode) | X      | -                                     |

(-: Not available, X: Available)

| PIN/FUNCTION |          |     |  |
|--------------|----------|-----|--|
| No.          | Pin Name | I/O | Function   |
| 1            | FILT     | O   | PLL Loop Filter Pin, Hi-Z when PDN pin = "L".  |
| 2            | AVSS     | -   | Analog Ground Pin  |
| 3            | PDN      | I   | Power-Down Mode Pin<br>"H": Power up, "L": Power down reset and initializes the control register.  |
| 4            | SMUTE    | I   | Soft Mute Pin<br>"H" : Soft Mute, "L" : Normal Operation   |
| 5            | DITHER   | I   | Dither Enable Pin<br>"H" : Dither ON, "L" : Dither OFF   |
| 6            | PLL2     | I   | PLL Mode Select 2 Pin  |
| 7            | ILRCK    | I/O | Input Channel Clock Pin, Output "L" when PDN = "L" and master mode.  |
| 8            | IBICK    | I/O | Audio Serial Data Clock Pin, Output "L" when PDN = "L" and master mode.  |
| 9            | SDTI     | I   | Audio Serial Data Input Pin  |
| 10           | IDIF0    | I   | Audio Interface Format 0 Pin for Input PORT  |
| 11           | IDIF1    | I   | Audio Interface Format 1 Pin for Input PORT  |
| 12           | IDIF2    | I   | Audio Interface Format 2 Pin for Input PORT  |
| 13           | PLL0     | I   | PLL Mode Select 0 Pin  |
| 14           | PLL1     | I   | PLL Mode Select 1 Pin  |
| 15           | UNLOCK   | O   | Unlock Status Pin, Output "H" when PDN = "L"   |
| 16           | OBIT0    | I   | Bit Length Select 0 Pin for Output Data  |
| 17           | OBIT1    | I   | Bit Length Select 1 Pin for Output Data  |
| 18           | IMCLK    | I   | Master Clock Input Pin for Input PORT  |
| 19           | CMODE0   | I   | Clock Mode Select 0 Pin  |
| 20           | CMODE1   | I   | Clock Mode Select 1 Pin  |
| 21           | CMODE2   | I   | Clock Mode Select 2 Pin  |
| 22           | ODIF0    | I   | Audio Interface Format 0 Pin for Output PORT   |
| 23           | ODIF1    | I   | Audio Interface Format 1 Pin for Output PORT   |
| 24           | SDTO     | O   | Audio Serial Data Output Pin for Output PORT, Output "L" when PDN pin = "L"  |
| 25           | OBICK    | I/O | Audio Serial Data Clock Pin for Output PORT<br>Output "L" when PDN = "L" and master mode.  |
| 26           | OLRCK    | I/O | Output Channel Clock Pin for Output PORT<br>Output "L" when PDN = "L" and master mode.   |
| 27           | OMCLK    | I   | Master Clock/TDM Data Input Pin for Output PORT<br>OMCLK: Master Clock Input Pin (except for PLL2/1/0 pin = "L/H/H")<br>TDMIN: TDM Data Input Pin (PLL2/1/0 pin = "L/H/H") |
| 28           | DVDD     | -   | Digital Power Supply Pin, 3.0 ~ 3.6V   |
| 29           | DVSS     | -   | Digital Ground Pin   |
| 30           | AVDD     | -   | Analog Power Supply Pin, 3.0 ~ 3.6V  |

Note: All input pins must not be left floating.

## ■ Handling of Unused pins

The unused digital I/O pins should be processed appropriately as below.

| Classification | Pin Name      | Setting   |
|----------------|---------------|---|
| Analog         | FILT          | This pin should be open.                              |
| Digital        | SMUTE, DITHER | These pins should be connected to DVSS.               |
|                | IMCLK, OMCLK  | These pins should be connected to DVSS in slave mode. |
|                | UNLOCK        | This pin should be open.                              |

### ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V; Note 1)

| Parameter                              |                       | Symbol       | min  | max      | Units |
|--|-----------------------|--------------|------|----------|-------|
| Power Supplies:                        | Analog                | AVDD         | -0.3 | 4.6      | V     |
|  | Digital               | DVDD         | -0.3 | 4.6      | V     |
|  | AVSS – DVSS  (Note 2) | $\Delta$ GND | -    | 0.3      | V     |
| Input Current, Any Pin Except Supplies |                       | IIN          | -    | $\pm$ 10 | mA    |
| Digital Input Voltage (Note 3)         |                       | VIND         | -0.3 | DVDD+0.3 | V     |
| Ambient Temperature (Power applied)    |                       | Ta           | -40  | 85       | °C    |
| Storage Temperature                    |                       | Tstg         | -65  | 150      | °C    |

Note 1. All voltages with respect to ground.

Note 2. AVSS, BVSS and DVSS must be connected to the same ground.

Note 3. PND, SMUTE, DITHER, PLL2, ILRCK, IBICK, SDTI, IDIF0, IDIF1, IDIF2, PLL0, PLL1, OBIT0, OBIT1, IMCLK, CMODE0, CMODE1, CMODE2, ODIF0, ODIF1, OBICK, OLRCK and OMCLK

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

### RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=0V; Note 1)

| Parameter                  |         | Symbol | min | typ | max  | Units |
|----------------------------|---------|--------|-----|-----|------|-------|
| Power Supplies<br>(Note 4) | Analog  | AVDD   | 3.0 | 3.3 | 3.6  | V     |
|                            | Digital | DVDD   | 3.0 | 3.3 | AVDD | V     |

Note 4. The power up sequence between AVDD and DVDD is not important.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

|                            |
|----------------------------|
| <b>SRC CHARACTERISTICS</b> |
|----------------------------|

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=DVSS=0V; data = 24bit; measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

| Parameter  | Symbol  | min | typ  | max | Units |
|--|---------|-----|------|-----|-------|
| <b>SRC Characteristics:</b>  |         |     |      |     |       |
| Resolution   |         |     |      | 24  | Bits  |
| Input Sample Rate  | FSI     | 8   |      | 216 | kHz   |
| Output Sample Rate   | FSO     | 8   |      | 216 | kHz   |
| THD+N (Input = 1kHz, 0dBFS, <a href="#">Note 5</a> )                       |         |     |      |     |       |
| FSO/FSI = 44.1kHz/48kHz  |         | -   | -130 | -   | dB    |
| FSO/FSI = 48kHz/44.1kHz  |         | -   | -124 | -   | dB    |
| FSO/FSI = 48kHz/192kHz   |         | -   | -133 | -   | dB    |
| FSO/FSI = 192kHz/48kHz   |         | -   | -124 | -   | dB    |
| Worst Case (FSO/FSI = 32kHz/176.4kHz)                                      |         | -   | -    | -91 | dB    |
| Dynamic Range (Input = 1kHz, -60dBFS, <a href="#">Note 5</a> )             |         |     |      |     |       |
| FSO/FSI = 44.1kHz/48kHz  |         | -   | 136  | -   | dB    |
| FSO/FSI = 48kHz/44.1kHz  |         | -   | 136  | -   | dB    |
| FSO/FSI = 48kHz/192kHz   |         | -   | 136  | -   | dB    |
| FSO/FSI = 192kHz/48kHz   |         | -   | 132  | -   | dB    |
| Worst Case (FSO/FSI = 48kHz/32kHz)   |         | 132 | -    | -   | dB    |
| Dynamic Range (Input = 1kHz, -60dBFS, A-weighted, <a href="#">Note 5</a> ) |         |     |      |     |       |
| FSO/FSI = 44.1kHz/48kHz  |         | -   | 140  | -   | dB    |
| Ratio between Input and Output Sample Rate                                 | FSO/FSI | 1/6 |      | 6   | -     |

Note 5. Measured by Audio Precision System Two Cascade



|                               |
|-------------------------------|
| <b>FILTER CHARACTERISTICS</b> |
|-------------------------------|

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

| Parameter                |                          | Symbol | min       | typ | max       | Units |
|--------------------------|--------------------------|--------|-----------|-----|-----------|-------|
| <b>Digital Filter</b>    |                          |        |           |     |           |       |
| Passband -0.01dB         | 0.985 ≤ FSO/FSI ≤ 6.000  | PB     | 0         |     | 0.4583FSI | kHz   |
|                          | 0.905 ≤ FSO/FSI < 0.985  | PB     | 0         |     | 0.4167FSI | kHz   |
|                          | 0.714 ≤ FSO/FSI < 0.905  | PB     | 0         |     | 0.3195FSI | kHz   |
|                          | 0.656 ≤ FSO/FSI < 0.714  | PB     | 0         |     | 0.2852FSI | kHz   |
|                          | 0.536 ≤ FSO/FSI < 0.656  | PB     | 0         |     | 0.2182FSI | kHz   |
|                          | 0.492 ≤ FSO/FSI < 0.536  | PB     | 0         |     | 0.2177FSI | kHz   |
|                          | 0.452 ≤ FSO/FSI < 0.492  | PB     | 0         |     | 0.1948FSI | kHz   |
|                          | 0.357 ≤ FSO/FSI < 0.452  | PB     | 0         |     | 0.1458FSI | kHz   |
|                          | 0.324 ≤ FSO/FSI < 0.357  | PB     | 0         |     | 0.1302FSI | kHz   |
|                          | 0.246 ≤ FSO/FSI < 0.324  | PB     | 0         |     | 0.0917FSI | kHz   |
|                          | 0.226 ≤ FSO/FSI < 0.246  | PB     | 0         |     | 0.0826FSI | kHz   |
|                          | 0.1667 ≤ FSO/FSI < 0.226 | PB     | 0         |     | 0.0583FSI | kHz   |
| Stopband                 | 0.985 ≤ FSO/FSI ≤ 6.000  | SB     | 0.5417FSI |     |           | kHz   |
|                          | 0.905 ≤ FSO/FSI < 0.985  | SB     | 0.5021FSI |     |           | kHz   |
|                          | 0.714 ≤ FSO/FSI < 0.905  | SB     | 0.3965FSI |     |           | kHz   |
|                          | 0.656 ≤ FSO/FSI < 0.714  | SB     | 0.3643FSI |     |           | kHz   |
|                          | 0.536 ≤ FSO/FSI < 0.656  | SB     | 0.2974FSI |     |           | kHz   |
|                          | 0.492 ≤ FSO/FSI < 0.536  | SB     | 0.2813FSI |     |           | kHz   |
|                          | 0.452 ≤ FSO/FSI < 0.492  | SB     | 0.2604FSI |     |           | kHz   |
|                          | 0.357 ≤ FSO/FSI < 0.452  | SB     | 0.2116FSI |     |           | kHz   |
|                          | 0.324 ≤ FSO/FSI < 0.357  | SB     | 0.1969FSI |     |           | kHz   |
|                          | 0.246 ≤ FSO/FSI < 0.324  | SB     | 0.1573FSI |     |           | kHz   |
|                          | 0.226 ≤ FSO/FSI < 0.246  | SB     | 0.1471FSI |     |           | kHz   |
|                          | 0.1667 ≤ FSO/FSI < 0.226 | SB     | 0.1020FSI |     |           | kHz   |
| Passband Ripple          |                          | PR     |           |     | ±0.01     | dB    |
| Stopband Attenuation     | 0.985 ≤ FSO/FSI ≤ 6.000  | SA     | 121.2     |     |           | dB    |
|                          | 0.905 ≤ FSO/FSI < 0.985  | SA     | 121.4     |     |           | dB    |
|                          | 0.714 ≤ FSO/FSI < 0.905  | SA     | 115.3     |     |           | dB    |
|                          | 0.656 ≤ FSO/FSI < 0.714  | SA     | 116.9     |     |           | dB    |
|                          | 0.536 ≤ FSO/FSI < 0.656  | SA     | 114.6     |     |           | dB    |
|                          | 0.492 ≤ FSO/FSI < 0.536  | SA     | 100.2     |     |           | dB    |
|                          | 0.452 ≤ FSO/FSI < 0.492  | SA     | 103.3     |     |           | dB    |
|                          | 0.357 ≤ FSO/FSI < 0.452  | SA     | 102.0     |     |           | dB    |
|                          | 0.324 ≤ FSO/FSI < 0.357  | SA     | 103.6     |     |           | dB    |
|                          | 0.246 ≤ FSO/FSI < 0.324  | SA     | 104.0     |     |           | dB    |
| 0.226 ≤ FSO/FSI < 0.246  | SA                       | 103.3  |           |     | dB        |       |
| 0.1667 ≤ FSO/FSI < 0.226 | SA                       | 73.2   |           |     | dB        |       |
| Group Delay              | (Note 6)                 | GD     | -         | 56  | -         | 1/fs  |

Note 6. This delay is the a period from the rising edge of ILRCK, just after the data is input, to the rising edge of OLRCK, just after the data is output, when there is no phase difference between ILRCK and OLRCK.

|                           |
|---------------------------|
| <b>DC CHARACTERISTICS</b> |
|---------------------------|

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V)

| Parameter                                     | Symbol | min      | typ | max     | Units |
|---|--------|----------|-----|---------|-------|
| High-Level Input Voltage                      | VIH    | 70%DVDD  | -   | -       | V     |
| Low-Level Input Voltage                       | VIL    | -        | -   | 30%DVDD | V     |
| High-Level Output Voltage (Iout=-400μA)       | VOH    | DVDD-0.4 | -   | -       | V     |
| Low-Level Output Voltage (Iout=400μA)         | VOL    | -        | -   | 0.4     | V     |
| Input Leakage Current                         | Iin    | -        | -   | ±10     | μA    |
| <b>Power Supplies</b>                         |        |          |     |         |       |
| Power Supply Current                          |        |          |     |         |       |
| Normal operation (PDN pin = "H")              |        |          |     |         |       |
| FSI=FSO=48kHz at Slave Mode: AVDD=DVDD=3.3V   |        |          | 15  |         | mA    |
| FSI=FSO=192kHz at Master Mode: AVDD=DVDD=3.3V |        |          | 65  |         | mA    |
| : AVDD=DVDD=3.6V                              |        |          |     | 100     | mA    |
| Power down (PDN pin = "L") (Note 7)           |        |          |     |         |       |
| AVDD+DVDD                                     |        |          | 10  | 100     | μA    |

Note 7. All digital input pins are held DVSS.

|                                  |
|----------------------------------|
| <b>SWITCHING CHARACTERISTICS</b> |
|----------------------------------|

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V; CL=20pF)

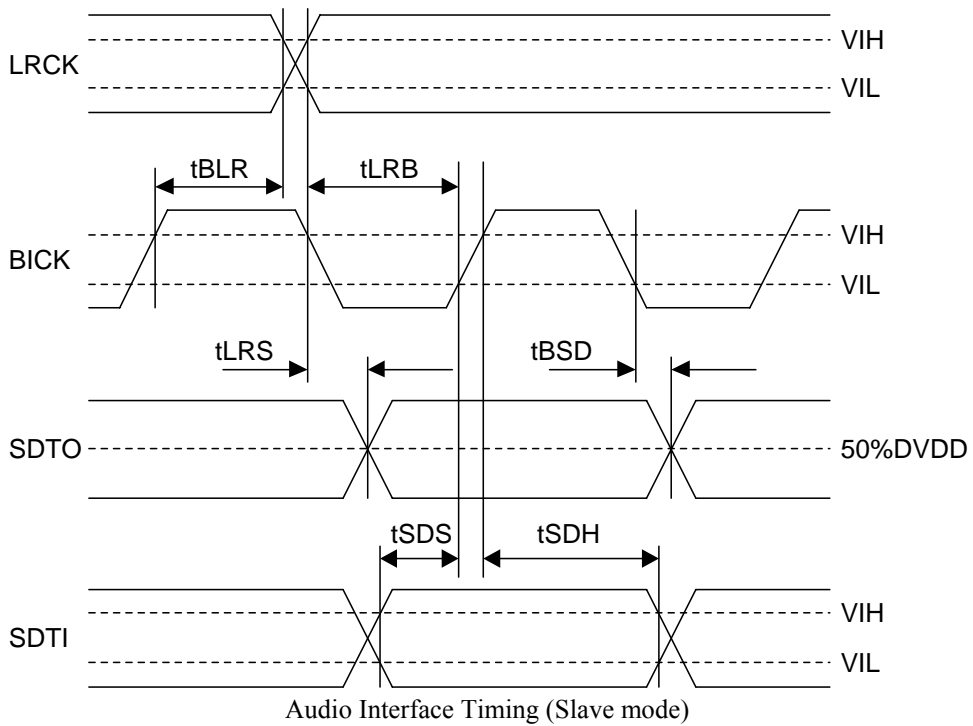
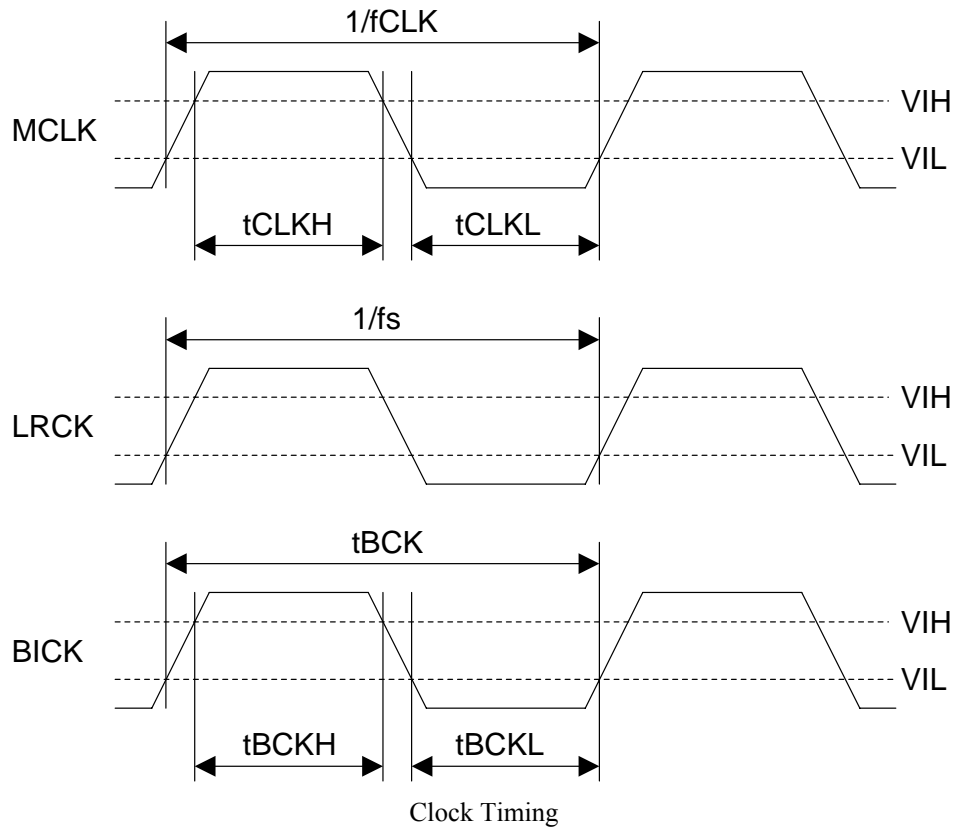
| Parameter                           | Symbol | min      | typ | max    | Units |
|-------------------------------------|--------|----------|-----|--------|-------|
| <b>Master Clock Timing</b>          |        |          |     |        |       |
| Frequency                           | fCLK   | 1.024    |     | 41.472 | MHz   |
| Pulse Width Low                     | tCLKL  | 0.4/fCLK |     |        | ns    |
| Pulse Width High                    | tCLKH  | 0.4/fCLK |     |        | ns    |
| <b>LRCK for Input data (ILRCK)</b>  |        |          |     |        |       |
| Frequency                           | fs     | 8        |     | 216    | kHz   |
| Duty Cycle                          | Duty   | 48       | 50  | 52     | %     |
|                                     | Duty   |          | 50  |        | %     |
| <b>LRCK for Output data (OLRCK)</b> |        |          |     |        |       |
| Frequency                           | fs     | 8        |     | 216    | kHz   |
| Duty Cycle                          | Duty   | 48       | 50  | 52     | %     |
|                                     | Duty   |          | 50  |        | %     |
| <b>LRCK for TDM Mode (OLRCK)</b>    |        |          |     |        |       |
| Frequency                           | fs     | 8        |     | 48     | kHz   |
| "H" time                            | tLRH   | 1/256fs  |     |        | ns    |
| "L" time                            | tLRL   | 1/256fs  |     |        | ns    |
| <b>Audio Interface Timing</b>       |        |          |     |        |       |
| <b>Input PORT (Slave mode)</b>      |        |          |     |        |       |
| IBICK Period (8kHz ~ 54kHz)         | tBCK   | 1/256fs  |     |        | ns    |
| (54kHz ~ 108kHz)                    | tBCK   | 1/128fs  |     |        | ns    |
| (108kHz ~ 216kHz)                   | tBCK   | 1/64fs   |     |        | ns    |
| IBICK Pulse Width Low               | tBCKL  | 27       |     |        | ns    |
| Pulse Width High                    | tBCKH  | 27       |     |        | ns    |
| ILRCK Edge to IBICK "↑" (Note 8)    | tLRB   | 15       |     |        | ns    |
| IBICK "↑" to ILRCK Edge (Note 8)    | tBLR   | 15       |     |        | ns    |
| SDTI Hold Time from IBICK "↑"       | tSDH   | 15       |     |        | ns    |
| SDTI Setup Time to IBICK "↑"        | tSDS   | 15       |     |        | ns    |

|  |       |         |      |    |    |
|--|-------|---------|------|----|----|
| <b>Input PORT (Master mode)</b>                    |       |         |      |    |    |
| IBICK Frequency                                    | fBCK  |         | 64fs |    | Hz |
| IBICK Duty   | dBCK  |         | 50   |    | %  |
| IBICK “↓” to ILRCK                                 | tMBLR | -20     |      | 20 | ns |
| SDTI Hold Time from IBICK “↑”                      | tSDH  | 15      |      |    | ns |
| SDTI Setup Time to IBICK “↑”                       | tSDS  | 15      |      |    | ns |
| <b>Output PORT (Slave mode)</b>                    |       |         |      |    |    |
| OBICK Period (8kHz ~ 54kHz)                        | tBCK  | 1/256fs |      |    | ns |
| (54kHz ~ 108kHz)                                   | tBCK  | 1/128fs |      |    | ns |
| (108kHz ~ 216kHz)                                  | tBCK  | 1/64fs  |      |    | ns |
| OBICK Pulse Width Low                              | tBCKL | 27      |      |    | ns |
| Pulse Width High                                   | tBCKH | 27      |      |    | ns |
| OLRCK Edge to OBICK “↑” (Note 8)                   | tLRB  | 20      |      |    | ns |
| OBICK “↑” to OLRCK Edge (Note 8)                   | tBLR  | 20      |      |    | ns |
| OLRCK to SDTO (MSB) (Except I <sup>2</sup> S mode) | tLRS  |         |      | 20 | ns |
| OBICK “↓” to SDTO                                  | tBSD  |         |      | 20 | ns |
| <b>Output PORT (TDM slave mode)</b>                |       |         |      |    |    |
| OBICK Period                                       | tBCK  | 81      |      |    | ns |
| OBICK Pulse Width Low                              | tBCKL | 32      |      |    | ns |
| Pulse Width High                                   | tBCKH | 32      |      |    | ns |
| OLRCK Edge to BICK “↑” (Note 8)                    | tLRB  | 20      |      |    | ns |
| OBICK “↑” to LRCK Edge (Note 8)                    | tBLR  | 20      |      |    | ns |
| OBICK “↓” to SDTO                                  | tBSD  |         |      | 20 | ns |
| TDMIN Hold Time                                    | tSDH  | 20      |      |    | ns |
| TDMIN Setup Time                                   | tSDS  | 10      |      |    | ns |
| <b>Output PORT (Master mode)</b>                   |       |         |      |    |    |
| OBICK Frequency                                    | fBCK  |         | 64fs |    | Hz |
| OBICK Duty   | dBCK  |         | 50   |    | %  |
| OBICK “↓” to OLRCK                                 | tMBLR | -20     |      | 20 | ns |
| OBICK “↓” to SDTO                                  | tBSD  | -20     |      | 20 | ns |
| <b>Reset Timing</b>                                |       |         |      |    |    |
| PDN Pulse Width (Note 9)                           | tPD   | 150     |      |    | ns |

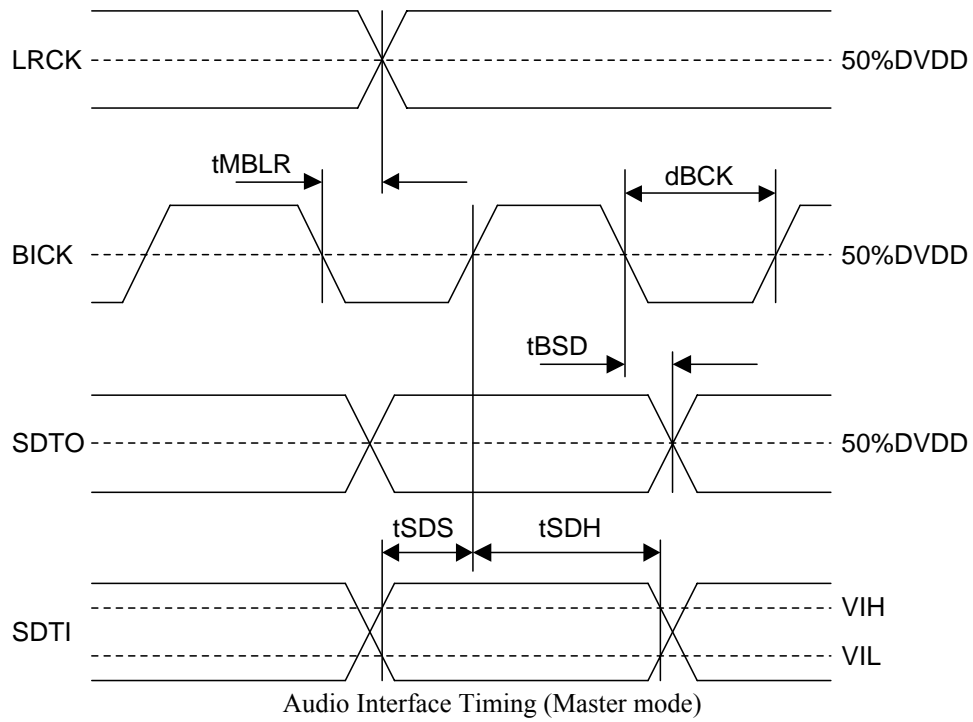
Note 8. BICK rising edge must not occur at the same time as LRCK edge.

Note 9. The AK4127 can be reset by bringing the PDN pin = “L”.

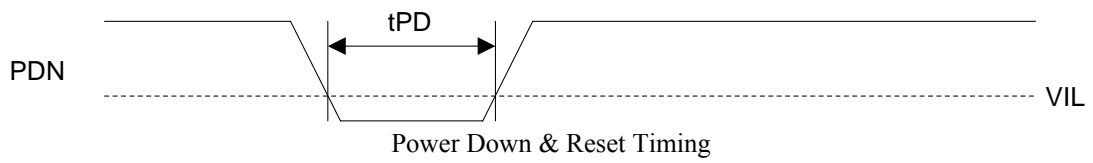
■ Timing Diagram



Note : BICK shows IBICK and OBICK, LRCK shows ILRCK and OLRCK.



Note : BICK shows IBICK and OBICK, LRCK shows ILRCK and OLRCK.



|                           |
|---------------------------|
| <b>OPERATION OVERVIEW</b> |
|---------------------------|

### ■ System Clock & Audio Interface Format for Input PORT

The input port works in master mode or slave mode. An internal system clock is created by the internal PLL using ILRCK (Mode 0 ~ 3 of Table 2) or IBICK (Mode 4 ~ 7 of Table 2) in slave mode. The MCLK is not needed in slave mode. And an internal system clock is created by IMCLK (Mode 8 ~ 15 of Table 2) in master mode. The PLL2-0 pins and IDIF2-0 pins select the master/slave and PLL mode. The PLL2-0 pins and IDIF2-0 pins should be controlled when the PDN pin = "L". When the PLL2-0 pin = "L/H/H", setting the output port slave (CMODE2-0pin = "H/L/L" or "H/H/L") enables the TDM mode at the output port.

The IDIF2-0 pins select the audio interface format for the input port. The audio data is MSB first, 2's compliment format. The SDTI is latched on the rising edge of IBICK. Select the audio interface format when the PDN pin = "L". When in BYPASS mode, both IBICK and OBICK are fixed to 64fs.

| Mode | IDIF2 | IDIF1 | IDIF0 | SDTI Format                           | ILRCK  | IBICK  | IBICK Freq       | Master / Slave |
|------|-------|-------|-------|---------------------------------------|--------|--------|------------------|----------------|
| 0    | L     | L     | L     | 16bit, LSB justified                  | Input  | Input  | ≥ 32fsi          | Slave          |
| 1    | L     | L     | H     | 20bit, LSB justified                  |        |        | ≥ 40fsi          |                |
| 2    | L     | H     | L     | 24/20bit, MSB justified               |        |        | ≥ 48fsi          |                |
| 3    | L     | H     | H     | 24/16bit, I <sup>2</sup> S Compatible |        |        | ≥ 48fsi or 32fsi |                |
| 4    | H     | L     | L     | 24bit, LSB justified                  |        |        | ≥ 48fsi          |                |
| 5    | H     | L     | H     | 24bit, MSB justified                  | Output | Output | 64fs             | Master         |
| 6    | H     | H     | L     | 24bit, I <sup>2</sup> S Compatible    |        |        | 64fs             |                |
| 7    | H     | H     | H     | Reserved                              |        |        |                  |                |

Table 1. Input Audio Interface Format (Input PORT)

| Mode | Master / Slave  | PLL2 | PLL1 | PLL0  | ILRCK Freq             | IBICK Freq                     | IMCLK                 | SMUTE (Note 14) |
|------|---|------|------|-------|------------------------|--------------------------------|-----------------------|-----------------|
| 0    | Slave<br>IMCLK = DVSS<br>IBICK = Input<br>ILRCK = Input     | L    | L    | L     | 8k ~ 96kHz             | Depending on IDIF2-0 (Note 11) | Not needed. (Note 13) | Manual          |
| 1    |   | L    | L    | H     | 8k ~ 216kHz            |                                |                       |                 |
| 2    |   | L    | H    | L     | 16k ~ 216kHz (Note 10) |                                |                       |                 |
| 3    |   | L    | H    | H     |                        |                                |                       | Manual          |
| 4    |   | H    | L    | L     | 8k ~ 216kHz (Note 11)  | 32fsi (Note 12)                | Not needed. (Note 13) | Manual          |
| 5    |   | H    | L    | H     |                        | 64fsi                          |                       |                 |
| 6    |   | H    | H    | L     |                        | 128fsi                         |                       |                 |
| 7    | H   | H    | H    | 64fsi |                        |                                |                       |                 |
| 8    | Master<br>IMCLK = Input<br>IBICK = Output<br>ILRCK = Output | L    | L    | L     | 8k ~ 216kHz            | 64fsi                          | 128fsi                | Manual          |
| 9    |   | L    | L    | H     | 8k ~ 108kHz            |                                | 256fsi                |                 |
| 10   |   | L    | H    | L     | 8k ~ 54kHz             |                                | 512fsi                | Semi-Auto       |
| 11   |   | L    | H    | H     | 8k ~ 216kHz            |                                | 128fsi                |                 |
| 12   |   | H    | L    | L     | 8k ~ 216kHz            |                                | 192fsi                | Manual          |
| 13   |   | H    | L    | H     | 8k ~ 108kHz            |                                | 384fsi                |                 |
| 14   |   | H    | H    | L     | 8k ~ 54kHz             |                                | 768fsi                |                 |
| 15   |   | H    | H    | H     | 8k ~ 216kHz            |                                | 192fsi                |                 |

Table 2. PLL Setting (Input PORT)

Note 10. PLL lock rage is changed by the value of R and C connected FILT pin. Refer to "PLL Loop Filter".

Note 11. The IBCIK must be continuous except when the clocks are changed.

Note 12. IBCIK = 32fsi is supported only 16bit LSB justified and I<sup>2</sup>S Compatible.

Note 13. Fixed to DVSS.

Note 14. Refer to "Soft Mute Operation" for Manual mode and Semi-Auto mode.

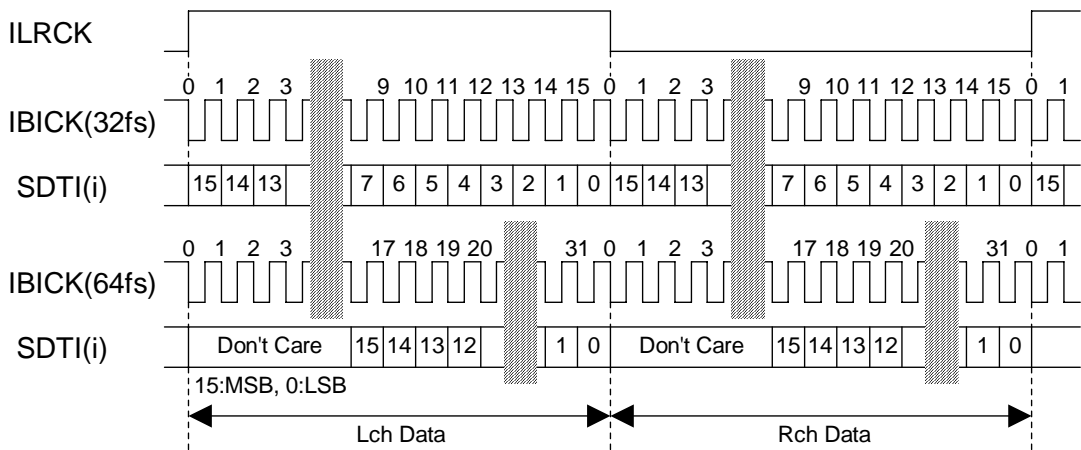


Figure 1. Mode 0 Timing

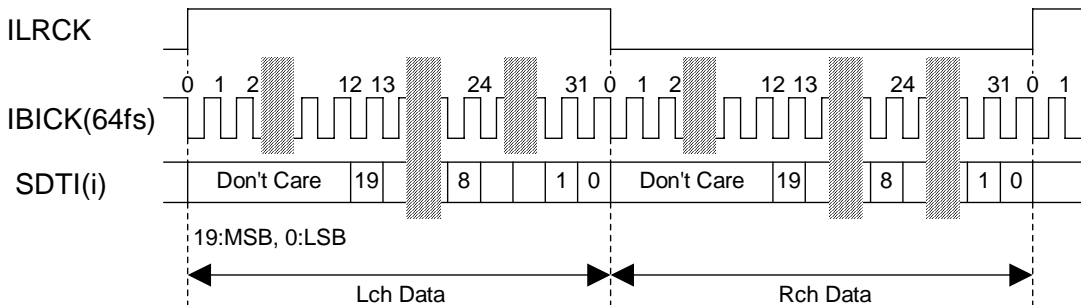


Figure 2. Mode 1 Timing

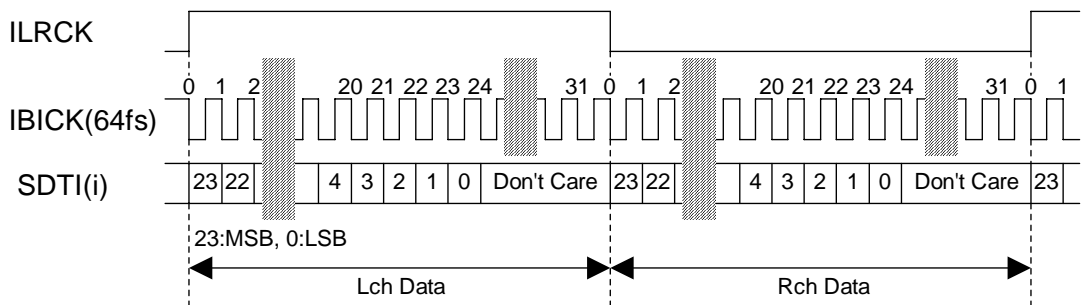


Figure 3. Mode 2,5 Timing (24bit MSB)

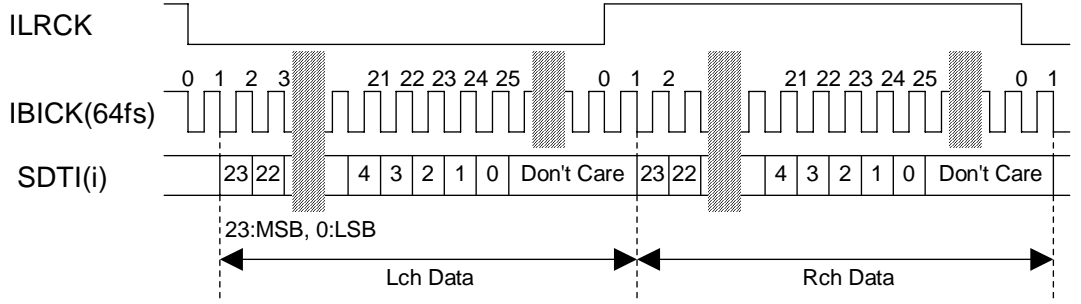


Figure 4. Mode 3, 6 Timing (24bit I<sup>2</sup>S)

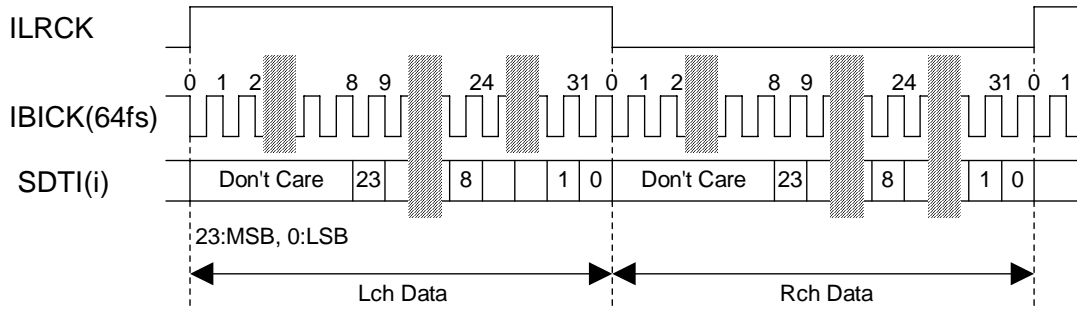


Figure 5. Mode 4 Timing

■ System Clock & Audio Interface Format for Output PORT

The output port works in master mode or slave mode. The MCLK is not needed in slave mode. The CMODE2-0 pins select the master/slave and bypass mode. The CMODE2-0 pins should be controlled when the PDN pin = “L”.

The ODIF1-0 pins and OBIT1-0 pins select the audio interface format for the output port. The audio data is MSB first, 2’s compliment format. The SDTO is clocked out on the falling edge of OBICK. Select the audio interface format when the PDN pin = “L”.

When in BYPASS mode, both IBICK and OBICK are fixed to 64fs. When the PLL2-0 pin= “L/H/H”, setting the output port slave (CMODE2-0pin = “H/L/L” or “H/H/L”) enables the TDM mode at the output port. The OMCLK pin changes to TDMIN pin for TDM data input in TDM mode.

| Mode | CMODE 2 | CMODE 1 | CMODE0 | Master / Slave  | OMCLK                               | fso         |
|------|---------|---------|--------|-----------------|-------------------------------------|-------------|
| 0    | L       | L       | L      | Master          | 256fso                              | 8k ~ 108kHz |
| 1    | L       | L       | H      | Master          | 384fso                              | 8k ~ 108kHz |
| 2    | L       | H       | L      | Master          | 512fso                              | 8k ~ 54kHz  |
| 3    | L       | H       | H      | Master          | 768fso                              | 8k ~ 54kHz  |
| 4    | H       | L       | L      | Slave           | Not used. Set to DVSS.<br>(Note 15) | 8k ~ 216kHz |
| 5    | H       | L       | H      | Master          | 128fso                              | 8k ~ 216kHz |
| 6    | H       | H       | L      | Slave (Bypass)  | Not used. Set to DVSS.<br>(Note 15) | 8k ~ 216kHz |
| 7    | H       | H       | H      | Master (Bypass) | Not used. Set to DVSS.              | 8k ~ 216kHz |

Note 15. Changed to TDMIN pin when PLL2-0 pins = “L/H/H”.

Table 3. Master/Slave Control (Output PORT)

| Mode | ODIF1 | ODIF0 | SDTO Format                 |
|------|-------|-------|-----------------------------|
| 0    | L     | L     | LSB justified               |
| 1    | L     | H     | (Reserved)                  |
| 2    | H     | L     | MSB justified               |
| 3    | H     | H     | I <sup>2</sup> S Compatible |

Table 4. Output Audio Interface Format 1 (Output PORT)



| Mode | Master / Slave                                   | OBIT1 | OBIT0 | SDTO  | OLRCK  | OBICK  | OBICK Frequency                 |               |
|------|--|-------|-------|-------|--------|--------|---------------------------------|---------------|
|      |  |       |       |       |        |        | MSB justified, I <sup>2</sup> S | LSB justified |
| 0    | Slave<br>CMODE2-0 =<br>“HLL” or “HHL”            | L     | L     | 16bit | Input  | Input  | ≥ 32fso                         | 64fso         |
| 1    |  | L     | H     | 18bit |        |        | ≥ 36fso                         |               |
| 2    |  | H     | L     | 20bit |        |        | ≥ 40fso                         |               |
| 3    |  | H     | H     | 24bit |        |        | ≥ 48fso                         |               |
| 4    | Master<br>Except<br>CMODE2-0 =<br>“HLL” or “HHL” | L     | L     | 16bit | Output | Output | 64fso                           |               |
| 5    |  | L     | H     | 18bit |        |        |                                 |               |
| 6    |  | H     | L     | 20bit |        |        |                                 |               |
| 7    |  | H     | H     | 24bit |        |        |                                 |               |

Table 5. Output Audio Interface Format 2 (Output PORT)

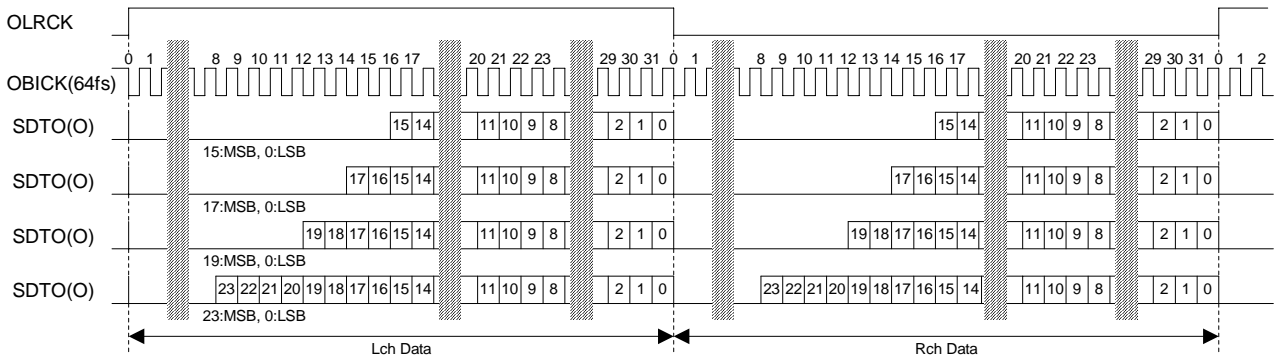


Figure 6. Normal Mode LSB Timing

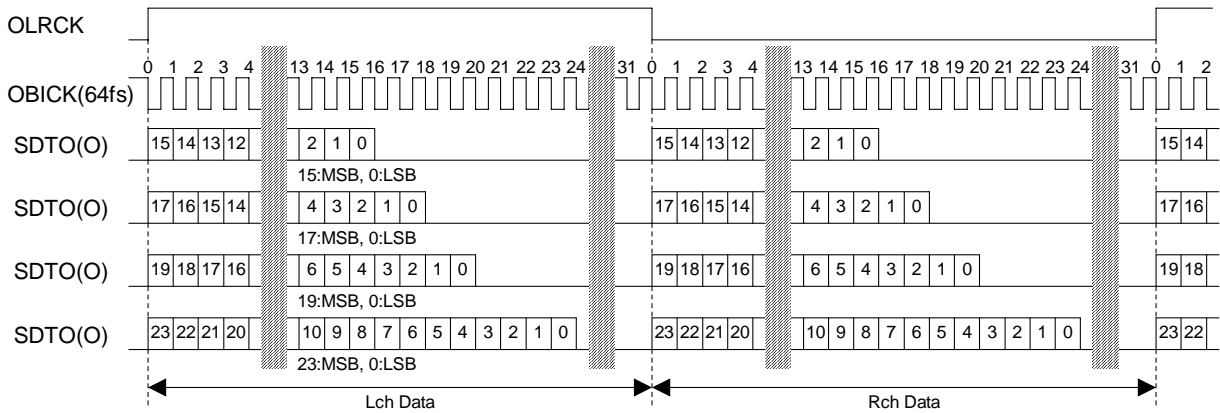


Figure 7. Normal Mode MSB Timing

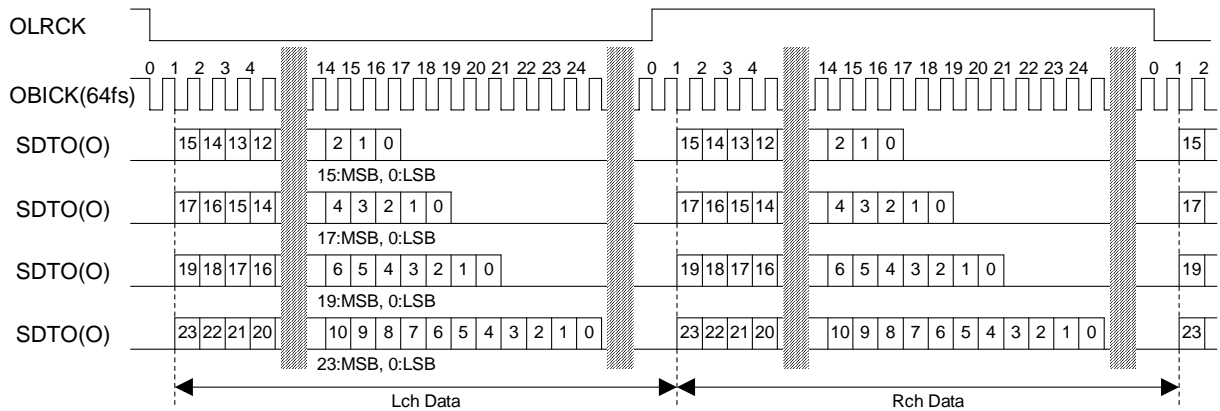


Figure 8. Normal Mode I<sup>2</sup>S Compatible Timing

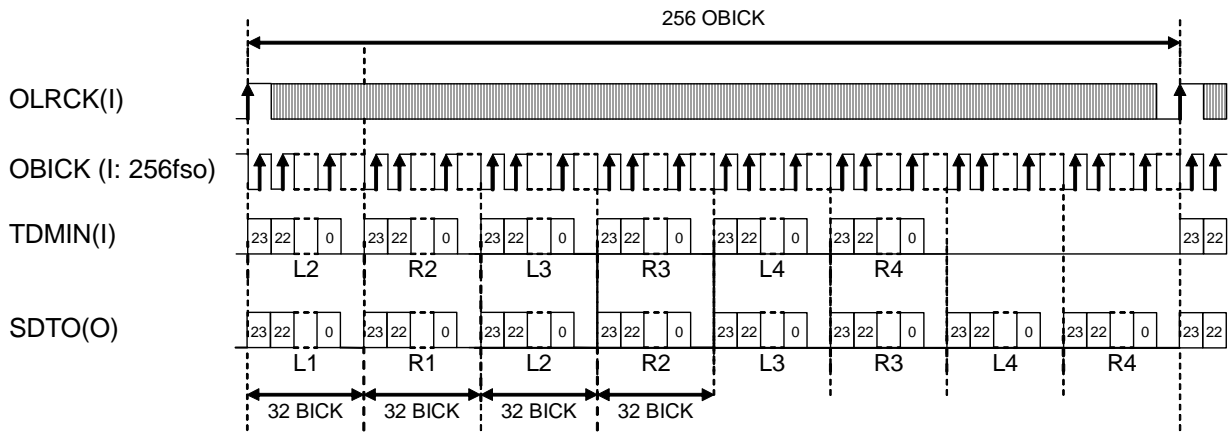


Figure 9. TDM mode MSB Timing

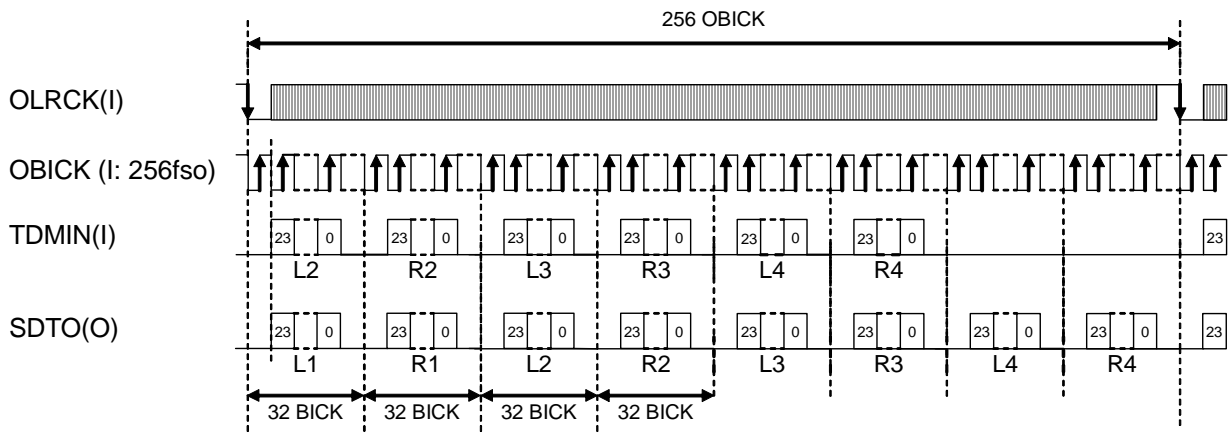


Figure 10. TDM mode I<sup>2</sup>S Compatible Timing

■ Cascade TDM Mode

The AK4127 supports cascading connection of up to four devices (8channels) in a daisy chain configuration at TDM mode. In this mode, the SDTO pin of device #N is connected to TDMIN pin of device #(N+1). The device can output up to 8ch TDM data multiplexed with TDMIN data. Figure 11 shows a connection example of a daisy chain.

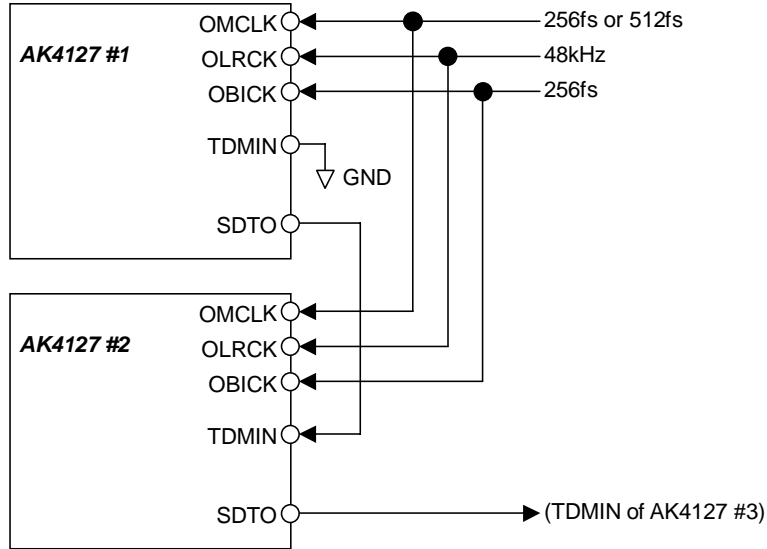


Figure 11. Cascade TDM Connection Diagram

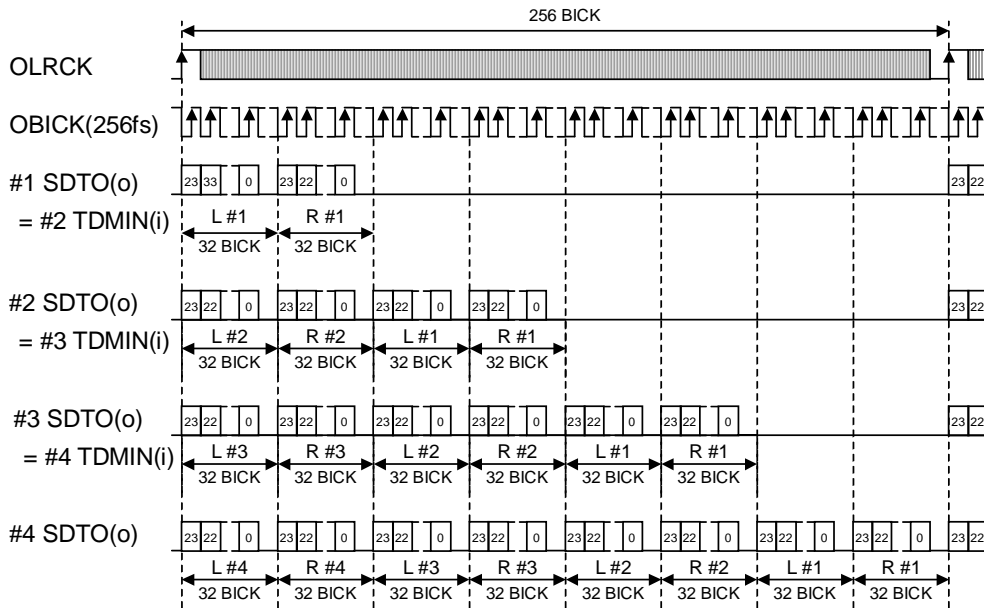


Figure 12. Cascade TDM Timing (4devices)

■ Soft Mute Operation

1. Manual mode

Soft mute operation is performed in the digital domain of the SRC output. Soft mute can be controlled by the SMUTE pin. When the SMUTE pin changes to “H”, the SRC output data is attenuated by  $-\infty$  within 1024 OLRCK cycles. When the SMUTE pin changes to “L” the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 OLRCK cycles. If the soft mute is cancelled before mute state after starting of the operation, the attenuation is discontinued and returned to 0dB by the same cycles. The soft mute is effective for changing the signal source.

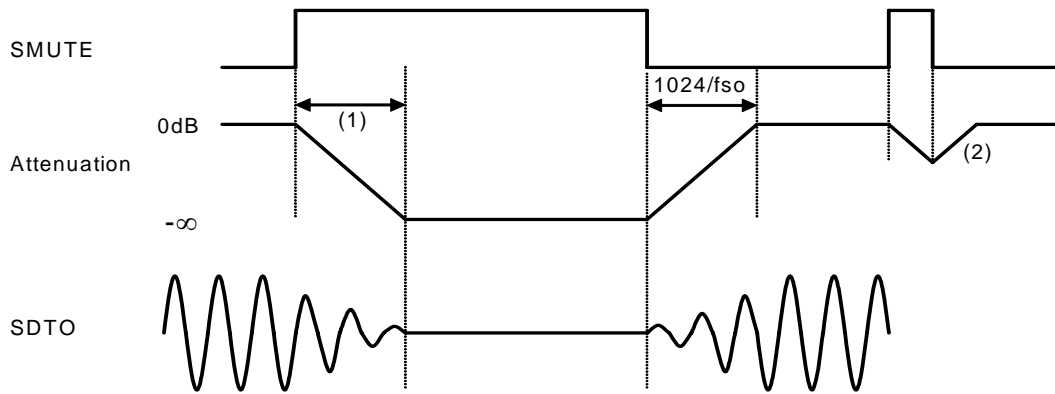


Figure 13. Soft Mute Function (Manual Mode)

- (1) The output data is attenuated by  $-\infty$  during 1024 OLRCK cycles ( $1024/f_{so}$ ).
- (2) If the soft mute is cancelled before attenuating to  $-\infty$  after starting the operation, the attenuation is discontinued and returned to 0dB by the same number of clock cycles.

2. Semi-Auto mode

The soft mute is cancelled automatically by the setting of PLL2-0 pins (Table 2), after the AK4127 detects the rising edge (PDN pin = “L” → “H”) and the mute is continued during  $4410/f_{so}=100ms@f_{so}=44.1kHz$ . After PDN pin = “L” → “H” and when SMUTE pin is “H”, the mute is not cancelled.

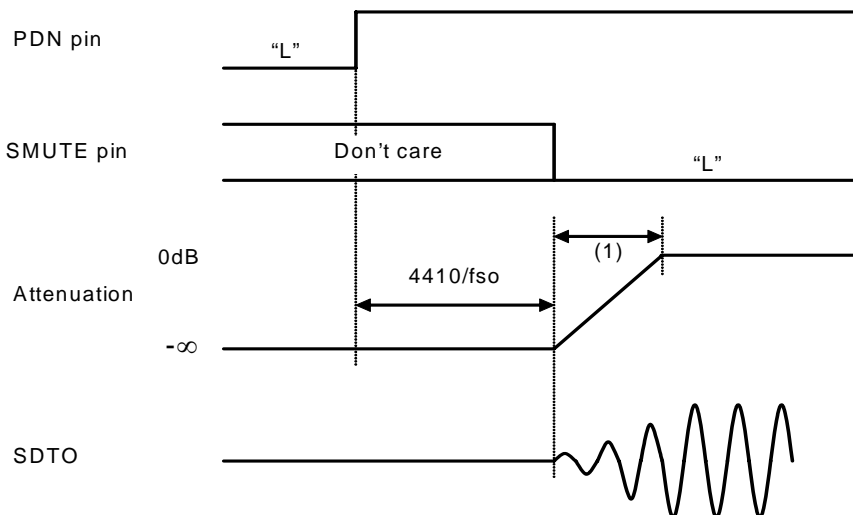


Figure 14. Soft Mute Function (Semi-Auto Mode)

- (1) The output data is returned to 0dB during 1024 OLRCK cycles ( $1024/f_{so}$ ).

■ Dither

The AK4127 has a dither circuit. The dither circuit adds the dither to the LSB of the output data, which is the value of the OBIT1-0 pins, by DITHER pin = “H” regardless of the SRC mode or the SRC bypass mode.

■ System Reset

Bringing the PDN pin = “L” sets the AK4127 power-down mode and initializes the digital filter. The AK4127 should be reset once by bringing the PDN pin = “L” when power-up. When the PDN pin = “L”, the SDTO output is “L”. The SDTO valid time is 100ms. Until the output data becomes valid, the SDTO pin outputs “L”. The SDTO valid time is 100ms. Until the output data becomes valid, the SDTO pin outputs “L”.

Case 1

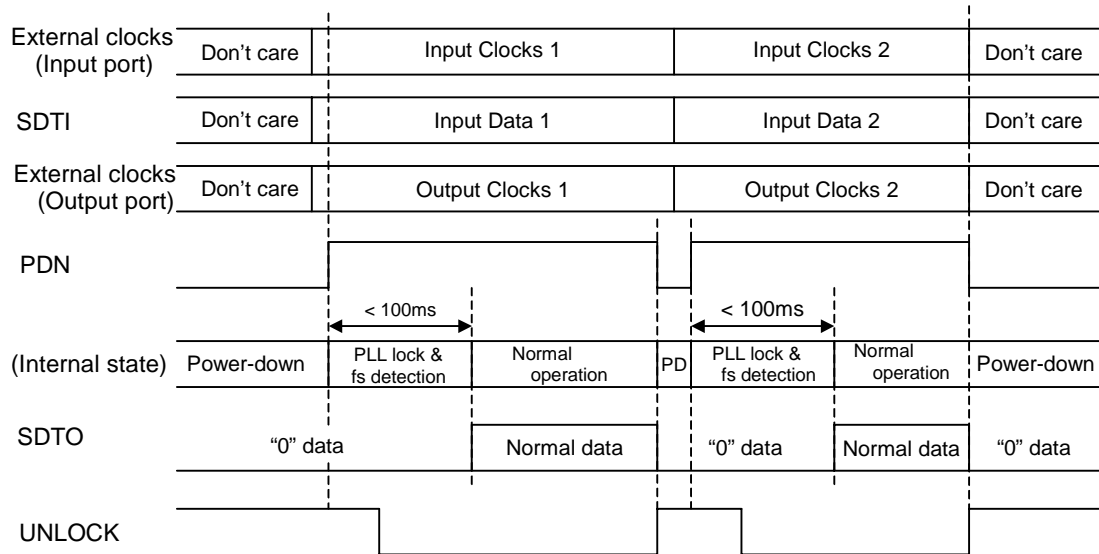


Figure 15. System Reset

Case 2

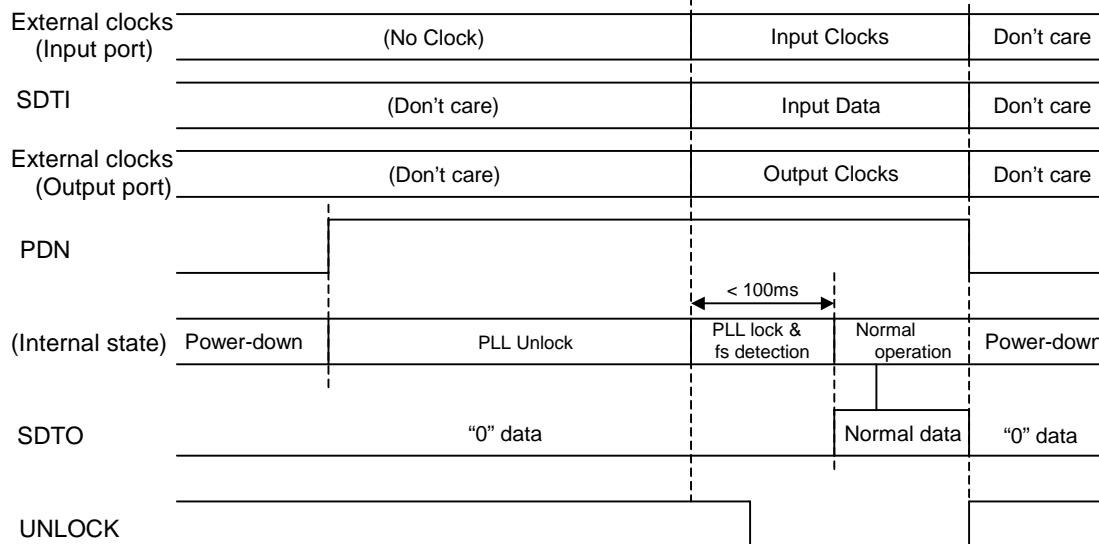


Figure 16. System Reset 2

## ■ Internal Reset Function for Clock Change

The AK4127 is reset automatically when the output clock is stopped. If the output clock is started again, normal data is output within 100ms.

## ■ Sequence of Changing Clocks

The change sequence of the clock supplied to AK4127 is shown in Figure 17.

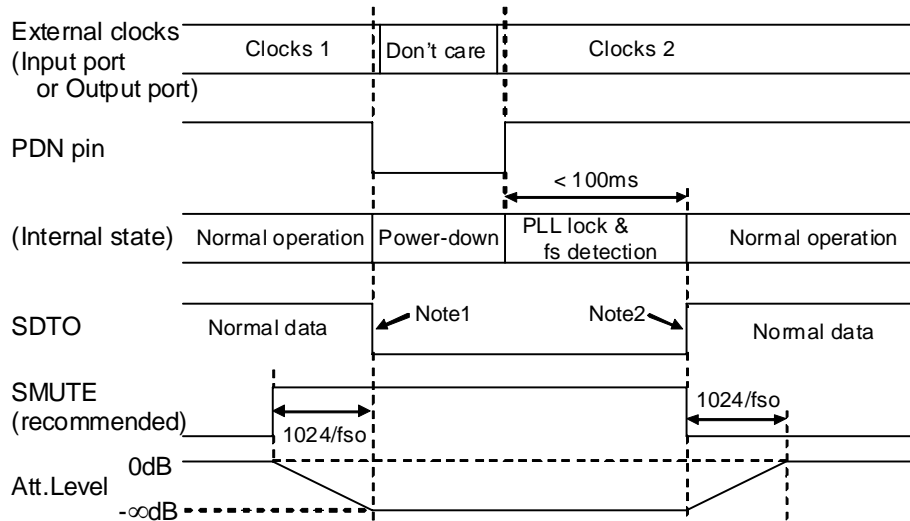


Figure 17. Sequence of Changing Clocks

Note 1. The data on SDTO may cause a clicking noise. To prevent this, set "0" to the SDTI from GD before the PDN pin changes to "L". It makes the data on SDTO remain as "0". SMUTE can also remove this clicking noise.

Note 2. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" for  $1024/f_{so} + 100\text{ms}$  or more from the timing PDN pin changes to "H" while the SMUTE pin = "H".

Note 3. When the PDN pin is not used for this clock change, a distorted signal may output for about 10ms ~ 100ms (typ) after changing clocks.

## ■ UNLOCK pin

The UNLOCK pin outputs "L" when the internal PLL is locked. When the internal PLL is unlocked, the UNLOCK pin outputs "H" and the SDTO = "0". When the PDN pin = "L", the UNLOCK pin outputs "H".

## ■ PLL Loop Filter

The C1 and R should be connected in series and attached between the FILT pin and AVSS in parallel with C2. Please be careful the noise onto the FILT pin. When using IBICK, the value of external element is not dependent on the IBICK input frequency.

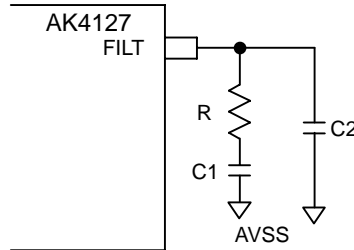


Figure 18. PLL Loop Filter

[Input PORT in slave mode]

### 1. When using ILRCK

| PLL2 | PLL1 | PLL0 | ILRCK        | R [ $\Omega$ ] | C1 [ $\mu$ F]   | C2 [nF]         |
|------|------|------|--------------|----------------|-----------------|-----------------|
| L    | L    | L    | 8k ~ 96kHz   | $1.8k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |
| L    | L    | H    | 8k ~ 216kHz  | $1k \pm 5\%$   | $1.0 \pm 30\%$  | $2.2 \pm 30\%$  |
|      |      |      | 16k ~ 216kHz | $1.5k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |
| L    | H    | L    | 8k ~ 216kHz  | $1k \pm 5\%$   | $1.0 \pm 30\%$  | $2.2 \pm 30\%$  |
|      |      |      | 16k ~ 216kHz | $1.5k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |
| L    | H    | H    | 8k ~ 216kHz  | $1k \pm 5\%$   | $1.0 \pm 30\%$  | $2.2 \pm 30\%$  |
|      |      |      | 16k ~ 216kHz | $1.5k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |

Table 6. PLL Loop Filter (ILRCK Mode)

- Note. Smaller value can be selected for the capacitors (C1, C2) in case of ILRCK range from 16kHz to 216kHz..

### 2. When using IBICK

| PLL2 | PLL1 | PLL0 | ILRCK       | R [ $\Omega$ ] | C1 [ $\mu$ F]   | C2 [nF]        |
|------|------|------|-------------|----------------|-----------------|----------------|
| H    | *    | *    | 8k ~ 216kHz | $470 \pm 5\%$  | $0.22 \pm 30\%$ | $1.0 \pm 30\%$ |

Table 7. PLL Loop Filter (IBICK Mode, \*: Don't care)

Note. The IBCIK must be continuous except when the clocks are changed.

Note. IBCIK = 32fsi is supported only 16bit LSB justified and I<sup>2</sup>S Compatible.

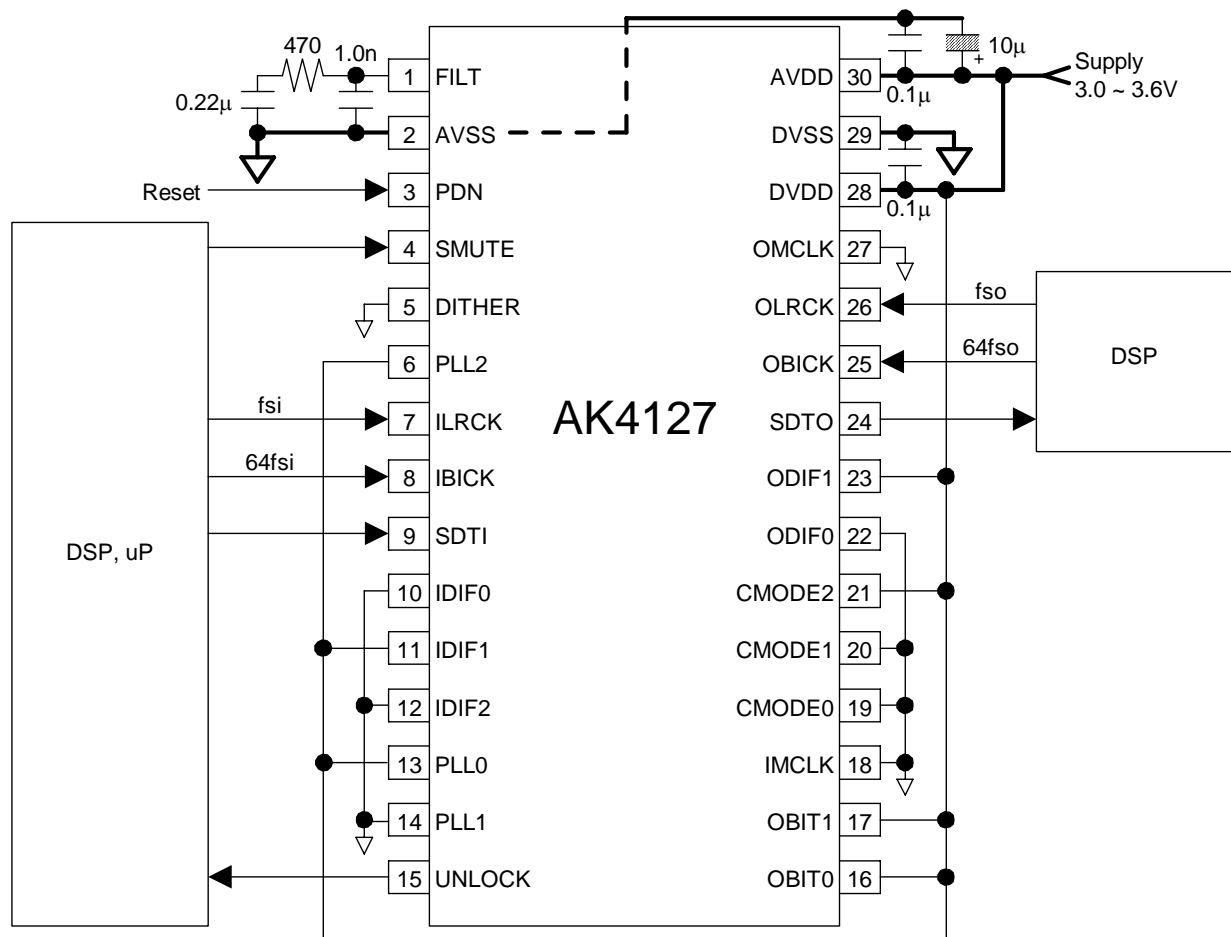
[Input PORT in master mode]

- When IMCLK is 256fs, 384fs, 512fs or 768fs, any external parts shown in [Figure 18](#) are not required.
- When IMCLK is 128fs or 192fs, the external parts shown in [Table 7](#) are required.

|                      |
|----------------------|
| <b>SYSTEM DESIGN</b> |
|----------------------|

Figure 19 and Figure 20 show the system connection diagrams. The evaluation board demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- Input PORT: Slave Mode, IBICK lock mode (64fsi), 24bit MSB justified
- Output PORT: Slave mode, 24bit MSB justified
- Dither = OFF



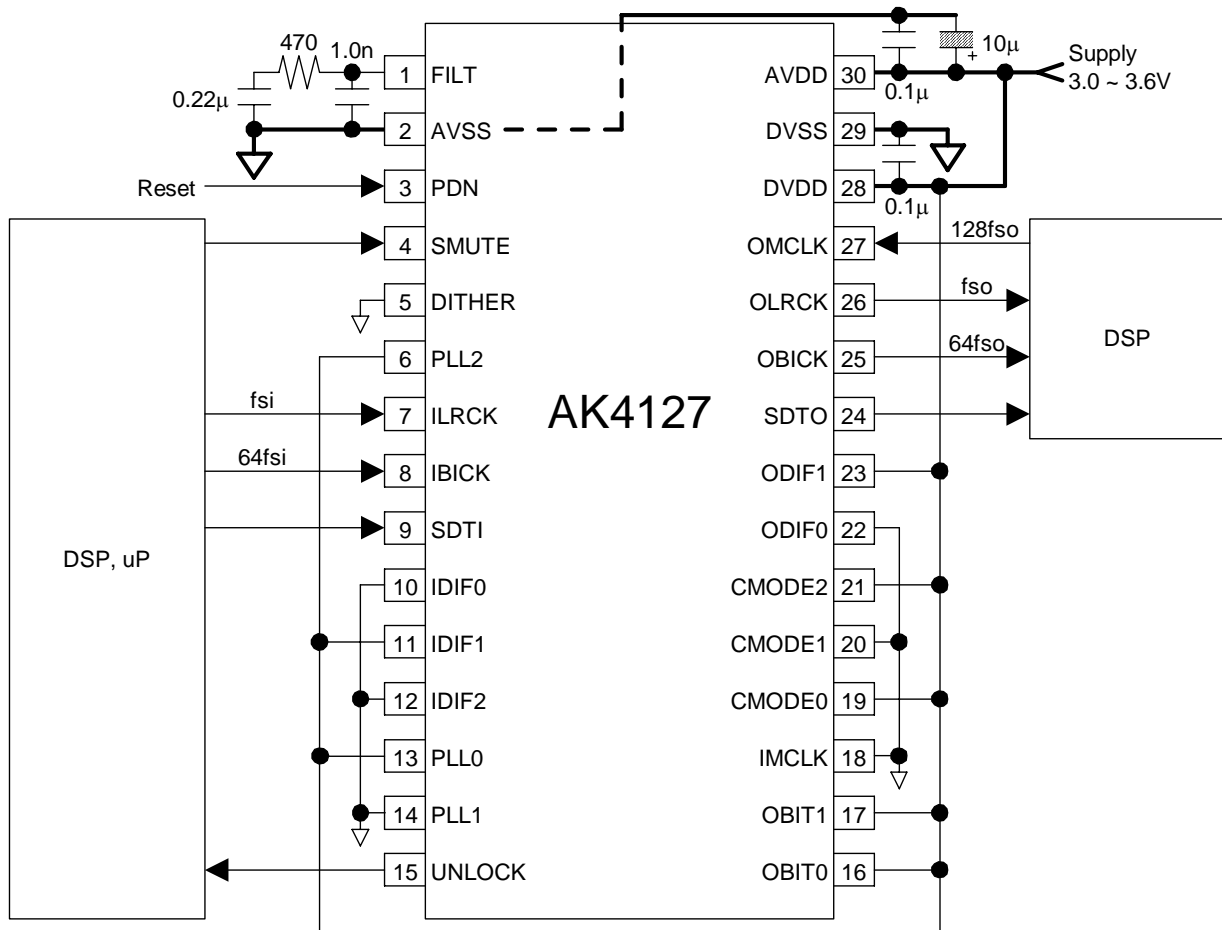
Note:

- AVSS and DVSS of the AK4127 must be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins must not be left floating.

Figure 19. Typical Connection Diagram (Slave mode)



- Input PORT: Slave Mode, IBICK lock mode (64fsi), 24bit MSB justified
- Output PORT: Master mode, 24bit MSB justified
- Dither = OFF



Note:

- AVSS and DVSS of the AK4127 must be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins must not be left floating.

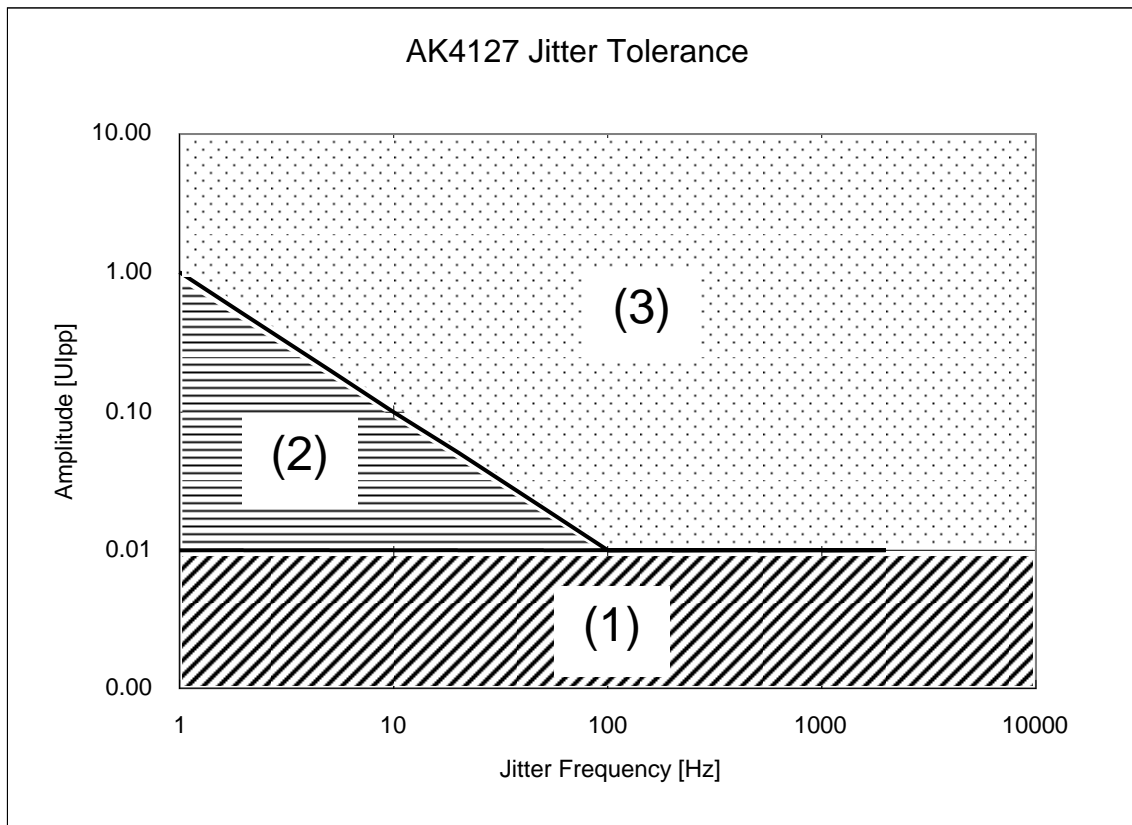
Figure 20. Typical Connection Diagram (Master mode)

## 1. Grounding and Power Supply Decoupling

The AK4127 requires careful attention to power supply and grounding arrangements. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not important. Decoupling capacitors should be as near to the AK4127 as possible, with the small value ceramic capacitor being the nearest.

## 2. Jitter Tolerance

Figure 21 shows the jitter tolerance to ILRCK and IBICK. The jitter quantity is defined by the jitter frequency and the jitter amplitude shown in Figure 21. When the jitter amplitude is 0.01UIpp or less, the AK4127 operates normally regardless of the jitter frequency.



- (1) Normal operation
- (2) There is a possibility that the distortion degrades. (It may degrade up to about -50dB.)
- (3) There is a possibility that the output data is lost.

Note:

- When PLL2-0 = "L/\*/\*" (\*: Don't care), the jitter amplitude is for ILRCK and 1UI (Unit Interval) is one cycle of ILRCK. When FSI = 48kHz, 1UI is  $1/48\text{kHz} = 20.8\mu\text{s}$ .
- When PLL2-0 = "H/\*/\*" (\*: Don't care), the jitter amplitude is for IBICK and 1UI (Unit Interval) is one cycle of IBICK. When FSI = 48kHz, 1UI is  $1/(64 \times 48\text{kHz}) = 326\text{ns}$ .

Figure 21. Jitter Tolerance

### Tracking to the Input Sampling Frequency

When the ILRCK is generated by an external PLL, it may take time to settle after changing the input sampling frequency because the response of an external PLL to the frequency change is slow. The AK4127 operates normally up to 23%/sec speed but outputs incorrect data at the speed of the frequency change over 23%/sec.

### 3. Digital Filter Response Example

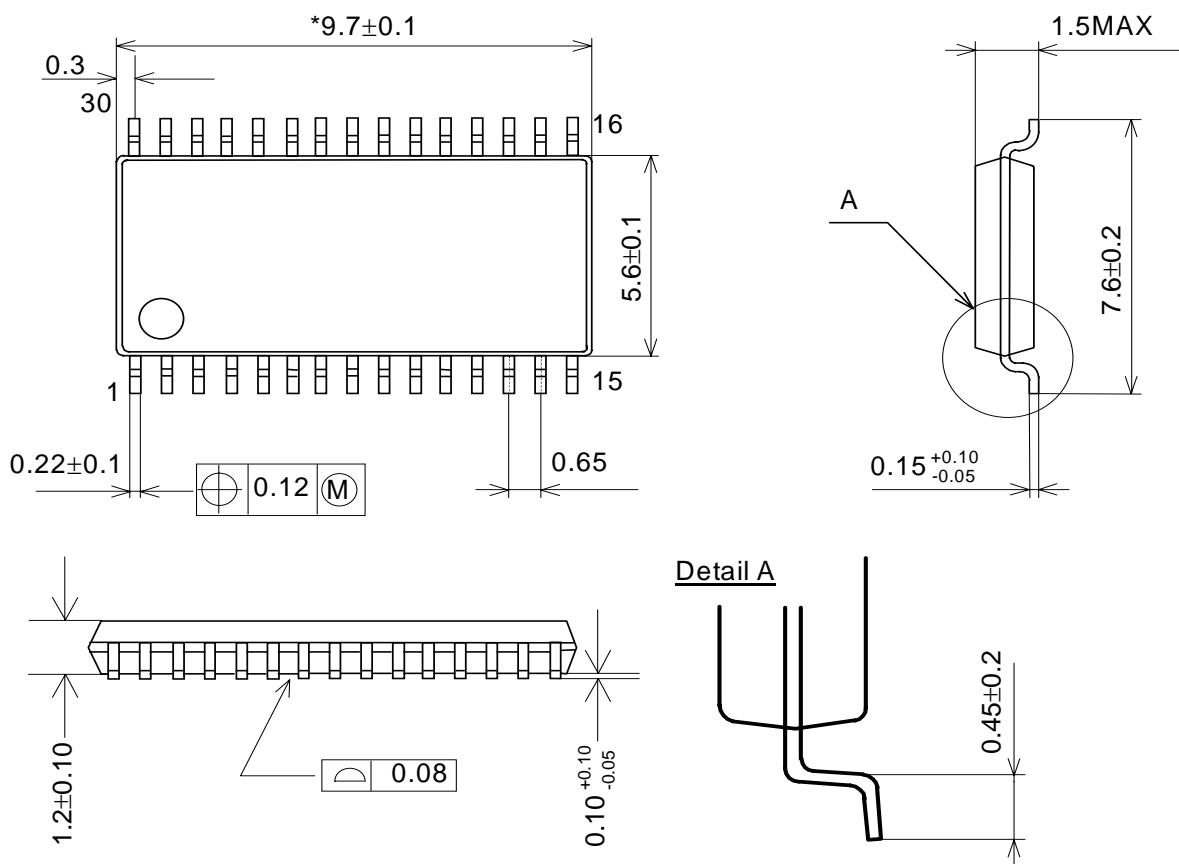
Table 8 shows the examples of digital filter response performed by the AK4127.

| Ratio | FSO/FSI [kHz] | Passband [kHz] | Stopband [kHz] | Stopband Attenuation [dB] | Gain [dB]     |
|-------|---------------|----------------|----------------|---------------------------|---------------|
| 4.000 | 192/48.0      | 22.000         | 26.000         | -121.2                    | -0.01@ 20k    |
| 1.000 | 48.0/48.0     | 22.000         | 26.000         | -121.2                    | -0.01@ 20k    |
| 0.919 | 44.1/48.0     | 20.000         | 24.100         | -121.4                    | -0.01@ 20k    |
| 0.725 | 32.0/44.1     | 14.088         | 17.487         | -115.3                    | -0.01@ 14.5k  |
| 0.667 | 32.0/48.0     | 13.688         | 17.488         | -116.9                    | -0.19@ 14.5k  |
| 0.544 | 48.0/88.2     | 19.250         | 26.232         | -114.6                    | -0.03@ 20k    |
| 0.500 | 48.0/96.0     | 20.900         | 27.000         | -100.2                    | -0.01@ 20k    |
| 0.500 | 44.1/88.2     | 19.202         | 24.806         | -100.2                    | -0.08@ 20k    |
| 0.459 | 44.1/96.0     | 18.700         | 25.000         | -103.3                    | -0.23@ 20k    |
| 0.363 | 32.0/88.2     | 12.863         | 18.665         | -102.0                    | -0.75@ 14.5k  |
| 0.333 | 32.0/96.0     | 12.500         | 18.900         | -103.6                    | -1.07@ 14.5k  |
| 0.250 | 48.0/192.0    | 17.600         | 30.200         | -104.0                    | -0.18@ 20k    |
| 0.250 | 44.1/176.4    | 16.170         | 27.746         | -104.0                    | -1.34@ 20k    |
| 0.230 | 44.1/192.0    | 15.860         | 28.240         | -103.3                    | -1.40@ 20k    |
| 0.167 | 32.0/192.0    | 11.200         | 19.600         | -73.2                     | -2.97@ 14.5k  |
| 0.181 | 32.0/176.4    | 10.278         | 17.987         | -73.2                     | -7.88@ 14.5k  |
| 0.167 | 8/48.0        | 2.800          | 4.900          | -73.2                     | -2.97@ 3.625k |
| 0.181 | 8/44.1        | 2.5695         | 4.4968         | -73.2                     | -7.88@ 3.625k |

Table 8. Digital Filter Example

**PACKAGE**

30pin VSOP (Unit: mm)

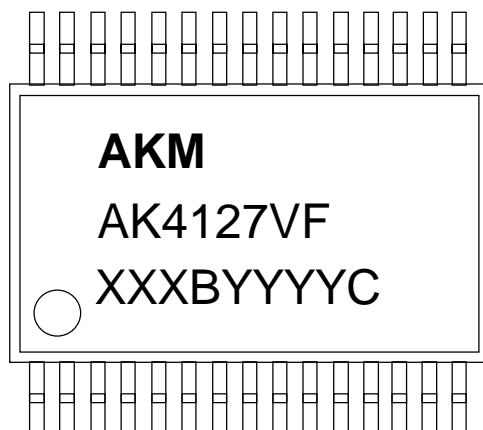


NOTE: Dimension "\*" does not include mold flash.

■ Material & Lead finish

|                               |                        |
|-------------------------------|------------------------|
| Package molding compound:     | Epoxy                  |
| Lead frame material:          | Cu                     |
| Lead frame surface treatment: | Solder (Pb free) plate |

|                |
|----------------|
| <b>MARKING</b> |
|----------------|



XXXXBYYYYC    Date code identifier

XXXXB: Lot number (X: Digit number, B: Alpha character)  
 YYYYYC: Assembly date (Y: Digit number, C: Alpha character)

|                         |
|-------------------------|
| <b>REVISION HISTORY</b> |
|-------------------------|

| Date (YY/MM/DD) | Revision | Reason               | Page | Contents   |
|-----------------|----------|----------------------|------|--|
| 07/02/07        | 00       | First edition        |      |  |
| 07/07/26        | 01       | Description Change   | 19   | Figure 13 and Figure 14 were changed.  |
|                 |          |                      | 21   | <ul style="list-style-type: none"> <li>■ Internal Rest Function for Clock Change</li> <li>■ Sequence of Changing Clocks</li> <li>■ UNLOCK pin</li> </ul> |
| 10/05/17        | 02       | Description Addition | 21   | <ul style="list-style-type: none"> <li>■ Sequence of changing clocks</li> </ul> Description is added in notes.   |

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