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XHRA-2HPA Datasheet

2015/07/09

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1 xCORE-AUDIO Processors

The xCORE-AUDIO Hi-Res family of parts offer 2-channel, 5.1 and 7.1 channel USB audio interfaces. Audio data from PC, Mac, Android, and iOS devices can be streamed through the device to I2S, DSD and/or S/PDIF interfaces. Sample rates of up to 384 KHz, and sample depths of up to 32 bits are supported.

The family of products has configuration options that include CODEC customisation, HID input and output options, and USB identification.

The XHRA-2HPA offers 2 channels of high resolution USB audio for applications that include DACs, headphone-amplifiers, USB headphones, docking solutions and more.

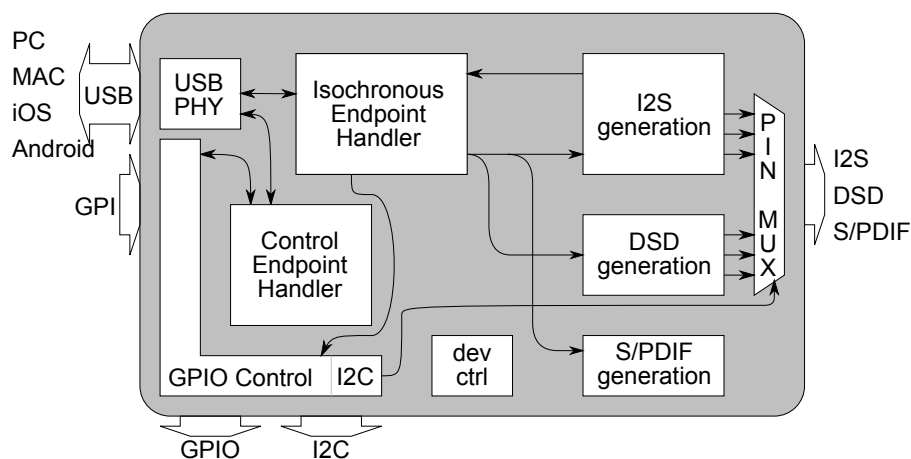


Figure 1:
XHRA-2HPA

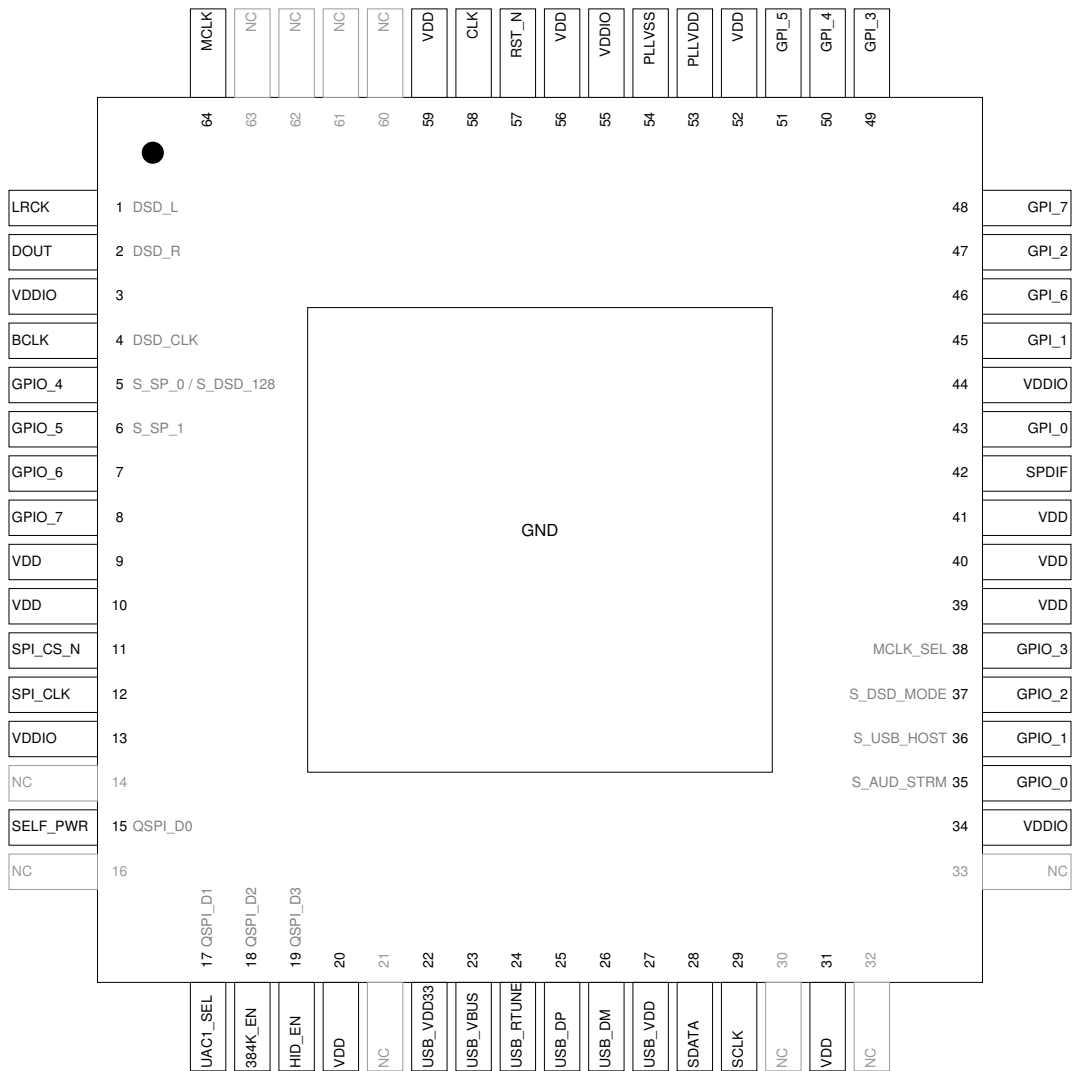
Key features of the XHRA-2HPA include:

- ▶ **USB connectivity:** USB Audio Class 2.0 or 1.0; low latency
- ▶ **Digital audio connectivity:** I2S, DSD and S/PDIF output
- ▶ **Configurable I/O:** HID, GPIO
- ▶ **Configurable CODEC:** I2C

2 XHRA-2HPA Features

- ▶ **USB: 2 high resolution channels OUT**
 - PCM up to 384 KHz (44.1, 48, 88.2, 96, 176.4, 192, 352.8, 384) sample rates
 - Asynchronous Isochronous transfer from host
 - Native DSD, DoP64 and DoP128
- ▶ **CODEC: I2S or DSD**
 - 16, 24, or 32 bit PCM
 - DSD64 and DSD128
- ▶ **Optional S/PDIF output**
 - Up to 192 KHz; 16/24 bit resolution
- ▶ **Flexible integration and control**
 - 8 GPIO for system control
 - 8 GPI for HMI with optional HID inputs
 - I2C master port for configuration and control
 - Basic configuration through straps
 - External flash for advanced configuration
- ▶ **Multiple OS support**
 - Windows
 - Mac OS X
 - Apple iOS (Apple Host Mode)
 - iAP2/iAP1 support
 - Android
- ▶ **Field upgrade capability**
- ▶ **Ambient Temperature Range**
 - Commercial qualification: 0°C to 70°C
- ▶ **Power**
 - Bus/Self powered.
 - Consumption: 400 mW.
- ▶ **64-pin TQFP package 0.5 mm pitch**

3 Pin Configuration



4 Signal Description

This section lists the signals and I/O pins available on the XHRA-2HPA. Pins marked ST have a Schmitt Trigger on their input. PU and PD refers to weak pull up and pull down present on the pins.

Power pins (9)			
Signal	Function	Type	Properties
GND	Digital ground	GND	
PLLVD	Analog PLL power	PWR	
PLLVSS	Analog ground for PLL	PWR	
USB_VDD	Digital core power	PWR	
USB_VDD33	USB Analog power	PWR	
VDD	Digital core power	PWR	
VDDIO	Digital I/O power	PWR	

Audio I/O pins (33)			
Signal	Function	Type	Properties
BCLK	I2S serial bit clock; Alternate function: DSD_CLK - DSD serial clock in DSD mode	I/O	
LRCK	I2S left right clock; Alternate function: DSD_L - DSD left channel signal in DSD mode	I/O	
DOUT	I2S serial data out to DAC or CODEC; Alternate function: DSD_R - DSD right channel data signal in DSD mode	Output	
SPDIF	S/PDIF transmitter output	Output	
MCLK	Audio Master clock input - (24.576MHz and 22.5792MHz)	Input	

Two wire configuration interface pins (2)			
Signal	Function	Type	Properties
SDATA	Master serial data (I2C interface)	I/O	PD
SCLK	Master clock output (I2C interface)	Output	PD

GPIO pins (8)			
Signal	Function	Type	Properties
GPIO_0	Programmable I/O pin; Default function: S_AUD_STRM - shows status of Audio stream. High - Audio stream active, Low - No audio stream	I/O	PD

(continued)

Signal	Function	Type	Properties
GPIO_1	Programmable I/O pin; Default function: S_USB_HOST – shows whether USB host connected or not. High – Connected, Low – Not connected	I/O	PD
GPIO_2	Programmable I/O pin; Default function: S_DSD_MODE – shows whether DSD mode is active or not. High – DSD mode, Low – PCM mode	I/O	PD
GPIO_3	Programmable I/O pin; Default function: MCLK_SEL – used to select the audio master clock between 24.576MHz and 22.5792MHz to support different audio sample rates	I/O	PD
GPIO_4	Programmable I/O pin; Default function: S_SP_0 – in PCM mode it denotes the currently active audio sample rate. Alternate function: S_DSD_128 – in DSD mode it denotes the DSD format. High – DSD128, Low – DSD64	I/O	PD
GPIO_5	Programmable I/O pin; Default function: S_SP_1 – in PCM mode it denotes the currently active audio sample rate.	I/O	PD
GPIO_6	Programmable I/O pin	I/O	PD
GPIO_7	Programmable I/O pin	I/O	PD

GPI pins (8)			
Signal	Function	Type	Properties
GPI_0	Programmable input; Alternate function: PLAY_PAUSE – HID play/pause button input	Input	PD
GPI_1	Programmable input; Alternate function: VOLP – HID volume up button input	Input	PD
GPI_2	Programmable input; Alternate function: VOLM – HID volume down button input	Input	PD
GPI_3	Programmable input; Alternate function: PREV – HID previous track select button input	Input	PD
GPI_4	Programmable input; Alternate function: NEXT – HID next track select button input	Input	PD
GPI_5	Programmable input; Alternate function: PREV – HID mute button input	Input	PD
GPI_6	Programmable input	Input	PD
GPI_7	Programmable input	Input	PD

Configuration I/O pins (5)			
Signal	Function	Type	Properties
SELF_PWR	Selects USB power option; Pull up - Self power; Alternate function: QSPI_D0 - Data line of Quad-SPI	Input	PD
UAC1_SEL	Selects USB Audio Class 1.0 version; Pull up - UAC 1.0. Alternate function: QSPI_D1 - Data line of Quad-SPI	Input	PD
384K_EN	Enables the 384KHz and 352.8KHz audio sample rates; Pull up - Enable. Alternate function: QSPI_D2 - Data line of Quad-SPI	Input	PD
HID_EN	Enables the HID button inputs on GPI pins; Pull up - Enable. Alternate function: QSPI_D3 - Data line of Quad-SPI	Input	PD

USB pins (5)			
Signal	Function	Type	Properties
USB_DM	USB Serial Data Inverted	I/O	
USB_DP	USB Serial Data	I/O	
USB_RTUNE	USB resistor	I/O	
USB_VBUS	USB Power Detect Pin	I/O	

Quad-SPI serial flash interface pins (6)			
Signal	Function	Type	Properties
SPI_CS_N	SPI chip select line (Active low) for external flash device.	Output	
SPI_CLK	SPI clock	Output	
QSPI_D0...D4	Four data lines of the Quad-SPI acting as alternate functions of Configuration I/Os mentioned above	Inputs	

System pins (2)			
Signal	Function	Type	Properties
CLK	PLL reference clock of 24MHz	Input	PD, ST
RST_N	Global reset input	Input	PU, ST

Reserved/NC pins (10)			
Signal	Function	Type	Properties
NC	No connection pins	Input	

Figure 2 shows the pin in relation to the block diagram.

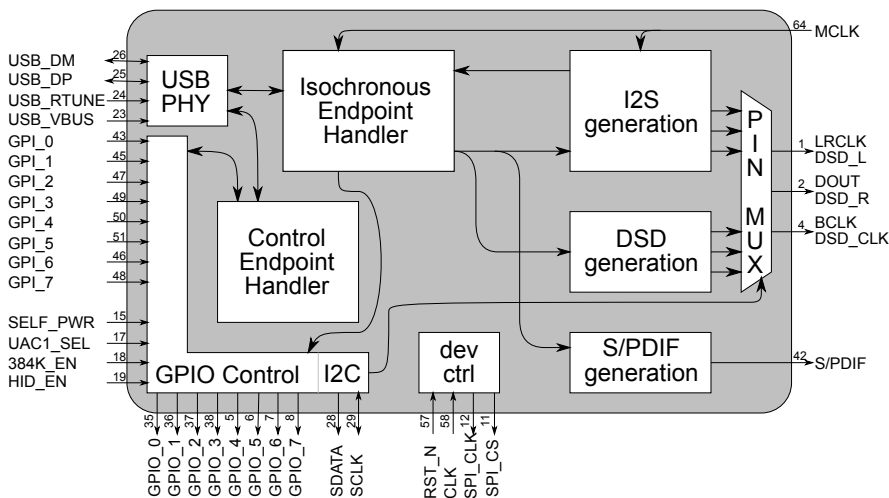


Figure 2:
Pins in relation to the block diagram

5 Example Application Diagram

Figure 3 shows a simplified schematic with the XHRA-2HPA device. The following section discusses the individual parts of the system.

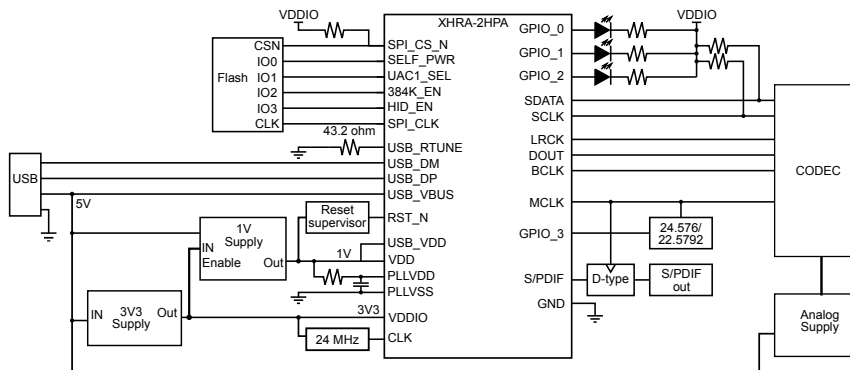


Figure 3:
Simplified Reference Schematic

6 Functional Description and System Components

The XHRA-2HPA streams 2-channel high resolution audio from a USB host to a number of potential interfaces, including I2S/DSD and S/PDIF. An I2C bus is

included that can be used to tailor the device to a number of different operating modes and system configurations.

The XHRA-2HPA needs to be provided with a clock and a Quad SPI flash. A CODEC containing a DAC can be used to drive stereo line out. An external flash is used to store configuration information. S/PDIF output can be connected to a suitable optical/coaxial transmitter circuit.

The XHRA-2HPA drives the I2C bus at 100 KHz. Two external 3K3 resistors should pull-up both SDA and SCLK lines. The configuration data can contain I2C commands to configure external devices such as CODECs, DACs and clock generation ICs etc.

6.1 Clocks

Two clocks are required for the device.

- ▶ 24 MHz clock to clock the USB side. (CLK)
- ▶ Audio master clock for the asynchronous clocking mode. (MCLK)

If the master clock is fixed at 24.576 MHz, then only 48, 96, 192, and 384 KHz can be supported; and the other frequencies should be disabled in the configuration (byte 6, Appendix A.2). If the master clock is fixed at 22.5792 MHz, then only 44.1, 88.2, 176.4, and 352.8 KHz can be supported, and the other sample rates should be disabled in the configuration (byte 6, Appendix A.2).

All sample rates can be supported if the master clock can switch between 24.576 MHz and 22.5792 MHz. This switch is controlled by GPIO_3 (MCLK_SEL) in default case. If GPIO_3 is high then the master clock should run at 24.576 MHz; otherwise it should run at 22.5792 MHz. If needed, GPIO_3 can be reassigned through the flash configuration.

6.2 CODEC

By default, XHRA-2HPA can work with any codec that supports I2S and/or DSD. To work with the default settings, the CODEC should expect:

- ▶ data transfer using I2S mode
- ▶ a master clock of 24.576 MHz for 48, 96, 192 (and 384) KHz sample rates
- ▶ a master clock of 22.5792 MHz for 44.1, 88.2, 176.4 (and 352.8) KHz sample rates.

CODECs that are configurable over I2C can be configured by storing a series of configuration sequences in the flash. These configuration sequences can, for example, store an initialisation sequence, switch sample rates, or mute the device. Similarly, the CODEC reset line can be controlled by any GPIO through flash configuration.

Example usage of CODECs is provided in the reference design platforms of XHRA-2HPA . Please refer to Appendix D for more information on the associated reference design platforms.

6.3 Flash

A Quad SPI flash memory with a minimum size of 1 MByte must be attached to the device. The pins of the QSPI interface are shown in the Figure 4; the four data lines are shared with configuration straps (see Appendix A).

Pin	Signal	Description
SPI_CS_N	SS	Slave Select
SELF_POWER	IO0	Data bit 0
UAC1_SEL	IO1	Data bit 1
384K_EN	IO2	Data bit 2
HID_EN	IO3	Data bit 3
SPI_CLK	SCLK	Clock

Figure 4:
QSPI pins

The QSPI flash memory should store the device firmware binary and the optional configuration information. Further information on the XHRA-2HPA firmware binary is available at <http://www.xmos.com/products/audio/xcore-audio-hi-res-2>.

The XHRA-2HPA device reads from the flash during booting. It expects each byte to be transferred with the *least-significant nibble first*. The programming tool which flashes the QSPI memory must make sure that the least significant nibble of a byte is transferred first. It should also ensure that the Quad SPI mode is enabled in the status register.

Figure 5 shows the list of currently supported Quad-SPI flash devices.

Vendor	Device Part Number
Spansion	S25FL116K
Spansion	S25FL132K
Spansion	S25FL164K
ISSI	IS25LQ080B
ISSI	IS25LQ016B
ISSI	IS25LQ032B

Figure 5:
Supported
Quad-SPI
flash devices

6.4 Configuration information

Configuration information is stored in the flash. This includes information such as the USB Vendor and Product Identification (VID/PID), serial number, and GPIO assignment. This is detailed in Appendix A.2. Basic configurations can be created by strapping IO pins, see Appendix A.1.

If no configuration information is found in the flash, the XHRA-2HPA device will use default values.

6.5 S/PDIF output (optional)

The device generates S/PDIF output. This can be connected to either an optical transmitter, or to a coaxial driver. If S/PDIF output is used, then the signal should first be fed through a D-type flip flop in order to synchronise the S/PDIF signal to the master-clock.

7 Board Integration

This section details the guidelines to be followed in designing a PCB with XHRA-2HPA device.

7.1 USB connections

USB_VBUS should be connected to the VBUS pin of the USB connector. A 2.2 μF capacitor to ground is required on the VBUS pin. A ferrite bead may be used to reduce HF noise.

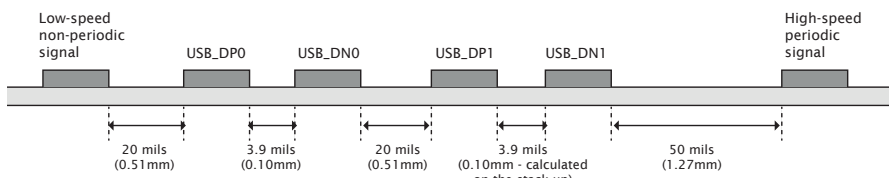
For self-powered systems, a bleeder resistor may be required to stop VBUS from floating when no USB cable is attached.

USB_DP and USB_DN should be connected to the USB connector.

7.2 USB signal routing and placement

The USB_DP and USB_DN lines are the positive and negative data polarities of a high speed USB signal respectively. Their high-speed differential nature implies that they must be coupled and properly isolated. The board design must ensure that the board traces for USB_DP and USB_DN are tightly length matched. In addition, according to the USB 2.0 specification, the USB_DP and USB_DN differential impedance must be 90Ω .

Figure 6:
USB trace separation showing a low speed signal, two differential pairs and a high-speed clock



7.2.1 General routing and placement guidelines

The following guidelines will help to avoid signal quality and EMI problems on high speed USB designs. They relate to a four-layer (Signal, GND, Power, Signal) PCB.

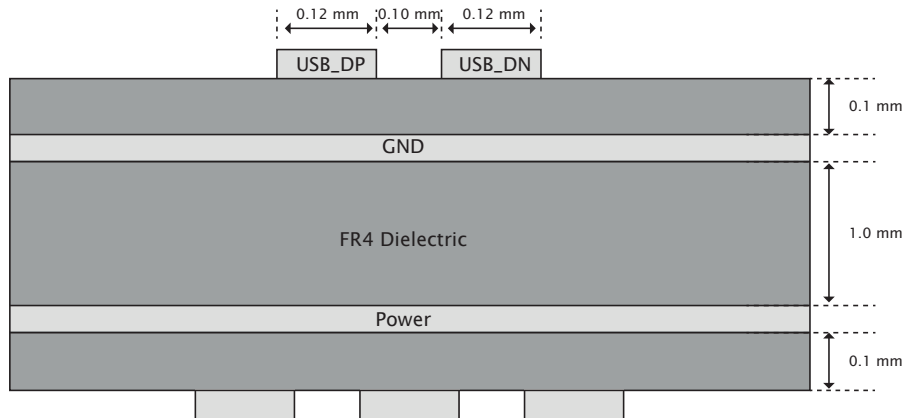


Figure 7:
Example USB
board stack

For best results, most of the routing should be done on the top layer (assuming the USB connector and XHRA-2HPA are on the top layer) closest to GND. Reference planes should be below the transmission lines in order to maintain control of the trace impedance.

We recommend that the high-speed clock and high-speed USB differential pairs are routed first before any other routing. When routing high speed USB signals, the following guidelines should be followed:

- ▶ High speed differential pairs should be routed together.
- ▶ High-speed USB signal pair traces should be trace-length matched. Maximum trace-length mismatch should be no greater than 4mm.
- ▶ Ensure that high speed signals (clocks, USB differential pairs) are routed as far away from off-board connectors as possible.
- ▶ High-speed clock and periodic signal traces that run parallel should be at least 1.27mm away from USB_DP/USB_DN (see Figure 6).
- ▶ Low-speed and non-periodic signal traces that run parallel should be at least 0.5mm away from USB_DP/USB_DN (see Figure 6).
- ▶ Route high speed USB signals on the top of the PCB wherever possible.
- ▶ Route high speed USB traces over continuous power planes, with no breaks. If a trade-off must be made, changing signal layers is preferable to crossing plane splits.
- ▶ Follow the $20 \times h$ rule; keep traces $20 \times h$ (the height above the power plane) away from the edge of the power plane.
- ▶ Use a minimum of vias in high speed USB traces.

- ▶ Avoid corners in the trace. Where necessary, rather than turning through a 90 degree angle, use two 45 degree turns or an arc.
- ▶ DO NOT route USB traces near clock sources, clocked circuits or magnetic devices.
- ▶ Avoid stubs on high speed USB signals.

7.3 Power supplies

The device has the following power supply pins:

- ▶ VDD pins for the digital core, including a USB_VDD pin that powers the USB PHY
- ▶ VDDIO pins for the I/O lines
- ▶ PLLVDD pins for the PLL
- ▶ A USB_VDD33 pin for the analogue supply to the USB-PHY

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The VDDIO supply must ramp to its final value before VDD reaches 0.4 V.

The PLLVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 Ω resistor and 100 nF multi-layer ceramic capacitor) is recommended on this pin.

The following ground pins are provided:

- ▶ PLLVSS for PLLVDD
- ▶ GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 μ F should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up. RST_N must be asserted low during and after power up for 100 ns.

7.4 Land patterns and solder stencils

The land pattern recommendations in this document are based on a RoHS compliant process and derived, where possible, from the nominal *Generic Requirements for Surface Mount Design and Land Pattern Standards IPC-7351B* specifications. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints.

Solder paste and ground via recommendations are based on our engineering and development kit board production. They have been found to work and optimized as appropriate to achieve a high yield. The size, type and number of vias used in the center pad affects how much solder wicks down the vias during reflow. This in turn, along with solder paster coverage, affects the final assembled package height. These factors should be taken into account during design and manufacturing of the PCB.

The following land patterns and solder paste contains recommendations. Final land pattern and solder paste decisions are the responsibility of the customer. These should be tuned during manufacture to suit the manufacturing process.

The package is a 64 pin Thin Quad Flat Pack package with exposed heat slug on a 0.5mm pitch. An example land pattern is shown in Figure 8.

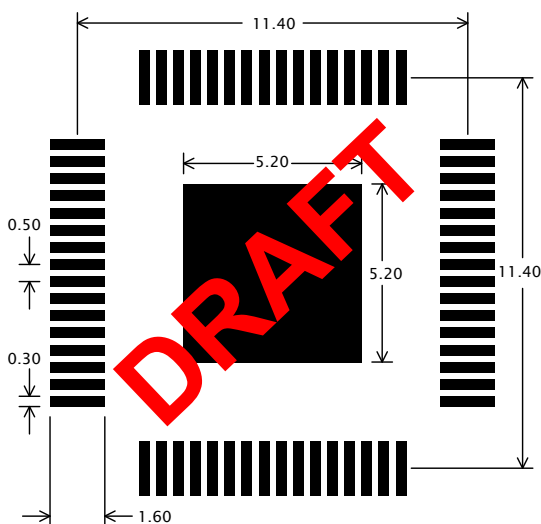
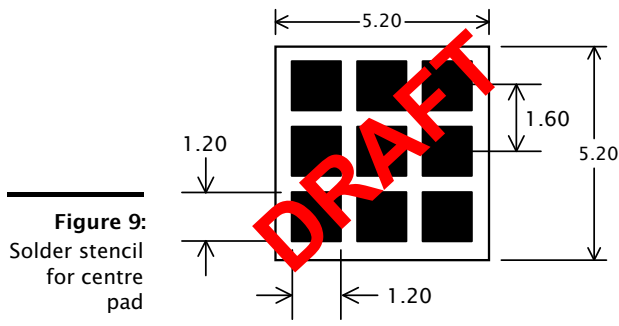


Figure 8:
Example land
pattern

For the 64 pin TQFP package, a 3x3 array of squares for solder paste is recommended as shown in Figure 9. This gives a paste level of 48%.

7.5 Ground and Thermal Vias

Vias under the heat slug into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. A 3 x 3 grid of



vias, with a 0.6mm diameter annular ring and a 0.3mm drill, equally spaced across the heat slug, would be suitable.

7.6 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour pressure of moisture. Example damage can include bond wire damage, die lifting, internal or external package cracks and/or delamination.

All XMOS devices are Moisture Sensitivity Level (MSL) 3 - devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from *Joint IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices J-STD-020* Revision D.

8 Example XHRA-2HPA Board Designs

An example layout is shown in Figure 10.

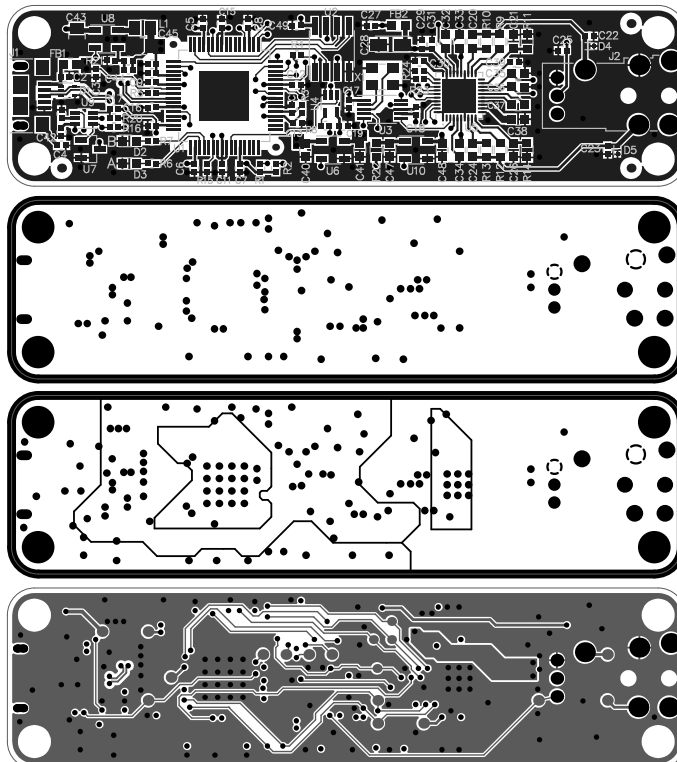


Figure 10:
Example layout, showing a 4-layer PCB layout of the part, from top to bottom

It is essential to place decouplers close to the device. In the layout shown in Figure 10, power is supplied on VDD and VDDIO through a decoupler located very close to the pin, with power supplied through a via underneath the device.

9 DC and Switching Characteristics

9.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIOL	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOR	I/O supply voltage	3.135	3.30	3.465	V	
VDD33	Peripheral supply	3.135	3.30	3.465	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	
Cl	xCORE Tile I/O load capacitance			25	pF	
Ta	Ambient operating temperature (Commercial)	0		70	°C	
	Ambient operating temperature (Industrial)	-40		85	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

Figure 11:
Operating conditions

9.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2.00		3.60	V	A
V(IL)	Input low voltage	-0.30		0.70	V	A
V(OH)	Output high voltage	2.20			V	B, C
V(OL)	Output low voltage			0.40	V	B, C
R(PU)	Pull-up resistance		35K		Ω	D
R(PD)	Pull-down resistance		35K		Ω	D

Figure 12:
DC characteristics

A All pins except power supply pins.

B All general-purpose I/Os are nominal 4 mA.

C Measured with 4 mA drivers sourcing 4 mA, 8 mA drivers sourcing 8 mA.

D Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.

9.3 ESD Stress Voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model	-2.00		2.00	KV	
CDM	Charged Device Model	-500		500	V	

Figure 13:
ESD stress voltage

9.4 Reset Timing

Figure 14:
Reset timing

Symbol	Parameters	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	5			μs	
T(INIT)	Initialization time			150	μs	A

A Shows the time taken to start booting after RST_N has gone high.

9.5 Power Consumption

Figure 15:
xCORE Tile
currents

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		45		mA	A, B, C
PD	Tile power dissipation		325		μW/MIPS	A, D, E, F
IDD	Active VDD current ()		255	310	mA	A, G
	Active VDD current		310	375	mA	A, H
I(ADDPLL)	PLL_AVDD current			5	mA	I

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages with no switching activity.

C Includes PLL current.

D Assumes typical tile and I/O voltages with nominal switching activity.

E Assumes 1 MHz = 1 MIPS.

F PD(TYP) value is the usage power consumption under typical operating conditions.

G Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 400 MHz, average device resource usage.

H Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.

I PLL_AVDD = 1.0 V

9.6 Clock

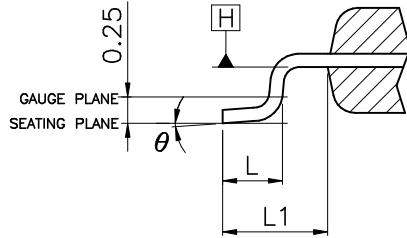
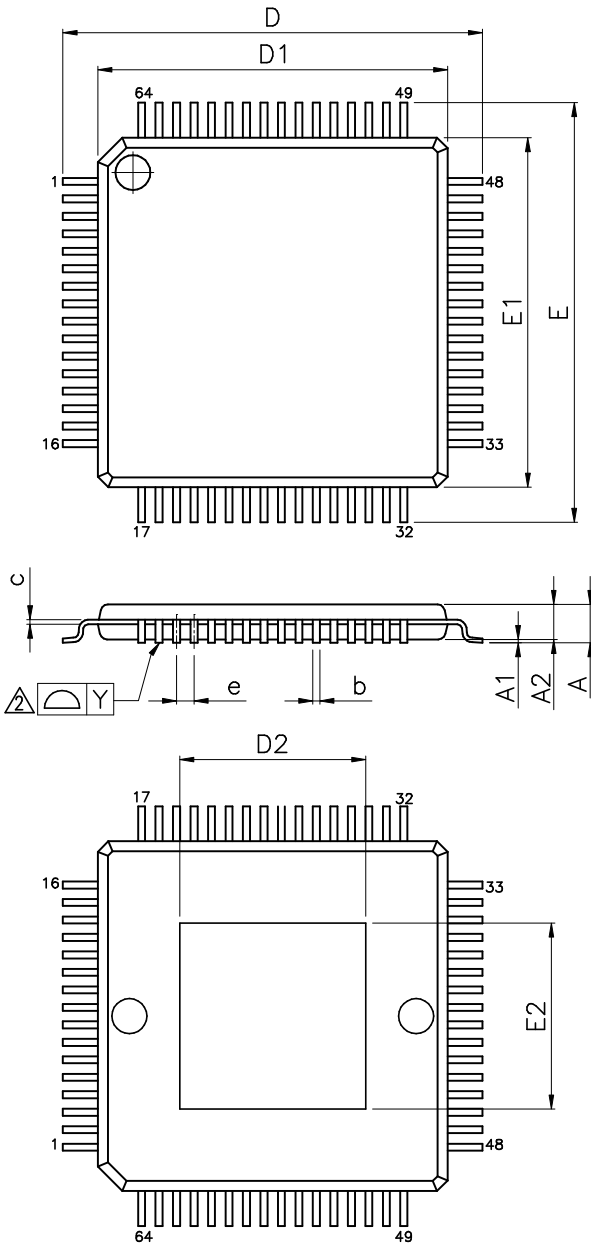
Figure 16:
Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	9	24	25	MHz	
SR	Slew rate	0.10			V/ns	
TJ(LT)	Long term jitter (pk-pk)			2	%	A
f(MAX)	Processor clock frequency ()			400	MHz	B
	Processor clock frequency			500	MHz	B

A Percentage of CLK period.

B Assumes typical tile and I/O voltages with nominal activity.

10 Package Information



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
D2	5.13	—	5.48
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
E2	5.13	—	5.48
b	0.17	0.22	0.27
c	0.09	—	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
e	0.50 BSC		
θ	0°	3.5°	7°
Y	0.08		

NOTES:

- JEDEC OUTLINE : MS-026 ACD-HD
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DIMENSIONS $D1$ AND $E1$ DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS $D1$ AND $E1$ DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

10.1 Part Marking

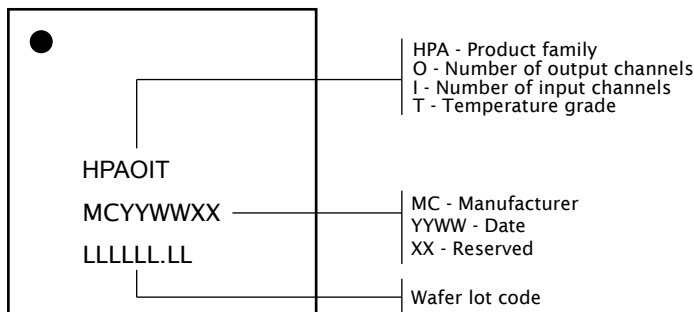


Figure 17:
Part marking scheme

11 Ordering Information

Figure 18:
Orderable part numbers

Product Code	Marking	Qualification	Channels
XHRA-2HPA-TQ64-C	HPA20	Commercial	2 OUT

12 Host Driver Support

XHRA-2HPA enumerates as USB Audio Class 2.0/1.0 compliant device in the host machine and requires a Audio Class compliant driver for its operation. USB Audio Class 2.0 and 1.0 are natively supported in Apple OSX (UAC 2.0 since OSX 10.6.4 version) and therefore doesn't need a driver installation. Windows operating systems do not natively support Audio Class 2.0 and hence require third party drivers to be installed. XMOS therefore provides a free Windows USB Audio driver for evaluation and prototyping and also a path to a more feature-rich production driver from Thesycon.

12.1 Windows Evaluation Driver

The Evaluation Driver is a fully featured evaluation version of the Thesycon 'TUSBAudio' USB Audio 2.0 Class Driver for Windows. It is available as a free download from xmos.com for evaluation and prototyping purposes only. The driver is locked to the default VID and PID of the XHRA-2HPA device and works with Windows XP, Vista, 7, 8 and 8.1 (32 and 64bit).

Note: For more information please refer to 'Thesycon Driver' section in the [USB 2.0 Driver for Windows](#) document.

12.2 XMOS Stereo Driver for Production

The XMOS Stereo Driver is based on the Thesycon 'TUSBAudio' USB Audio 2.0 Class Driver for Windows and is available free-of-charge to qualified XMOS customers for prototyping and production runs of up to 10,000 units.

The XMOS USB Audio 2.0 Stereo Driver uses the XMOS USB VendorID (VID) and an XMOS assigned customer ProductID (PID). For more information please refer to 'XMOS Stereo Driver' section in the [USB 2.0 Driver for Windows](#) document.

13 Apple MFi compatibility

XHRA-2HPA can operate with Apple iPod, iPhone, and iPad devices that feature USB host support. Information regarding this functionality is protected by the Made For iPod (MFi) program and associated licensing.

Please contact XMOS for details and further documentation.

Appendices

A Configuration

The system is configured through one of two mechanisms:

- ▶ a limited number of straps or
- ▶ the flash that contains configuration information.

Flash configuration overwrites all strap options.

A.1 Configuration straps

There are four pins that can be used to configure basic functionality. To select a function, the pin must be pulled to VDDIO with a 3.3K resistor. Do not strap the pin directly to VDDIO.

The straps are not required if the configuration information is stored in flash.

The straps have the following meanings:

- ▶ **SELF_PWR**. If this is selected, the device will be self-powered. By default, the device will advertise itself as bus-powered. Select this function if you have an external power-supply.
- ▶ **UAC1_SEL**. If this is selected, the device will advertise as a USB-Audio class 1.0 device instead of Audio class 2.0. This makes the device operate with reduced set of features, i.e. USB in full speed mode, audio sampling rates of upto 96KHz only and no DFU support.
- ▶ **384K_EN**. If this is selected, the device will enable 384 KHz and 352.8 KHz audio sample rates (in addition to the other lower sample rates).
- ▶ **HID_EN**. If this is selected, the device will take HID audio control inputs over the GPI pins.

If no configuration straps are used, and there is no information in flash, then the device will configure to:

- ▶ Bus-powered (ie, VBUS should power 1V and 3V3)
- ▶ Up to 192 KHz sample rate only.
- ▶ USB Audio class 2.0.
- ▶ HID inputs disabled.

This is a useful default for applications like a headphone amplifier.

A.2 Flash Configuration

Configuration can be stored in the QSPI flash. Byte 0 of the configuration is stored in address 0x80000. Presence of configuration data in flash is identified by length bytes and marker bytes at the beginning of the configuration section. If no configuration is found during the booting of the device, then the strap values combined with default values will be used for the operation.

The parameters that can be configured in flash are described in the remainder of this section.

Note: Configuration section starts at address 0x80000 of the QSPI flash memory.

A.2.1 Bytes 0..18

- ▶ **Bytes 0 and 1:** Length of the configuration section in bytes excluding these length bytes. (stored LSB first)
- ▶ **Byte 2 and 3:** Marker bytes. Must store 0xA5,0x00.
- ▶ **Bytes 4 and 5:** USB VID: this is the Vendor ID of your company as registered with USB (stored LSB first)
- ▶ **Bytes 6 and 7:** USB PID: this is the Product ID of this product as identified by your company (stored LSB first).
- ▶ **Byte 8:** USB Maximum power in units of 2mA. Default is 0xFA i.e., 500mA
- ▶ **Byte 9:** stores four flags that are used instead of the straps (see the previous section for the complete definition of each bit):
 - ▶ bit 0: SELF_PWR.
 - ▶ bit 1: UACT_SEL
 - ▶ bit 2: 384K_EN
 - ▶ bit 3: HID_EN
 - ▶ bits 4-7: reserved, store 0
- ▶ **Byte 10:** stores two bit flags that configure the I2S format. By default, I2S comes up in I2S default mode (that is, the data is one clock later than the LRCLK), but it can be configured to use left aligned mode or right aligned mode instead. At most one of bit 0 or 1 should be set:
 - ▶ bit 0: Select left aligned mode.
 - ▶ bit 1: Select right aligned mode.
- ▶ **Byte 11:** stores eight flags that configure which sample rates are supported. At least 1 bit should be set:
 - ▶ bit 0: 48 KHz supported
 - ▶ bit 1: 96 KHz supported
 - ▶ bit 2: 192 KHz supported

- ▶ bit 3: 384 KHz supported (ignored if bit 2 of Byte 9 is 0)
- ▶ bit 4: 44.1 KHz supported
- ▶ bit 5: 88.2 KHz supported
- ▶ bit 6: 176.4 KHz supported
- ▶ bit 7: 352.8 KHz supported (ignored if bit 2 of Byte 9 is 0)
- ▶ **Bytes 12-19:** Reserved, store 0x00.

A.2.2 Byte 20 and further

From byte 20 onwards the USB strings are stored following one after the other:

- ▶ The Vendor/Manufacturer String, the name of your company.
- ▶ The Product String, the name of the product.
- ▶ The Serial number String, the serial number of the product.

All strings are stored as a *length byte* followed by the string itself as unicode characters in UTF-16LE format. The length byte counts the number of bytes used for the string. Near the end of this section, we will show some examples, and how to build unicode strings.

The strings are followed by bytes specifying the Language ID as described by USB.org, for example it is 0x0409 for English and it is stored with LSB first.

Immediately after the Language ID follows a stream of bytes that describe events and associated I2C write-commands or GPIO commands that can be used to configure external hardware, CODECs, etc. An event refers to an asynchronous change in the system like sample frequency change, USB connected/disconnected etc.

Each section comprises an EVENT (a byte with a value in the range 0x00 to 0x7E called event ID) followed by one or more COMMANDS. A COMMAND can be a single byte GPIO command, single byte sleep command or a three-byte I2C write command.

- ▶ GPIO commands will pull a specific GPIO pin high or low.
- ▶ Sleep command enables to provide delay inbetween command execution.
- ▶ I2C commands comprise an I2C bus-address, an I2C register number, and an I2C register value; these three bytes will be sent over the I2C bus at 100 KHz.

A.2.3 Events

Figure 19 shows the different possible events and their IDs:

Event ID	Description
0x00	48 KHz selected
0x02	96 KHz selected
0x04	192 KHz selected
0x06	384 KHz selected
0x08	44.1 KHz selected
0x0A	88.2 KHz selected
0x0C	176.4 KHz selected
0x0E	352.8 KHz selected
0x14	Audio streaming started
0x16	Audio streaming stopped
0x18	Initialisation event (called once at the beginning)
0x1A	USB connected
0x1C	USB disconnected
0x1E	DSD mode selected
0x20	PCM mode selected
0x22	DSD128 selected
0x24	DSD64 selected
0xFE	No more events (used to terminate the sequence)

Figure 19:
Event IDs

A.2.4 Commands

The one-byte GPIO and Sleep commands supported are listed in Figure 20.

Command ID	Description
0xD0	Set GPIO 0 low.
0xD2	Set GPIO 1 low.
0xD4	Set GPIO 2 low.
0xD6	Set GPIO 3 low.
0xD8	Set GPIO 4 low.
0xDA	Set GPIO 5 low.
0xDC	Set GPIO 6 low.
0xDE	Set GPIO 7 low.
0xE0	Set GPIO 0 high.
0xE2	Set GPIO 1 high.
0xE4	Set GPIO 2 high.
0xE6	Set GPIO 3 high.
0xE8	Set GPIO 4 high.
0xEA	Set GPIO 5 high.
0xEC	Set GPIO 6 high.
0xEE	Set GPIO 7 high.
0xF0	Sleep 1 ms.
0xF2	Sleep 10 ms.
0xF4	Sleep 100 ms.

Figure 20:
Command
IDs

The three-byte I2C write commands supported are:

- ▶ 0bAAAA AAA1, 0xRR, 0xVV: where
 - ▶ AAAAAA are the I2C address bits (7 bits),
 - ▶ 0xRR is the register number,
 - ▶ 0xVV is the register value.

A.2.5 Example

For example, let us consider the following byte sequence is the configuration.

```
0x34, 0x00, 0xA5, 0x00
0x33, 0x71, 0xDE, 0xAD, 0xFA, 0x00,
0x00, 0xFF, 0x00, 0x00, 0x00, 0x00,
0x00, 0x00, 0x00, 0x00,
0x08, 0x00, 0x58, 0x00, 0x4D, 0x00, 0x4F, 0x00, 0x53,
0x08, 0x00, 0x78, 0x00, 0x48, 0x00, 0x52, 0x00, 0x41,
0x04, 0x00, 0x31, 0x00, 0x30, 0x09, 0x04,
0x14, 0xE2, 0x00, 0x11, 0x56, 0x00, 0xEE, 0xDC,
0xFE
```

The above bytes in flash means:

- ▶ 0x34, 0x00: Length field denoting (0x0034) 52 bytes in configuration.
- ▶ 0xA5, 0x00: Marker bytes.
- ▶ 0x33 0x71: VID 0x7133 (two bytes at address 4 and 5)
- ▶ 0xDE 0xAD: PID 0xADDE (two bytes at address 6 and 7)
- ▶ 0xFA: USB power - 500mA (one byte at address 8)
- ▶ 0x00: Straps all low: i.e., self powered, UAC 2.0, No 384 KHz and HID inputs disabled. (byte at address 9)
- ▶ 0x00: Use default I2S mode. (byte at address 10)
- ▶ 0xFF: Enable all sample rates (byte at address 11)
- ▶ 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00: Reserved bytes (bytes 12..19)
- ▶ 0x08 0x58 0x00 0x4D 0x00 0x4F 0x00 0x53 0x00: Vendor string, uses 8 bytes (0x08), 0x58 0x00 ('X'), 0x4D 0x00 ('M'), 0x4F 0x00 ('O'), 0x53 0x00 ('S'), forms the string "XMOS".
- ▶ 0x08 0x78 0x00 0x48 0x00 0x52 0x00 0x41 0x00: Product string, uses 8 bytes (0x08), 0x78 0x00 ('x'), 0x48 0x00 ('H'), 0x52 0x00 ('R'), 0x41 0x00 ('A') forms the string "xHRA".
- ▶ 0x04 0x31 0x00 0x30 0x00: Serial number string, uses 4 bytes (0x04), the unicode characters are 0x31 0x00 ('1') and 0x30 0x00 ('0'), forming the string "10".
- ▶ 0x09 0x04: Language ID 0x0409 corresponds to "English (United States)".
- ▶ 0x14: If Audio stream is started (event).
 - ▶ 0xE2: Set GPIO 1 High (command).
- ▶ 0x00: If 48 KHz sample rate is selected (event)
 - ▶ 0x11 0x56 0x00: Write the value 0x00 to register 0x56 of I2C device 0x11 (Device address 0x10, with write bit (LSB) set).
 - ▶ 0xEE: Set GPIO 7 High.
 - ▶ 0xDC: Set GPIO 6 Low.
- ▶ 0xFE: No more events

A.2.6 Default behaviour

If no flash configuration is present, the following default values are used:

- ▶ The VID defaults to the XMOS vendor ID, 0x20B1.
- ▶ The PID defaults to a value that depends on the device part.
- ▶ The vendor string defaults to "XMOS"
- ▶ The product string defaults to a value that depends on the device part.
- ▶ The serial number defaults to none.

In addition to this, there is a default set of events that are used if there is no flash configuration found.

- ▶ 0x14 0xE0: if audio stream started, set GPIO 0 high.
- ▶ 0x16 0xD0: if audio stream stopped, set GPIO 0 low.
- ▶ 0x1A 0xE4: if USB connected, set GPIO 1 high.
- ▶ 0x1C 0xD4: if USB disconnected, set GPIO 1 low.
- ▶ 0x1E 0xE4: if DSD mode selected, set GPIO 2 high.
- ▶ 0x20 0xD4: if PCM mode selected, set GPIO 2 low.
- ▶ 0x00 0xE6 0xD8 0xDA:
if 48 KHz selected, set GPIO 3 high, GPIO 4 low, GPIO 5 low.
- ▶ 0x02 0xE6 0xE8 0xDA:
if 96 KHz selected, set GPIO 3 high, GPIO 4 high, GPIO 5 low.
- ▶ 0x04 0xE6 0xD8 0xEA:
if 192 KHz selected, set GPIO 3 high, GPIO 4 low, GPIO 5 high.
- ▶ 0x06 0xE6 0xE8 0xEA:
if 384 KHz selected, set GPIO 3 high, GPIO 4 high, GPIO 5 high.
- ▶ 0x08 0xD6 0xD8 0xDA:
if 44.1 KHz selected, set GPIO 3 low, GPIO 4 low, GPIO 5 low.
- ▶ 0x0A 0xD6 0xE8 0xDA:
if 88.2 KHz selected, set GPIO 3 low, GPIO 4 high, GPIO 5 low.
- ▶ 0x0C 0xD6 0xD8 0xEA:
if 176.4 KHz selected, set GPIO 3 low, GPIO 4 low, GPIO 5 high.
- ▶ 0x0E 0xD6 0xE8 0xEA:
if 352.8 KHz selected, set GPIO 3 low, GPIO 4 high, GPIO 5 high.
- ▶ 0xFE: No more events

These are disabled when any event is present in the flash, and should hence be added to flash if this behaviour is expected.

Figure 21 shows the GPIO state changes corresponding to the sample rate change events.

Active Sample rate	GPIO_3 (MCLK_SEL)	GPIO_5 (S_SP_1)	GPIO_4 (S_SP_0)
48 KHz	1	0	0
96 KHz	1	0	1
192 KHz	1	1	0
384 KHz	1	1	1
44.1 KHz	0	0	0
88.2 KHz	0	0	1
176.4 KHz	0	1	0
352.8 KHz	0	1	1
In DSD mode			
DSD64	0	X	0
DSD128	0	X	1

Figure 21:
Sample rate
encoding

B Schematics Design Check List

- ✓ This section is a checklist for use by schematics designers using the XHRA-2HPA. Each of the following sections contains items to check for each design.

B.1 Power supplies

- VDDIO supply is within specification before the VDD (core) supply is turned on. Specifically, the VDDIO supply is within specification before VDD (core) reaches 0.4V (Section 7.3).
- The VDD supply ramps monotonically (rises constantly) from 0V to its final value (0.95V - 1.05V) within 10ms (Section 7.3).
- The VDD supply is capable of supplying 300 mA (Section 7.3).
- PLLVDD is filtered with a low pass filter, for example an RC filter, see Section 7.3

B.2 Power supply decoupling

- The design has multiple decoupling capacitors per supply, for example at least four 0402 or 0603 size surface mount capacitors of 100nF in value, per supply (Section 7.3).
- A bulk decoupling capacitor of at least 10uF is placed on each supply (Section 7.3).

B.3 Power on reset

- The RST_N pin is asserted (low) during or after power up. The device is not used until this reset has taken place. A voltage supervisor type reset device is recommended to guarantee a good reset. This also has the benefit of resetting the system should the relevant supply go out of specification.

B.4 Clock

- The CLK input pin is supplied with a clock with monotonic rising edges and low jitter.

C PCB Layout Design Check List

- ✓ This section is a checklist for use by PCB designers using the XHRA-2HPA. Each of the following sections contains items to check for each design.

C.1 Ground Plane

- Multiple vias (eg, 9) have been used to connect the center pad to the PCB ground plane. These minimize impedance and conduct heat away from the device. (Section 7.5).
- Other than ground vias, there are no (or only a few) vias underneath or closely around the device. This create a good, solid, ground plane.

C.2 Power supply decoupling

- The decoupling capacitors are all placed close to a supply pin (Section 7.3).
- The decoupling capacitors are spaced around the device (Section 7.3).
- The ground side of each decoupling capacitor has a direct path back to the center ground of the device.

C.3 PLLVDD

- The PLLVDD filter (especially the capacitor) is placed close to the PLLVDD pin (Section 7.3).

D Associated Design Documentation

Document Title	Information	Document Number
xCORE-AUDIO HiRes-2 DAC/HPA Reference Platform Hardware Manual	Reference design manual	X3357

E Related Documentation

All datasheets of this family (including this one) are listed below:

Document Title	Information	Document Number
XHRA-2HPA Datasheet	Datasheet 2 channel output	Xxxxx

F Revision History

Date	Description
2015-05-01	Preliminary release
2015-05-19	Updated configuration and block diagram
2015-07-03	Added supported QSPI flash devices and minor text changes
2015-07-09	Updated DC characterisitcs



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