

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

# LC823433TA

## Audio Processing System LSI for MP3 Record and Playback Devices



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

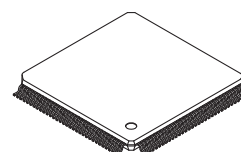
### Overview

LC823433TA is an audio processing system for MP3 record and playback devices.

It integrates DSP for digital signal processing and analog blocks such as audio ADC, audio DAC, and speaker and headphone amplifier in addition to LCD segment driver.

### Features

- 32-bit LPDSP32
  - SRAM (246 KB)
    - PM 75 KB (40 KB + 35 KB : ISOLATED)
    - DMA 170 KB (16 KB + 154 KB:ISOLATED)
    - DMB 1 KB (ISOLATED)ISOLATED area : Power ON/OFF control is available by register.
  - ROM (264.5 KB)
    - PM 227.5 KB (ISOLATED)
    - DMA 34 KB (ISOLATED)
    - DMB 3 KB (ISOLATED)ISOLATED area : Power ON/OFF control is available by the register.
  - SIO (Clock Serial IO 2 ch)
    - SIO0 : Ch0 eSIO (Clock speed = Sysclk/1 (max))  
program load and execute is possible using Serial Flash  
(after internal ROM Boot)
    - SIO1 : Ch1 SIO (Clock speed = Sysclk/8 (max))
  - UART (1 ch)
  - I<sup>2</sup>C (1 ch Single Master, Full/Standard)
  - Plain Timer (2 ch)
    - Timer0 : w/ Watch Dog Timer
    - Timer1 : w/o Watch Dog Timer and XT1 operation
  - Multiple Timer (2 ch)  
PWM output (1 ch)
  - RTC (Real Time Clock)  
Operating voltage is independent of internal core operating voltage.  
Only RTC power supply can be active during all others inactive (ISOLATED).



TQFP128 14x14 / TQFP128L

Continued on next page.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

Continued from preceding page.

- SD card IF (2 ch) (w/o CPRM)  
eSD/eMMC can be connected.
  - SD ch0 : program load and execute using eSD/eMMC (after internal ROM Boot) is possible.
  - SD ch1 : SD card
- USB2.0 (480M bps/12M bps) Device IF. built-in PHY
- 10 bit A/D converter (3 ch)
- GPIO (31 ch)  
(GPIOs share the terminals with other functions. Refer to the terminal list in detail).
  - LCD controller, LCD Driver. 18SEG \* 8COM, 1/8Duty, 1/4Bias
- Internal ROM Boot is possible.
- Firmware writing function.  
The firmware reading from SD ch1 and writing to the following devices:
  - Serial Flash connected SIO0.
  - eMMC/eSD connected SD ch0.
- JTAG (for debugger)
  
- Audio Functions
  - Record and Playback
    - Compression method : MP3<sup>1</sup> (MPEG1/2/2.5 Layer3). Stereo/Mono compatible.
    - Sampling frequencies : 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz
    - Bitrate : 8k bps (\*1) to 320k bps (for Decoder-VBR)  
(\*1) Encoder supports only Mono (one channel) for 8k bps.
  - Adjusting the playback speed
    - Fast playback : 1.0 times to 2.0 times 10 steps.
    - Slow playback : 0.5 times to 1.0 times 10 steps.
  - Multipurpose filter
  - Audio data automatic transfer function
    - The audio buffer executes the data transfer between internal SRAM (DMA) and the audio block.  
Wait cycle(s) is inserted to the LPDSP32 access to the SRAM while the audio buffer accesses to internal SRAM(DMA).
  - Digital volume, digital mute, BEEP, and level meter
    - The interrupt generation function at the operation completion  
(e.g. interrupt at mute completion).
  - Audio timer
    - LR clock count and the interrupt generation function.
  - Flexible PCM audio interface (two interfaces)
    - Master/Slave Mode Selectable
    - Data Formats : I<sup>2</sup>S mode etc.
  - Sample Rate Converters
    - 0.5 times to 64 times conversion range.
  - Digital microphone IF (2 ch)

Continued on next page.

---

<sup>1</sup> MPEG Layer-3 audio coding technology licensed from Fraunhofer IIS and Thomson.

Supply of this product does not convey license nor imply any right to distribute content created with this product in revenue-generating broadcast systems (terrestrial, satellite, cable and/or other distribution channels), streaming applications (via Internet, intranets and/or networks), other content distribution systems (pay-audio or audio-on-demand applications and the like) or on physical media (compact discs, digital versatile discs, semiconductor chips, hard drives, memory cards and the like).

Supply of this product does not convey license under the relevant intellectual property of Thomson and/or Fraunhofer Gesellschaft nor imply any right to use this product in any finished end user or ready-to-use final product. An independent license for such use is required. For details, please visit <http://mp3licensing.com/>.

Continued from preceding page.

- Analog function

- Microphone amplifier 0 / 18 / 24 / 30 dB (2 ch)
- PGA with ALC -12 dB to 35.25 dB in 0.75 dB steps (2 ch)
- 16-bit  $\Delta\Sigma$ ADC (2 ch)
- Digital filter for 16-bits  $\Delta\Sigma$ DAC (2 ch)
- AB class amplifier

The power supply only to AB class amplifier is possible (ISOLATED).

Thermal shutdown circuit built-in

- Speaker amplifier (1 ch BTL) 1dB to 4.5 dB in 0.5 dB steps  
Maximum output 300 mW @3.0 V, Speaker = 8[ $\Omega$ ], 1 dB
- Headphone amplifier (2 ch) 0 dB to 3 dB in 1 dB steps (Only same gain setting to 2 ch is possible)  
Maximum output 5 mW @3.0 V, HeadPhone = 16[ $\Omega$ ], Rd (Series) = 33[ $\Omega$ ], 1 dB

- Clock

- RCOSC : Internal RC oscillation. 1 MHz (TYP)
- XT1 : Main XTAL. 32.768 kHz.  
Used as an original oscillation of the system clock and the audio clock, and a RTC clock.
- XT2 : Optional XTAL. 12 MHz (TYP) etc.
- PLL1 : For system clock generation (LPDSP32 is included).
- PLL2 : For audio clock generation

## Specification

- Supply voltage : 1.3 V (core, etc), 3.15 V (Audio, USB, etc)
- Maximum operation frequency : 42 MHz (DSP@1.3 V)
- Package : 128 pin TQFP

## Application

- IC Recorder, Audio Player
- Radio Recorder, Home Audio (Mini compo)

**Specifications**

**Absolute Maximum Ratings** at  $V_{SS} = 0\text{ V}$

Parameter	Symbol	Domain of applicability	Ratings	Unit
Supply voltage	V <sub>DD1</sub> V <sub>DDRTC</sub> A <sub>VDDPLL1</sub> A <sub>VDDPHY1</sub>		-0.3 to +1.8	V
	V <sub>DD2</sub> V <sub>DDLCD</sub> A <sub>VDDPLL2</sub> A <sub>VDDADC</sub> A <sub>VDDAADC</sub> A <sub>VDDADAC</sub> A <sub>VDDSPAMP</sub> A <sub>VDDPHY2</sub>		-0.3 to +3.96	V
Input voltage	V <sub>I</sub>		-0.3 to *V <sub>DD</sub> *+0.3 (Max 3.96)	V
Operating temperature	T <sub>opr</sub>		-20 to +75	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Recommended Operating Conditions** at  $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD1</sub>		1.15	1.3	1.65	V
	V <sub>DDRTC</sub>		0.9	1.5	1.65	V
	A <sub>VDDPLL1</sub>		1.15	1.3	1.65	V
	V <sub>DD2</sub>		2.7	3.15	3.3	V
	V <sub>DDLCD</sub>		2.7	3.15	3.3	V
	A <sub>VDDPLL2</sub>		2.7	3.15	3.3	V
	A <sub>VDDADC</sub>		2.7	3.15	3.3	V
	A <sub>VDDAADC</sub>		2.7	2.8	3.3	V
	A <sub>VDDADAC</sub>		2.7	2.8	3.3	V
	A <sub>VDDSPAMP</sub>		1.8	3.15	3.8	V
	A <sub>VDDPHY1</sub>		1.35	1.5	1.65	V
A <sub>VDDPHY2</sub>		3.0	3.15	3.6	V	
Input voltage	V <sub>IN</sub>		0		*V <sub>DD</sub> *	V
	V <sub>IN3</sub> (RTC)		0		3.6	V
	V <sub>IN_ADC</sub> (AN0-AN2).	I <sub>AN</sub> < 300 $\mu\text{A}$	0		3.3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# LC823433TA

**DC Characteristics** at  $T_a = -20^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ,  $V_{DD1} = 1.15\text{ V}$  to  $1.65\text{ V}$ ,  $V_{DD2} = 2.7\text{ V}$  to  $3.3\text{ V}$ ,  
 $V_{DDRTC} = 0.9\text{ V}$  to  $1.65\text{ V}$

Parameter	Symbol	Application	Test Conditions	min	typ	max	Unit
Input high voltage	$V_{IH}$	3ICUD		$0.7 \times V_{DD2}$			V
		3IS, 3ISUD	Schmitt	$0.75 \times V_{DD2}$			V
		1IC		$0.7 \times V_{DDRTC}$			V
		1IS	Schmitt	$0.7 \times V_{DDRTC}$			V
Input low voltage	$V_{IL}$	3ICUD				$0.3 \times V_{DD2}$	V
		3IS, 3ISUD	Schmitt			$0.25 \times V_{DD2}$	V
		1IC				$0.2 \times V_{DDRTC}$	V
		1IS	Schmitt			$0.2 \times V_{DDRTC}$	V
Input high leakage current	$I_{IH}$	3ICUD, 3IS, 3ISUD	$V_{IN} = V_{DD2}$			10	$\mu\text{A}$
		1IC, 1IS	$V_{IN} = 3.3\text{V}$			10	$\mu\text{A}$
Input low leakage current	$I_{IL}$	3IS, 3ISUD	$V_{IN} = V_{SS}$	-10			$\mu\text{A}$
		1IC, 1IS	$V_{IN} = V_{SSRTC}$	-10			$\mu\text{A}$
Output high voltage	$V_{OH}$	3T2	$I_{OH} = -2\text{ mA}$	$V_{DD2}-0.4$			V
		3T4	$I_{OH} = -4\text{ mA}$	$V_{DD2}-0.4$			V
		3T4(8)	$I_{OH} = -4\text{ mA}$ ( $I_{OH} = -8\text{ mA}$ )	$V_{DD2}-0.4$			V
		3T6(12)	$I_{OH} = -6\text{ mA}$ ( $I_{OH} = -12\text{ mA}$ )	$V_{DD2}-0.4$			V
Output low voltage	$V_{OL}$	3T2	$I_{OL} = 2\text{ mA}$			0.4	V
		3T4	$I_{OL} = 4\text{ mA}$			0.4	V
		3T4(8)	$I_{OL} = 4\text{ mA}$ ( $I_{OL} = 8\text{ mA}$ )			0.4	V
		3T6(12)	$I_{OL} = 6\text{ mA}$ ( $I_{OL} = 12\text{ mA}$ )			0.4	V
		OD3	$I_{OL} = 0.3\text{ mA}$			0.3	V
Output leakage current	$I_{OZ}$	3T2, 3T4, 3T4(8), 3T6(12)	When it outputs Hi-Z	-10		10	$\mu\text{A}$
Pull-up resistor	Rup	3ICUD, 3ISUD		30	80	190	k $\Omega$
Pull-down resistor	Rdn	3ICUD, 3ISUD		30	80	190	k $\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

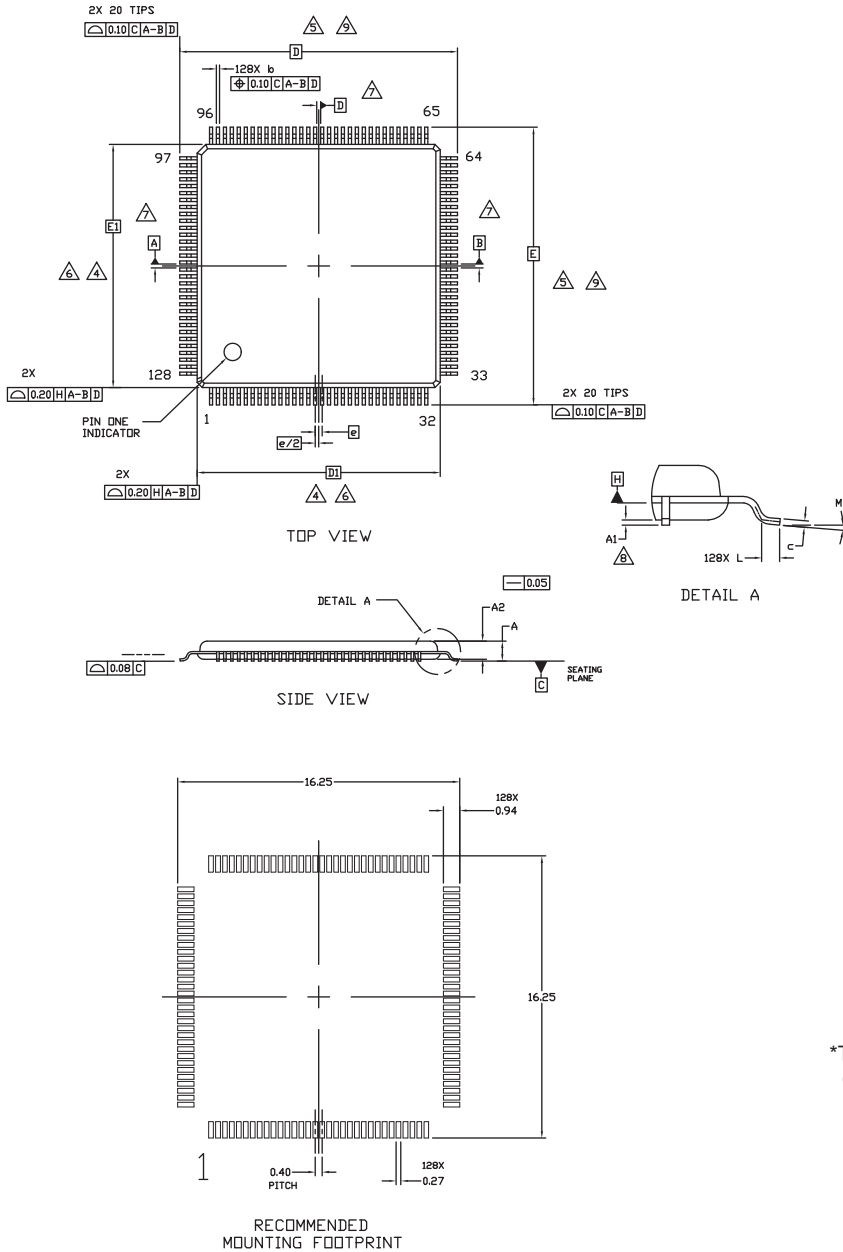
Package Dimensions

unit : mm

TQFP128 14x14 / TQFP128L

CASE 932BA

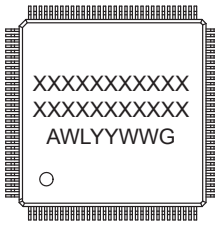
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MFC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
  4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
  5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
  6. DIMENSIONS D1 AND E1 TO BE DETERMINED AT DATUM PLANE H.
  7. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
  8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
  9. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

DIM	MILLIMETERS	
	MIN.	MAX.
A	---	1.20
A1	0.05	0.15
A2	1.00 REF	
b	0.13	0.23
c	0.09	0.20
D	16.00 BSC	
D1	14.00 BSC	
E	16.00 BSC	
E1	14.00 BSC	
e	0.40 BSC	
L	0.45	0.75
M	0*	7*

GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

# LC823433TA

## Pin Assignment (Bonding Option)

Direction		Attribute			
I	Input pin	3IS	3 V Schmitt input	1IS	1 V Schmitt input (3 V tolerant correspondence)
O	Output pin	3ICUD	3 V CMOS input pull-up/down	1IC	1 V CMOS input (3 V tolerant correspondence)
B	Bidirectional pin	3ISUD	3 V Schmitt input pull-up/down	OD3	1 V 0.3 mA open drain output (3 V tolerant correspondence)
P	Power supply pin	3T2	3 V 2 mA tristate output		
		3T4	3 V 4 mA tristate output	X	Oscillation amplifier
		3T4(8)	Tristate output with 3 V 4 mA / 8 mA switch function	3A	3 V analog through
		3T6(12)	Tristate output with 3 V 6 mA / 12 mA switch function	1A	1 V analog through

TQFP128L Pin No.	Name	Direction	Attribute
1	AV <sub>SS</sub> SPAMP	P	
2	AV <sub>DD</sub> SPAMP	P	
3	AVREFSP	O	3A
4	HPINL/SPKINM	I	3A
5	HPINR	I	3A
6	AV <sub>SS</sub> ADAC	P	
7	OUTMR	O	3A
8	OUTML/OUTM	O	3A
9	AV <sub>DD</sub> ADAC	P	
10	AV <sub>SS</sub> AADC	P	
11	AVREF	O	3A
12	AV <sub>DD</sub> AADC	P	
13	AINL	I	3A
14	AINR	I	3A
15	AV <sub>DD</sub> ADC	P	
16	AN0	I	3A
17	AN1	I	3A
18	AN2	I	3A
19	V <sub>SS</sub>	P	
20	V <sub>DD2</sub>	P	
21	V <sub>DD1</sub>	P	
22	TIOCA0/P10	B/B	3ISUD/3T2
23	BMODE0	I	3IS
24	BMODE1	I	3IS
25	BMODE2	I	3IS
26	NRES	I	3IS
27	SDCLK1/MCLK1/P00	O/B/B	3ISUD/3T6(12)
28	SDCMD1/LRCK1/P02	B/O/B	3ISUD/3T4(8)
29	SDAT10/BCK1/P03	B/B/B	3ISUD/3T4(8)
30	SDAT11/DIN1/P04	B/I/B	3ICUD/3T4(8)
31	SDAT12/DOUT1/P05	B/O/B	3ICUD/3T4(8)
32	SDAT13/SDO1/P06	B/O/B	3ICUD/3T4(8)
33	SDWP1/SDI1/P01	I/I/B	3ISUD/3T2
34	SDCD1/SCK1/P0A	I/B/B	3ISUD/3T2
35	SDCLK0/P14	O/B	3ICUD/3T6(12)
36	V <sub>DD2</sub>	P	
37	V <sub>SS</sub>	P	
38	SDCMD0/P15	B/B	3ICUD/3T4(8)

Continued on next page.



## LC823433TA

Continued from preceding page.

TQFP128L Pin No.	Name	Direction	Attribute
39	SDAT03/P16	B/B	3ICUD/3T4(8)
40	SDAT02/P17/SYSCLK	B/B/O	3ICUD/3T4(8)
41	SDAT01/P18/AUD0CLK	B/B/O	3ICUD/3T4(8)
42	SDAT00/P19/AUD1CLK	B/B/O	3ICUD/3T4(8)
43	VSS	P	
44	XIN2	I	X
45	XOUT2	O	X
46	AVDDPHY1(+VDD1)	P	
47	AVSSPHY1	P	
48	AVSSPHY1	P	
49	RREF	B	3A
50	AVSSPHY2	P	
51	AVDDPHY2	P	
52	AVDDPHY2	P	
53	AVSSPHY2	P	
54	AVSSPHY2	P	
55	AVSSPHY2	P	
56	AVDDPHY2	P	
57	DP	B	3A
58	DM	B	3A
59	AVSSPHY2	P	
60	AVDDPHY2	P	
61	COM0	O	3A
62	COM1	O	3A
63	COM2	O	3A
64	COM3	O	3A
65	VDDLCD	P	
66	VLCD1	O	3A
67	VLCD2	O	3A
68	VLCD3	O	3A
69	VSS	P	
70	VDD1	P	
71	SEG0	O	3A
72	SEG1	O	3A
73	SEG2	O	3A
74	SEG3	O	3A
75	SEG4	O	3A
76	SEG5	O	3A
77	SEG6	O	3A
78	SEG7	O	3A
79	SEG8	O	3A
80	SEG9	O	3A
81	SEG10	O	3A
82	SEG11	O	3A
83	SEG12	O	3A
84	SEG13	O	3A
85	SEG14	O	3A
86	SEG15	O	3A
87	SEG16	O	3A
88	SEG17	O	3A
89	COM4	O	3A
90	COM5	O	3A

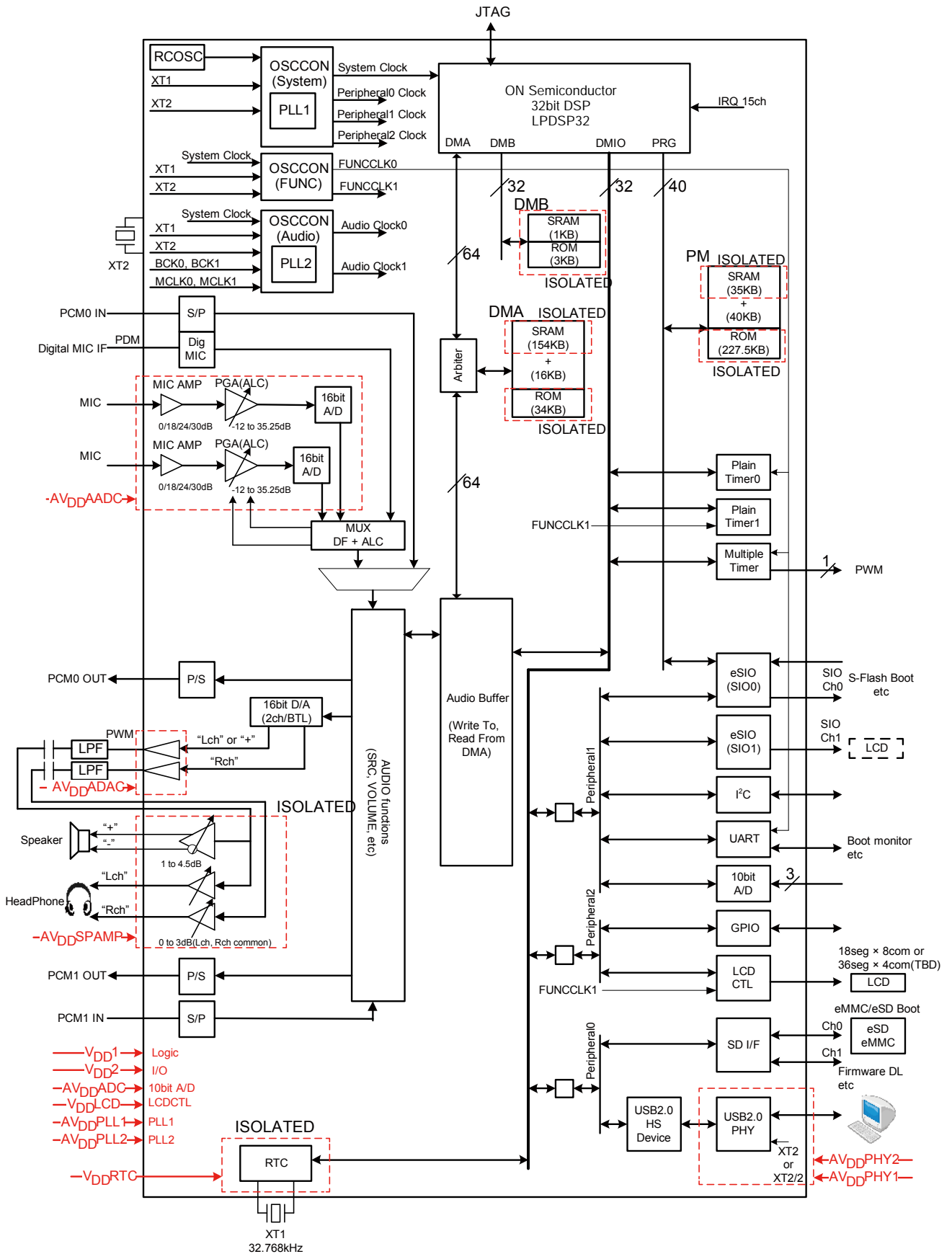
Continued on next page.

## LC823433TA

Continued from preceding page.

TQFP128L Pin No.	Name	Direction	Attribute
91	COM6	O	3A
92	COM7	O	3A
93	HPDET/SDI1/SCL/P1A	I/I/O/B	3ISUD/3T2
94	HPMUTE/SDO1/SDA/P1B	O/O/B/B	3ISUD/3T2
95	JTDO/P1C	O/B	3ICUD/3T2
96	JTDI/P1D	I/B	3ICUD/3T2
97	JTMS/P1E	I/B	3ICUD/3T2
98	JTCK/P1F	I/B	3ICUD/3T2
99	V <sub>DD1</sub>	P	
100	V <sub>DD2</sub>	P	
	SFMODE (Internal Signal)	I	3IS
101	V <sub>SS</sub>	P	
102	TXD/SCL/P12	O/O/B	3ISUD/3T2
103	RXD/SDA/P13	I/B/B	3ISUD/3T2
104	SCK0/P07	B/B	3ISUD/3T4
105	SDO0/P08	O/B	3ISUD/3T4
106	SDI0/P09	I/B	3ISUD/3T2
107	MCLK0/DMCKO/SCK1/P0B	B/O/B/B	3ISUD/3T2
108	DIN0/DMDIN/P0F	I/I/B	3ISUD/3T2
109	DOU0/P0E/NCS	O/B/O	3ISUD/3T2
110	KEYINT1	I	1IS
111	KEYINT0	I	1IS
112	RTCRSTB	I	1IC
113	PWRON	O	OD3
114	LINEFIXB	I	1IS
115	XOUT32K	O	X
116	XIN32K	I	X
117	V <sub>DDRTC</sub>	P	
	RTCMODE (Internal Signal)	I	1IS
118	V <sub>SSRTC</sub>	P	
119	AV <sub>DD</sub> PLL1	P	
120	VCNT1	O	1A
121	V <sub>SS</sub>	P	
122	AV <sub>DD</sub> PLL2	P	
123	VCNT2	O	3A
124	AV <sub>SS</sub> PLL2	P	
125	HPOUTR	O	3A
126	HPOUTL	O	3A
127	SPOUTP	O	3A
128	SPOUTN	O	3A

Block Diagram



Note

- Refer to the pin assignment for port share
- ISOLATED SRAMs and ROMs described in this figure can be power off by a register, in addition to the tiny SRAMs (not described in this figure) in the SD I/F, USB2.0, SRC, 16bit D/A, DF.

# LC823433TA

## Pin Functions

### • JTAG

Pin name	Pol.	Type	Description	Num.
JTDO/ P1C	-/ -	O/ B	JTAG test data output/ General purpose port	1
JTDI/ P1D	-/ -	I/ B	JTAG test data input/ General purpose port. The input level of the terminal JTDI is taken by rising edge of the terminal NRES. The value can be read as a register, and can be used as the operation mode setting.	1
JTMS/ P1E	-/ -	I/ B	JTAG test mode selection/ General purpose port The input level of the terminal JTMS is taken by rising edge of the terminal NRES. The value can be read as a register, and can be used as the operation mode setting.	1
JTCK/ P1F	Pos/ -	I/ B	JTAG test clock/ General purpose port	1
Total				4

### • RTC

Pin name	Pol.	Type	Description	Num.
XIN32K	Pos	I	32.768 kHz oscillation amplifier input (XT1)	1
XOUT32K	-	O	32.768 kHz oscillation amplifier output (XT1)	1
RTCRSTB (VDET)	Neg Neg	I I	RTC reset input There is an optional bonding as Power supply watch comparison input.	1
PWRON (RTCINT)	- Neg	O O	Main power supply ON/OFF control There is an optional bonding as RTC interrupt output.	1
LINEFIXB (BACKUPB)	Neg Neg	I I	RTC isolator cutting and the connection There is an optional bonding as RTC operation mode selection.	1
V <sub>DD</sub> RTC	-	P	RTC block power supply.	1
V <sub>SS</sub> RTC	-	P	RTC ground pin.	1
Total				7

## LC823433TA

• SIO (synchronous serial) interface Ch0 (eSIO)/Timer PWM output/General purpose port

Pin name	Pol.	Type	Description	Num.
SCK0/ P07	Pos/ -	B/ B	Serial I/F Ch0 clock/ General purpose port (It is possible to use it as an external interrupt input.)	1
SDO0/ P08	-/ -	O/ B	Serial I/F Ch0 data output/ General purpose port (It is possible to use it as an external interrupt input).	1
(SDO0(SIO0))	-(-)	O(B)	There is an optional bonding as serial I/F Ch0 data output (Data I/O 0 when at high speed operating).	
SDI0/ P09	-/ -	I/ B	Serial I/F Ch0 data input/ General purpose port (It is possible to use it as an external interrupt input).	1
(SDI0(SIO3))	-(-)	I(B)	There is an optional bonding as serial I/F Ch0 data input (Data I/O 3 when at high speed operating).	
TIOCA0/ P10	-/ -	B/ B	MTM Ch0 A input capture and output capture/ General purpose port	1
(V <sub>SS</sub> )	-	P	There is an optional bonding as V <sub>SS</sub> .	
Total				4

• UART (asynchronization serial) interface/I<sup>2</sup>C interface/General purpose port

Pin name	Pol.	Type	Description	Num.
TXD/ SCL/ P12	-/ -/ -	O/ O/ B	UART transmitted serial data output/ I <sup>2</sup> C clock output (open drain output)/ General purpose port (It is possible to use it as an external interrupt input).	1
RXD/ SDA/ P13	-/ -/ -	I/ B/ B	UART received serial data input/ I <sup>2</sup> C data (open drain output)/ General purpose port (It is possible to use it as an external interrupt input).	1
Total				2

• Headphone control/SIO (synchronous serial) interface Ch1 (SDI, SDO)/I<sup>2</sup>C interface/General purpose port

Pin name	Pol.	Type	Description	Num.
HPDET/ SDI1/ SCL/ P1A	Pos/ -/ -/ -	I/ I/ O/ B	Headphone insertion detection/ Serial I/F Ch1 data input/ I <sup>2</sup> C clock output (open drain output)/ General purpose port (It is possible to use it as an external interrupt input).	1
HPMUTE/ SDO1/ SDA/ P1B	Pos/ -/ -/ -	O/ O/ B/ B	Headphone mute/ Serial I/F Ch1 data output/ I <sup>2</sup> C data (open drain output)/ General purpose port	1
Total				2

## LC823433TA

- PCM interface Ch0/Digital mic interface/  
SIO (synchronous serial) interface Ch1 (SCK)/General purpose port/RTC (KeyInt RTC model)

Pin name	Pol.	Type	Description	Num.
MCLK0/ DMCKO/ SCK1/ P0B	Pos/ -/ -/ -	B/ O/ B/ B	PCM Ch0 master clock/ Digital mic clock output/ Serial I/F Ch1 clock/ General purpose port (It is possible to use it as an external interrupt input).	1
KEYINT1  (NHOLD(SIO1))  (BCK0/ P0C)	-  -  -/ -	I  O(B)  B/ B	KEY interrupt1 (Notes: Operate in V <sub>DD</sub> RTC and the V <sub>SS</sub> RTC power supply).  There is an optional bonding as serial I/F Ch0 hold output (Data I/O 1 when at high speed operating).  There is an optional bonding as PCM Ch0 bit clock/ General purpose port	1
KEYINT0  (NWP(SIO2))  (LRCK0/ P0D)	-  -  -/ -	I  O(B)  B/ B	KEY interrupt0 (Notes: Operate in V <sub>DD</sub> RTC and the V <sub>SS</sub> RTC power supply).  There is an optional bonding as serial I/F Ch0 write protect output (Data I/O 2 when high speed operating).  There is an optional bonding as PCM Ch0 LR clock/ General purpose port (It is possible to use it as an external interrupt input).	1
DIN0/ DMDIN/ P0F	-/ -/ -	I/ I/ B	PCM Ch0 data input/ Digital mic data input/ General purpose port (It is possible to use it as an external interrupt input).	1
DOUT0/ P0E/  NCS  (NCS)	-/ -/  Neg  Neg	O/ B/  O  O	PCM Ch0 data output/ General purpose port (It is possible to use it as an external interrupt input)/ CS for serial I/F Ch0 (When it boots from internal ROM and the program from SerialFlash connected to serial I/F Ch0 is loaded, it is used as CS control terminal of SerialFlash).  There is an optional bonding as CS for serial I/F Ch0.	1
Total				5

## LC823433TA

• SD interface Ch0/General purpose port

Pin name	Pol.	Type	Description	Num.
SDCLK0/ P14	Pos/ -	O/ B	SD card I/F Ch0 clock output/ General purpose port	1
SDCMD0/ P15	-/ -	B/ B	SD card I/F Ch0 command line/ General purpose port	1
SDAT03/ P16	-/ -	B/ B	SD card I/F Ch0 data 3/ General purpose port	1
SDAT02/ P17/ SYSCLK	-/ -/ -	B/ B/ O	SD card I/F Ch0 data 2/ General purpose port/ System Clock output (for evaluation)	1
SDAT01/ P18/ AUD0CLK	-/ -/ -	B/ B/ O	SD card I/F Ch0 data 1/ General purpose port/ Audio0 Clock output (for evaluation)	1
SDAT00/ P19/ AUD1CLK	-/ -/ -	B/ B/ O	SD card I/F Ch0 data 0/ General purpose port/ Audio1 Clock output (for evaluation)	1
Total				6

• SD interface Ch1/PCM interface Ch1/SIO (synchronous serial) interface Ch1/General purpose port

Pin name	Pol.	Type	Description	Num.
SDCLK1/ MCLK1/ P00	Pos/ Pos/ -	O/ O/ B	SD card I/F Ch1 clock output/ PCM Ch1 master clock/ General purpose port	1
SDCMD1/ LRCK1/ P02	-/ -/ -	B/ B/ B	SD card I/F Ch1 command line/ PCM Ch1 LR clock/ General purpose port	1
SDAT13/ SDO1/ P06	-/ -/ -	B/ O/ B	SD card I/F Ch1 data 3/ Serial I/F Ch1 data output/ General purpose port	1
SDAT12/ DOUT1/ P05	-/ -/ -	B/ O/ B	SD card I/F Ch1 data 2/ PCM Ch1 data output/ General purpose port	1
SDAT11/ DIN1/ P04	-/ -/ -	B/ I/ B	SD card I/F Ch1 data 1/ PCM Ch1 data input/ General purpose port	1
SDAT10/ BCK1/ P03	-/ -/ -	B/ B/ B	SD card I/F Ch1 data 0/ PCM Ch1 bit clock/ General purpose port	1
SDWP1/ SDI1/ P01	-/ -/ -	I/ I/ B	SD card I/F Ch1 write protect/ Serial I/F Ch1 data input/ General purpose port (It is possible to use it as an external interrupt input).	1
SDCD1/ SCK1/ P0A	-/ -/ -	I/ B/ B	SD card I/F Ch1 card detect/ Serial I/F Ch1 clock/ General purpose port (It is possible to use it as an external interrupt input).	1
Total				8

## LC823433TA

### • Oscillation amplifier and PLL

Pin name	Pol.	Type	Description	Num.
XIN2	Pos	I	Oscillation amplifier input for audio (XT2)	1
XOUT2	-	O	Oscillation amplifier output for audio (XT2)	1
VCNT1	-	O	VCO control for PLL1	1
AV <sub>DD</sub> PLL1	-	P	Analog power supply for PLL1	1
AV <sub>SS</sub> PLL1	-	P	Analog ground for PLL1	1
VCNT2	-	O	VCO control for PLL2	1
AV <sub>DD</sub> PLL2	-	P	Analog power supply for PLL2	1
AV <sub>SS</sub> PLL2	-	P	Analog ground for PLL2	1
Total				8

### • 10-bit A/D

Pin name	Pol.	Type	Description	Num.
AN[2:0]	-	I	ADC input	3
AV <sub>DD</sub> ADC	-	P	Power supply for ADC	1
V <sub>SS</sub> (AV <sub>SS</sub> ADC)	-	P	Ground for ADC. It connects V <sub>SS</sub> in LSI (terminal sharing). There is an optional bonding as dedicated ground AV <sub>SS</sub> ADC .	1
Total				5

### • Audio CODEC

Pin name	Pol.	Type	Description	Num.
AINL	-	I	Analog voice input Lch (stereo) Analog voice input (monaural).	1
AINR	-	I	Analog voice input Rch (stereo)	1
AVREF	-	O	Audio ADC reference output	1
AV <sub>DD</sub> AADC	-	P	Power supply for audio ADC	1
AV <sub>SS</sub> AADC	-	P	Ground for audio ADC	1
OUTML/ OUTM	-/ -	O/ O	Audio DAC PWM output (Lch for HP)/ Audio DAC PWM output (monaural for speaker)	1
OUTMR	-	O	Audio DAC PWM output (Rch for HP)	1
AV <sub>DD</sub> ADAC	-	P	Power supply for audio DAC	1
AV <sub>SS</sub> ADAC	-	P	Ground for audio DAC	1
HPINL/ SPKINM	-	I/ I	Headphone amplifier input (Lch) / Speaker amplifier input (monaural)	1
HPINR	-	I	Headphone amplifier input (Rch)	1
SPOUTP	-	O	AB class speaker amplifier output (+)	1
SPOUTN	-	O	AB class speaker amplifier output (-)	1
HPOUTL	-	O	Headphone amplifier output (Lch)	1
HPOUTR	-	O	Headphone amplifier output (Rch)	1
AVREFSP	-	O	AB class amplifier reference output	1
AV <sub>DD</sub> SPAMP	-	P	Analog power supply for AB class amplifier	1
AV <sub>SS</sub> SPAMP	-	P	Analog ground for AB class amplifier	1
Total				18



## LC823433TA

• LCD Driver (4COM/8COM bonding switch)

Pin name	Pol.	Type	Description	Num.
SEG[17:0]	-	O	Segment output for LCD	18
COM[7:4]	-	O	COM [7:4], Common driver output for LCD (when 8COM is used).	4
(SEG[21:18])	-	O	There is an optional bonding as segment outputs, SEG[21:18], for the LCD(when 4COM is used).	
COM[3:0]	-	O	Common driver output for LCD. •Both 8COM and 4COM ... COM[3:0].	4
VLCD1	-	O	LCD drive voltage output 1 •When 1/3 bias is used ... $2 * V_{DDLCD} / 3$ . •When 1/4 bias is used ... $3 * V_{DDLCD} / 4$ .	1
VLCD2	-	O	LCD drive voltage output 2 •When 1/3 bias is used ... $1 * V_{DDLCD} / 3$ . •When 1/4 bias is used ... $2 * V_{DDLCD} / 4$ .	1
VLCD3	-	O	LCD drive voltage output 3 •When 1/3 bias is used ... $1 * V_{DDLCD} / 3$ . •When 1/4 bias is used ... $1 * V_{DDLCD} / 4$ .	1
V <sub>DDLCD</sub>	-	P	3 V power supply for LCD driver	1
Total				30

# LC823433TA

• USB 2.0 HS Device/LCD Driver (bonding switch when 4COM is used)

Pin name	Pol.	Type	Description	Num.
DP	-	B	USB D+ (Device)	1
(SEG32)	-	O	There is an optional bonding as segment output 32 for LCD.	
DM	-	B	USB D- (Device)	1
(SEG33)	-	O	There is an optional bonding as segment output 33 for LCD.	
RREF	-	B	Reference resistance for USB PHY.	1
(SEG24)	-	O	There is an optional bonding as segment output 24 for LCD.	
AV <sub>DD</sub> PHY1	-	P	Analog 1.5 V power supply for USB PHY. It connects V <sub>DD1</sub> in LSI (terminal sharing).	1
AV <sub>SS</sub> PHY1	-	P	Analog ground for USB PHY.	1
(SEG22)	-	O	There is an optional bonding as segment output 22 for LCD.	
AV <sub>SS</sub> PHY1	-	P	Analog ground for USB PHY.	1
(SEG23)	-	O	There is an optional bonding as segment output 23 for LCD.	
AV <sub>DD</sub> PHY2	-	P	Analog 3.3 V power supply for USB PHY.	1
(SEG26)	-	O	There is an optional bonding as segment output 26 for LCD.	
AV <sub>DD</sub> PHY2	-	P	Analog 3.3 V power supply for USB PHY.	1
(SEG27)	-	O	There is an optional bonding as segment output 27 for LCD.	
AV <sub>DD</sub> PHY2	-	P	Analog 3.3 V power supply for USB PHY.	1
(SEG31)	-	O	There is an optional bonding as segment output 31 for LCD.	
AV <sub>DD</sub> PHY2	-	P	Analog 3.3 V power supply for USB PHY.	1
(SEG35)	-	O	There is an optional bonding as segment output 35 for LCD.	
AV <sub>SS</sub> PHY2	-	P	Analog ground for USB PHY.	1
(SEG25)	-	O	There is an optional bonding as segment output 25 for LCD.	
AV <sub>SS</sub> PHY2	-	P	Analog ground for USB PHY.	1
(SEG28)	-	O	There is an optional bonding as segment output 28 for LCD.	
AV <sub>SS</sub> PHY2	-	P	Analog ground for USB PHY.	1
(SEG29)	-	O	There is an optional bonding as segment output 29 for LCD.	
AV <sub>SS</sub> PHY2	-	P	Analog ground for USB PHY.	1
(SEG30)	-	O	There is an optional bonding as segment output 30 for LCD.	
AV <sub>SS</sub> PHY2	-	P	Analog ground for USB PHY.	1
(SEG34)	-	O	There is an optional bonding as segment output 34 for LCD.	
Total				15

# LC823433TA

• Power supply etc.

Pin name	Pol.	Type	Description	Num.
BMODE[2:0]	-	I	Operation mode selection	3
NRES	Neg	I	External reset and GPIO•LCD driver output force input •When it is active (L input), the state of the GPIO•LCD driver is forced, and LED lighting and the LCD display is controlled until reset depends on LSI. When Low is input : GPIO = Hiz, LCD = Low Fixed (PIOFIXB). •The state of JTDI and JTMS of JTAG is taken into the internal register by rising edge of NRES (for operation mode setting).	1
V <sub>DD1</sub>	-	P	Digital internal power supply There is one V <sub>DD1</sub> which is also connected with AV <sub>DD</sub> PHY1.	3
V <sub>DD2</sub>	-	P	Digital IO power supply	3
V <sub>SS</sub>	-	P	Digital ground There is one V <sub>SS</sub> which is also connected with AV <sub>SS</sub> ADC.	4
Total				14
Total				128

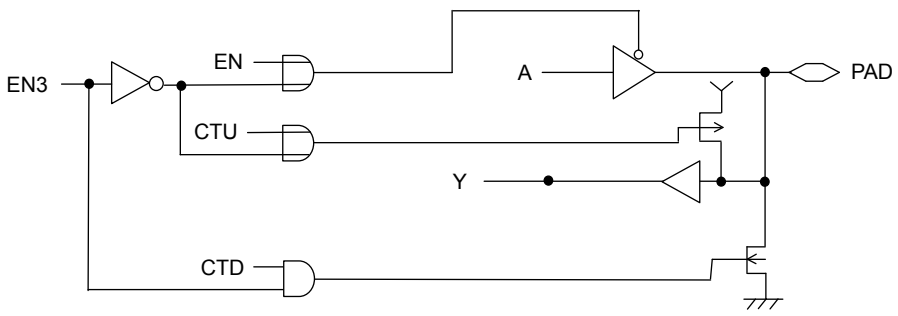
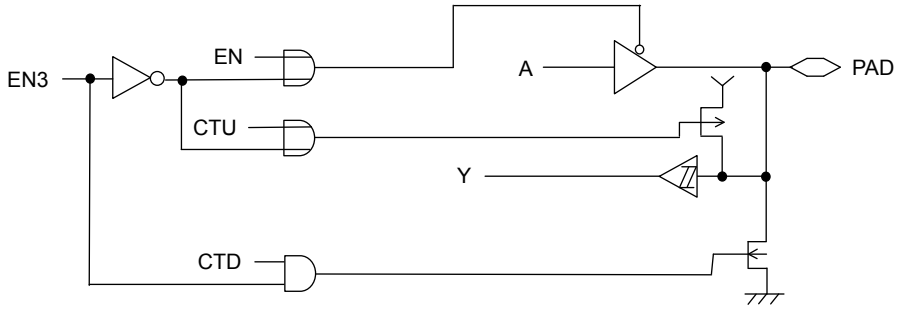
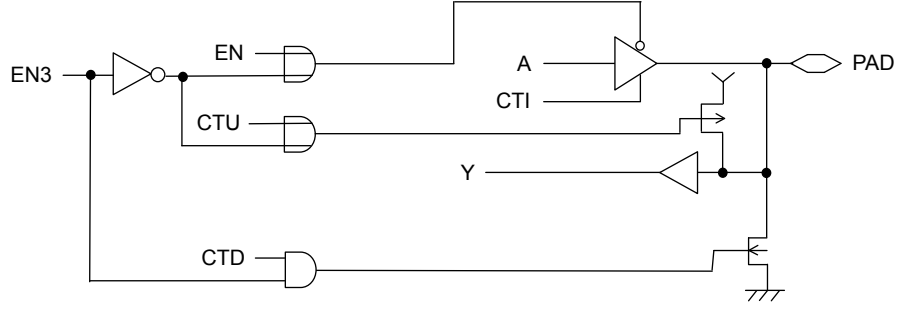
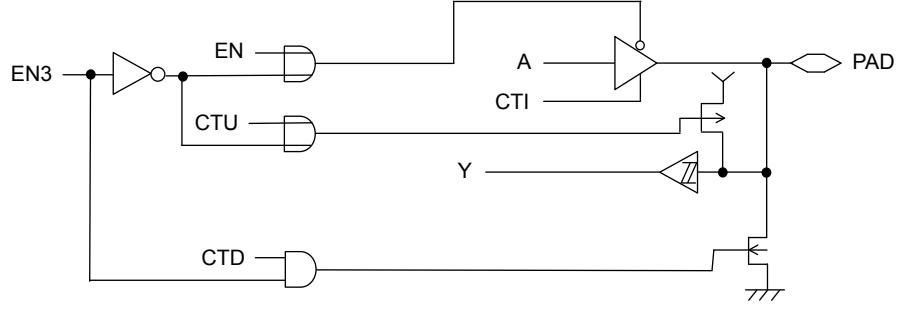
Notes : Do not open an unused digital input terminal or a digital bidirectional terminal of input state, and set Pull-up/Pull-down register in ON (only terminals with this function) or connect to digital IO power supply or digital ground.  
 Left open AINL, AINR, HPINL/SPKINM, and HPINR terminals if they are not used (do not fix to L or H).

## Operational mode

Various boot modes etc. can be selected by switching BMODE[2:0] terminal.

BMODE2	BMODE1	BMODE0	Operational mode
0	0	0	Internal ROM boot (eMMC Physical Boot - SD interface Ch0)
0	0	1	Internal ROM boot (IPL Boot - SD interface Ch0)
0	1	0	Internal ROM boot (Partition Boot - SD interface Ch0)
0	1	1	Internal ROM boot (External Serial Flash Boot - SIO (synchronous serial) interface Ch0)
1	0	0	Liberation of the terminal for SD interface Ch0 and SIO Ch0 (SDCLK0, SDCMD0, SDAT03, SDAT02, SDAT01, SDAT00, SCK0, SDO0, SDIO, and DOUT0 (NCS) are output Hiz).
1	0	1	Internal ROM boot (Deletion Partition area and IPL user area – SD interface Ch0 and SIO external Serial Flash Ch0)
1	1	0	LSI test mode (Do not set to this mode when working actually).
1	1	1	LSI test mode (Do not set to this mode when working actually).

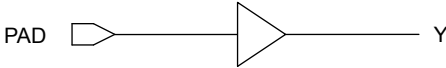
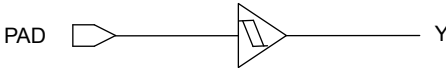
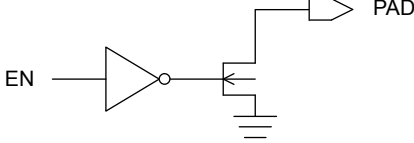
Pin Type

<p>3ICUD/ 3T2</p>	 <p>EN3 = 0: PAD is configured as input &amp; Pull_up OFF, Pull_down OFF, EN3 = 1 normal</p>
<p>3ISUD/ 3T2  3ISUD/ 3T4</p>	 <p>EN3 = 0: PAD is configured as input &amp; Pull_up OFF, Pull_down OFF, EN3 = 1 normal</p>
<p>3ICUD/ 3T4(8)  3ICUD/ 3T6(12)</p>	 <p>CTI current ability switch terminal 0: 4 mA 1: 8 mA / 0: 6 mA 1: 12 mA EN3 = 0: PAD is configured as input &amp; Pull_up OFF, Pull_down OFF, EN3 = 1 normal</p>
<p>3ISUD/ 3T4(8)  3ISUD/ 3T6(12)</p>	 <p>CTI current ability switch terminal 0: 4 mA 1: 8 mA / 0: 6 mA 1: 12 mA EN3 = 0: PAD is configured as input &amp; Pull_up OFF, Pull_down OFF, EN3 = 1 normal</p>

Continued on next page.

# LC823433TA

Continued from preceding page.

1IC	
1IS 3IS	
OD3	

## ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC823433TA-2H	TQFP128 14x14 / TQFP128L (Pb-Free / Halogen Free)	450 / Tray JEDEC

\* I<sup>2</sup>C Bus is a trademark of Philips Corporation.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.