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General Description

The ICS874001I-02 is a high performance Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874001I-02 has two different PLL bandwidth modes: 2MHz and 3MHz. The 2MHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 3MHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth mode. The 874001I-02 can be set for different modes using the F_SELx pins, as shown in Table 3C.

The ICS874001I-02 uses IDT's 3RD Generation FemtoClock® PLL technology to achieve the lowest possible phase noise. The device is packaged in a small 20-pin TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

Features

- One differential LVDS output pair
- One differential clock input
- CLK, nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Input frequency range: 98MHz to 128MHz
- Output frequency range: 98MHz to 640MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 15ps (maximum), 3.3V
- RMS period jitter: 3ps (maximum), 3.3V
- Two bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

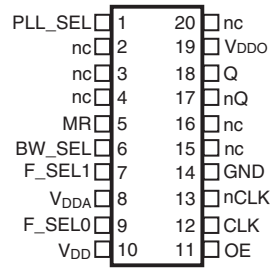
PLL Bandwidth Control Table

BW_SEL
0 = PLL Bandwidth: 2MHz (default)
1 = PLL Bandwidth: 3MHz

PLL_SEL Control Table

PLL_SEL
0 = Bypass
1 = VCO (default)

Pin Assignment



ICS874001I-02
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Block Diagram

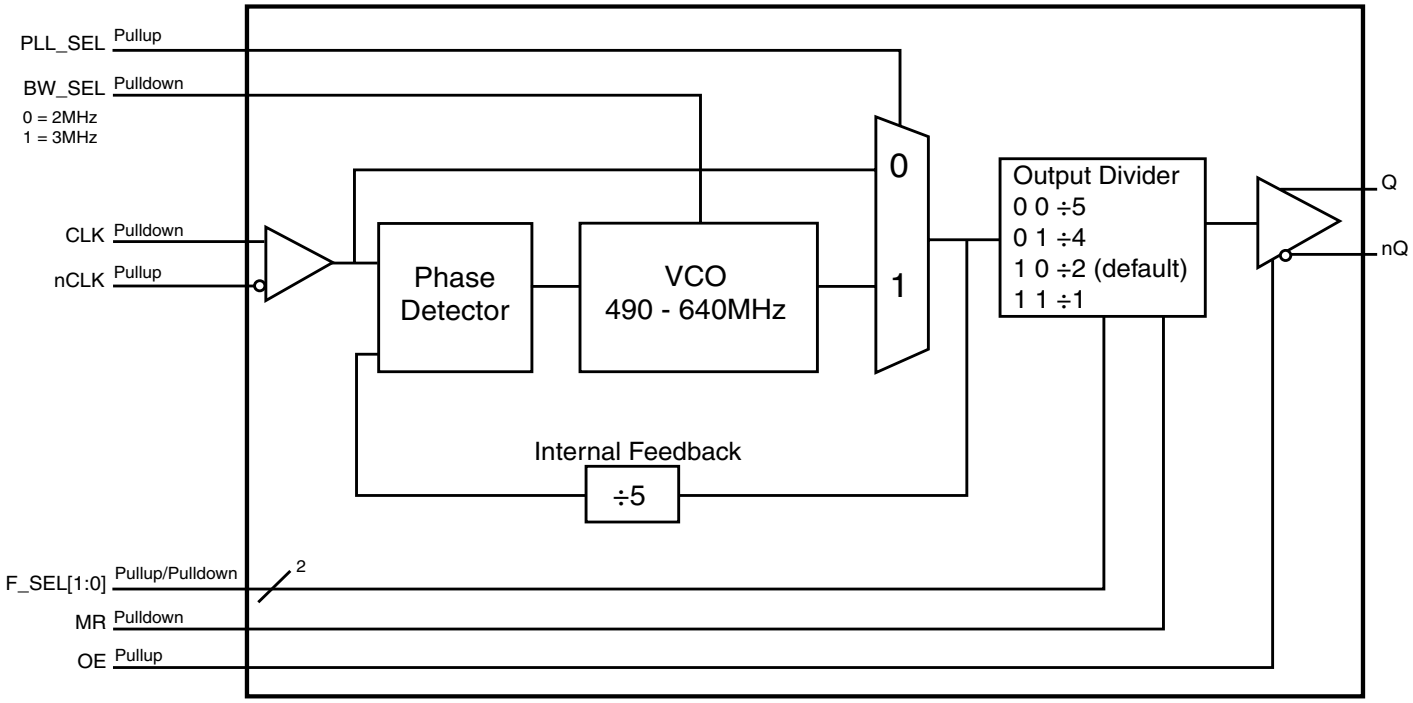


Table 1. Pin Descriptions

Number	Name	Type		Description
1	PLL_SEL	Input	Pullup	PLL select pin. When LOW, bypasses the VCO. When HIGH selects VCO. LVCMOS/LVTTL interface levels.
2, 3, 4, 15, 16, 20	nc	Unused		No connect.
5	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go LOW and the inverted output nQ to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	BW_SEL	Input	Pulldown	PLL Bandwidth select pin. LVCMOS/LVTTL interface levels. See Table 3B.
7	F_SEL1	Input	Pullup	Frequency select pin. See Table 3C. LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
9	F_SEL0	Input	Pulldown	Frequency select pin. See Table 3C. LVCMOS/LVTTL interface levels.
10	V_{DD}	Power		Core supply pin.
11	OE	Input	Pullup	Output enable. When HIGH, outputs are enabled. When LOW, forces outputs to High-Impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
17, 18	nQ, Q	Output		Differential output pair. LVDS interface levels.
19	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Inputs	Outputs
OE	**Q, nQ**
0	High-Impedance
1	Enabled

Table 3B. PLL Bandwidth Control Table

Inputs	
BW_SEL	**PLL Bandwidth**
0	2MHz (default)
1	3MHz

Table 3C. F_SELx Function Table

Input Frequency (MHz)	Inputs			Output Frequency (MHz)
	F_SEL1	**F_SEL0**	**Divider**	
100	0	0	÷5	100
100	0	1	÷4	125
100	1	0	÷2	250 (default)
100	1	1	÷1	500

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				72	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				24	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.12	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				70	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				22	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.465V$	-0.3		0.8	V
			$V_{DD} = 2.625V$	-0.3		0.7	V
I_{IH}	Input High Current	F_SEL0, MR, BW_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		F_SEL1, OE, PLL_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
I_{IL}	Input Low Current	F_SEL0, MR, BW_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		F_SEL1, OE, PLL_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA

Table 4D. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		nCLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		nCLK	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} – 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4E. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	390	480	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2	1.4	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4F. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	390	480	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.0	1.2	1.4	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		98		640	MHz
$t$jit(cc)	Cycle-to-Cycle Jitter; NOTE 1				15	ps
$t$jit(per)	RMS Period Jitter; NOTE 1			2	3	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	230		470	ps
odc	Output Duty Cycle	N ≠ 1	47		53	%
		N = 1	40		60	%

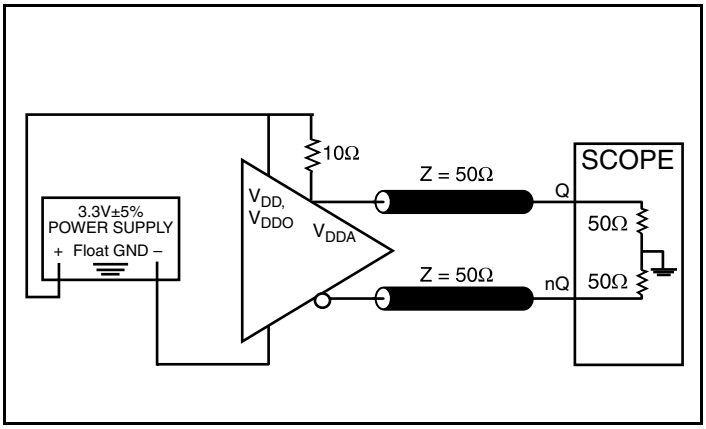
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

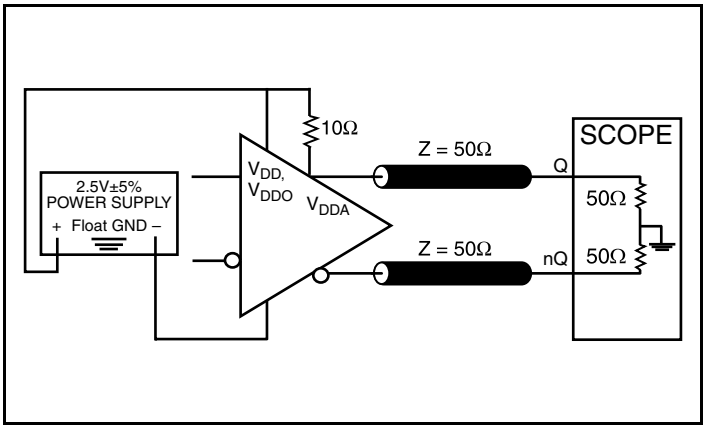
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		98		640	MHz
$t$jit(cc)	Cycle-to-Cycle Jitter; NOTE 1				20	ps
$t$jit(per)	RMS Period Jitter; NOTE 1			2	4	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	230		500	ps
odc	Output Duty Cycle	N ≠ 1	47		53	%
		N = 1	40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

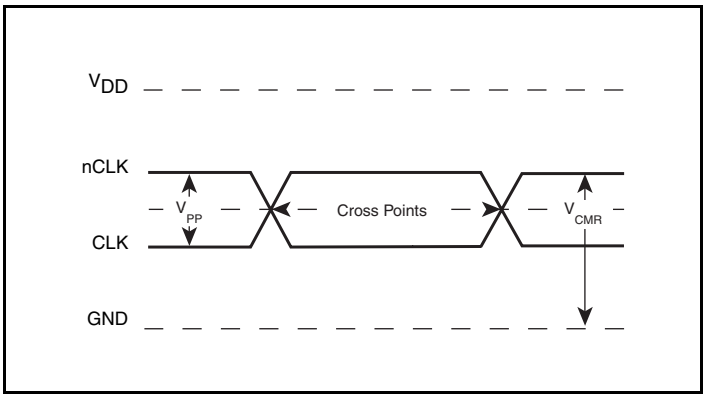
Parameter Measurement Information



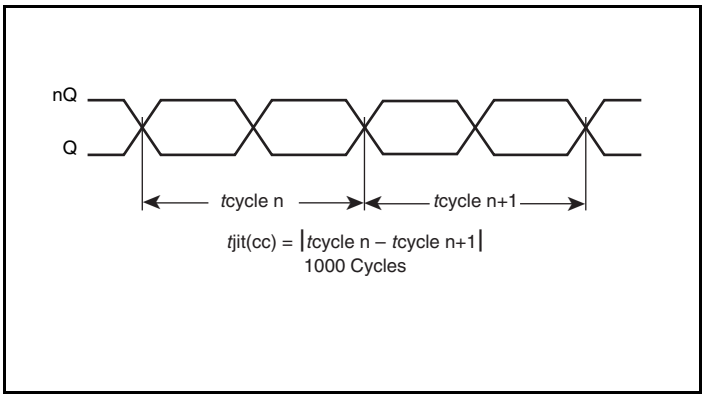
3.3V LVDS Output Load AC Test Circuit



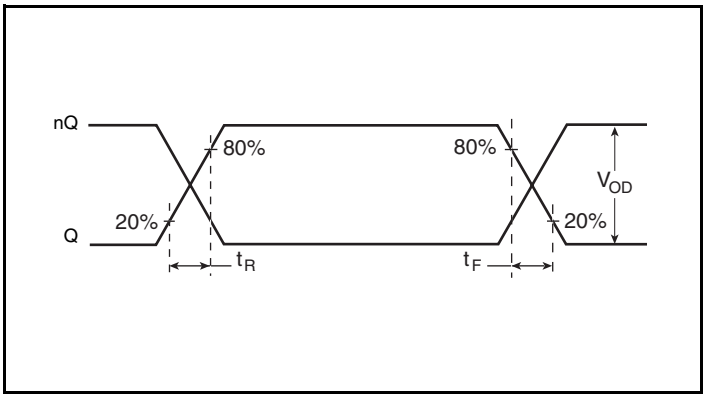
2.5V LVDS Output Load AC Test Circuit



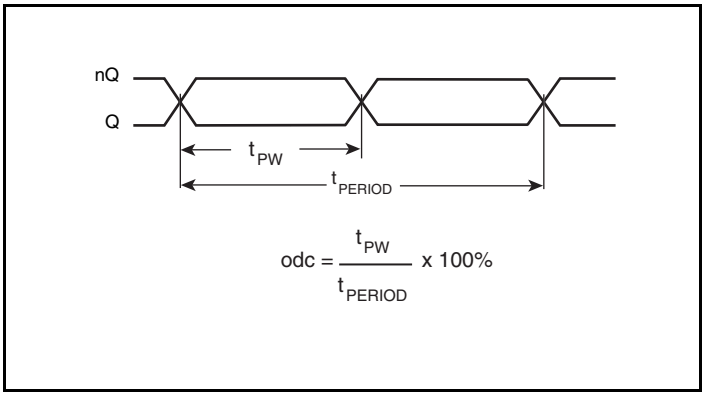
Differential Input Level



Cycle-to-Cycle Jitter

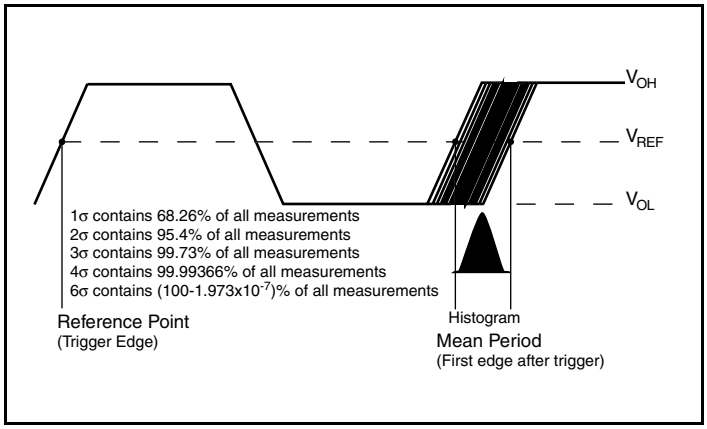


Output Rise/Fall Time

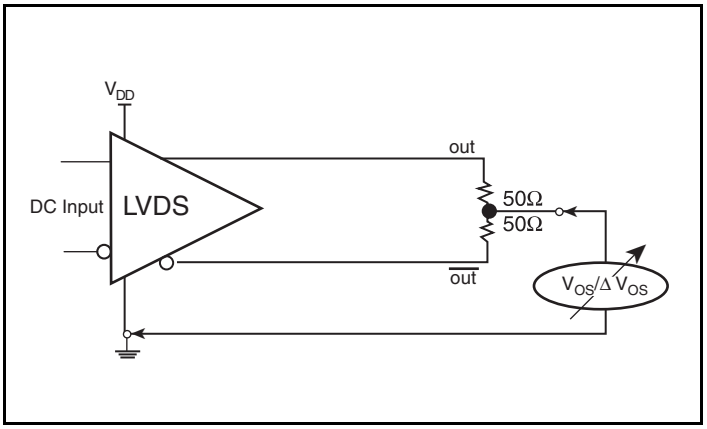


Output Duty Cycle/Pulse Width/Period

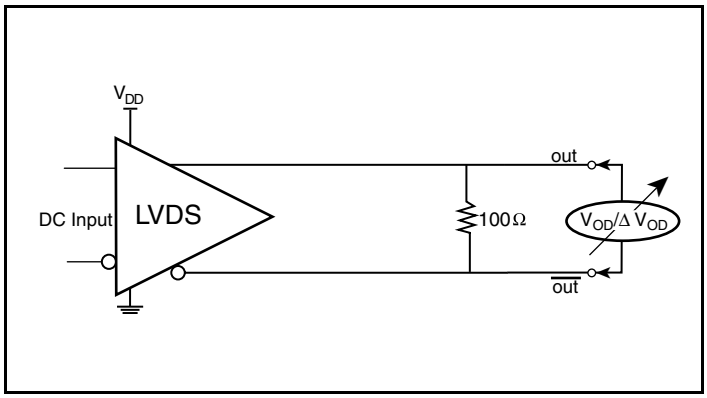
Parameter Measurement Information, continued



RMS Period Jitter



Offset Voltage Setup



Differential Output Voltage Setup

ApplicationS Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS874001I-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

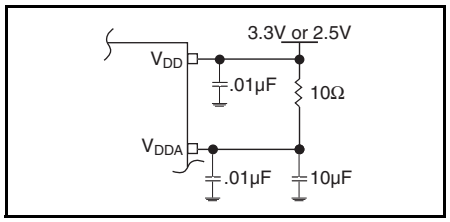


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

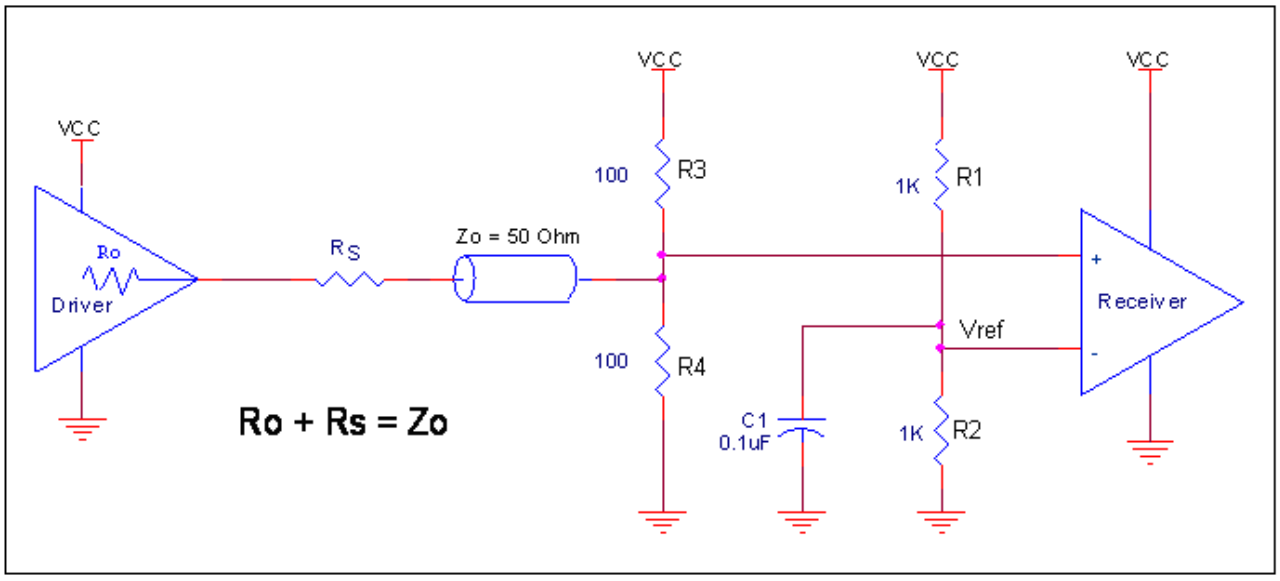
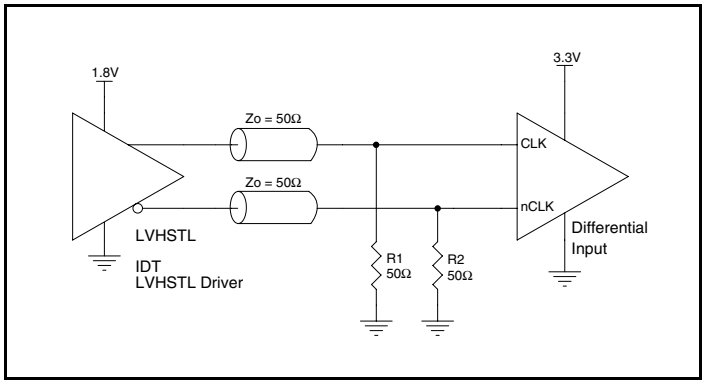


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

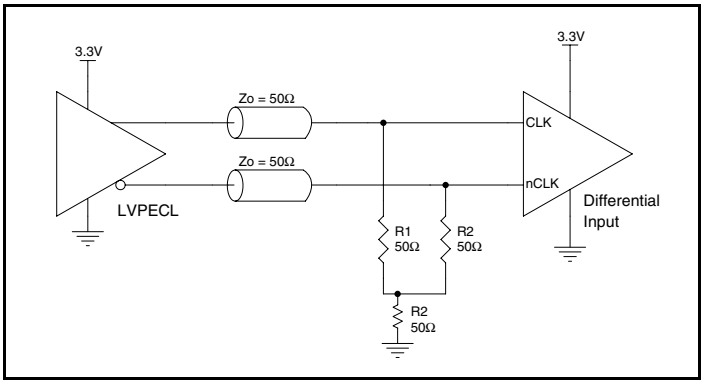


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

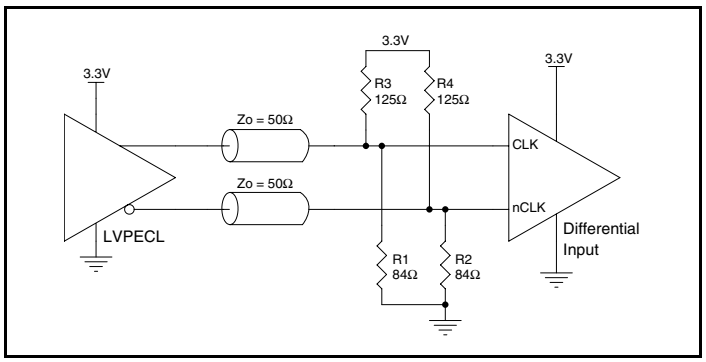


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

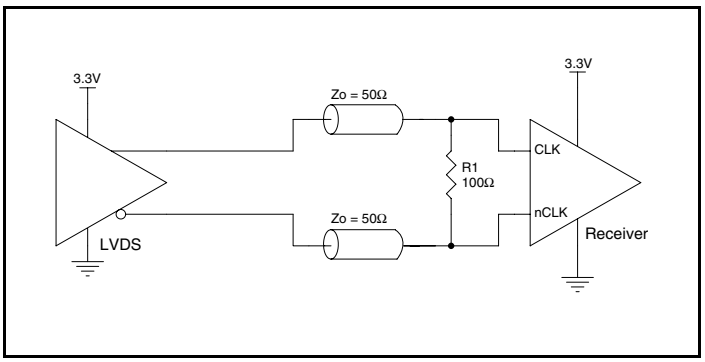


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

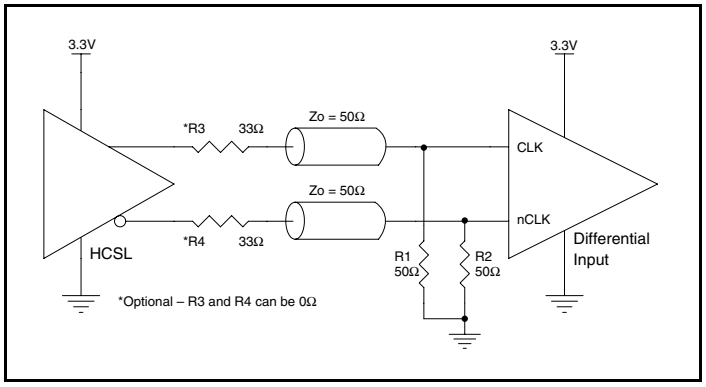


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

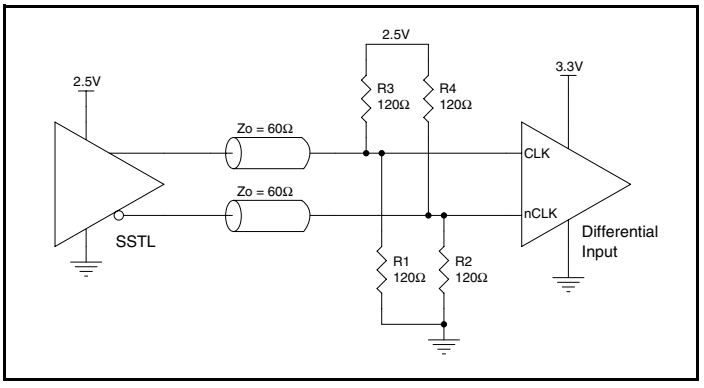


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

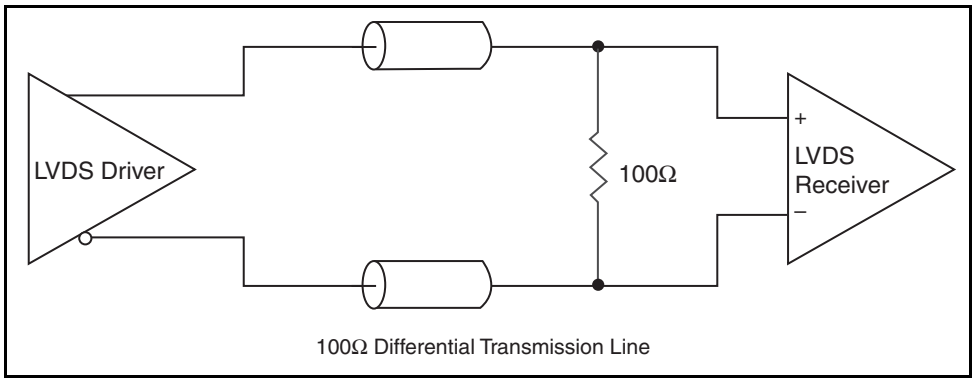


Figure 4. Typical LVDS Driver Termination

Schematic Layout

Figure 5 shows an example of ICS874001I-02 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver.

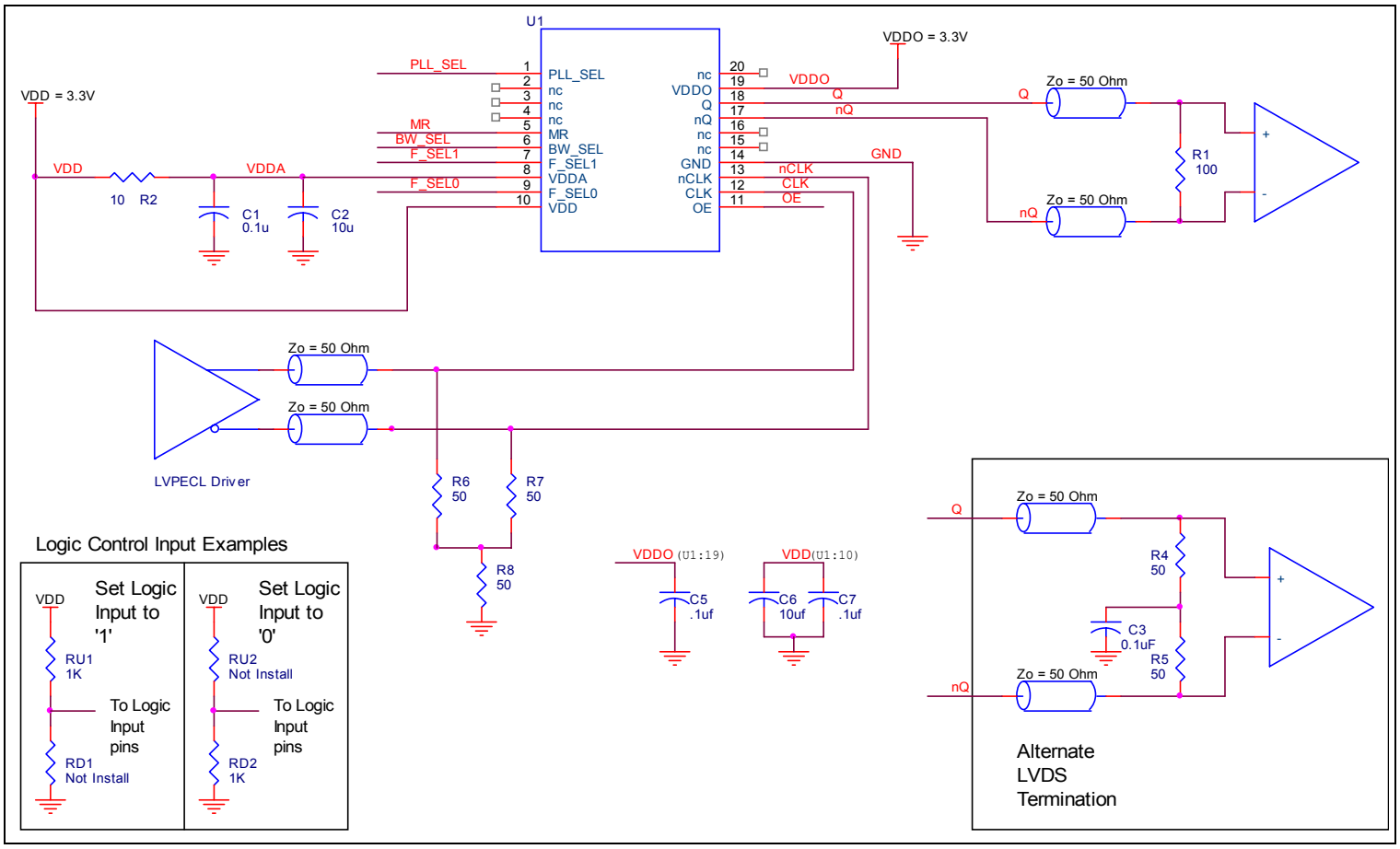


Figure 5. ICS874001I-02 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for theICS874001I-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS874001I-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (72mA + 12mA) = **291.06mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 24mA = **83.16mW**

Total Power$_{\_MAX}$ = 291.06mW + 83.16mW = **374.22mW**

•

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.374W * 86.7°C/W = 117°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

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Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Transistor Count

The transistor count for ICS874001I-02 is: 1,608

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

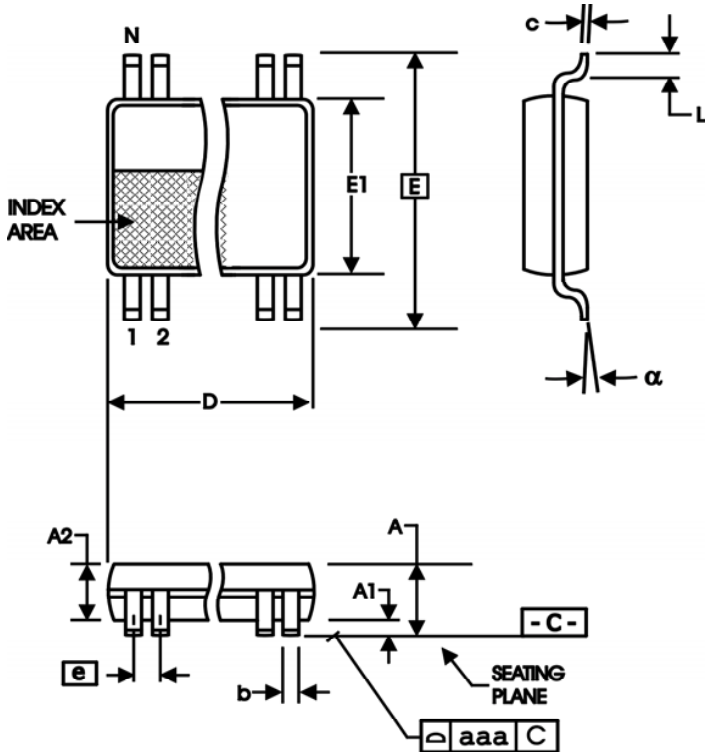

Table 8 Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874001AGI-02LF	ICS4001AI02L	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
874001AGI-02LFT	ICS4001AI02L	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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