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Si52111-B5/B6

PCI-Express Gen 3 Single Output Clock Generator

Features

- PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 common clock compliant
- Gen 3 SRNS Compliant
- Low power HCSL differential output buffer
- Supports Serial-ATA (SATA) at 100 MHz
- No termination resistors required
- 25 MHz Crystal Input or Clock input
- Triangular spread spectrum profile for maximum EMI reduction (Si52111-B6)
- Extended Temperature: –40 to 85 °C
- 3.3 V Power supply
- Small package 10-pin TDFN (3x3 mm)
- Si52111-B5 does not support spread spectrum outputs
- Si52111-B6 supports 0.5% down spread outputs

Ordering Information:
See page 13

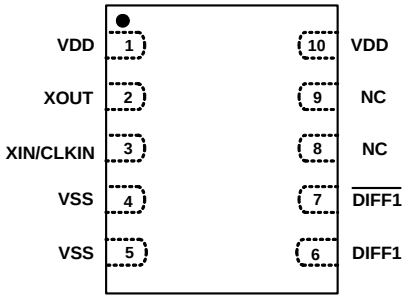
Applications

- Network Attached Storage
- Multi-function Printer
- Wireless Access Point
- Routers

Description

Si52111-B5/B6 is a high-performance, PCIe clock generator that can source one PCIe clock output from a 25 MHz crystal or clock input. The clock output is compliant to PCIe Gen 1, Gen 2, Gen 3, Gen 3 SRNS and Gen 4 common clock specifications. The ultra-small footprint (3x3 mm) and industry leading low power consumption make Si52111-B5/B6 the ideal clock solution for consumer and embedded applications. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

Pin Assignments



Patents pending

Functional Block Diagram

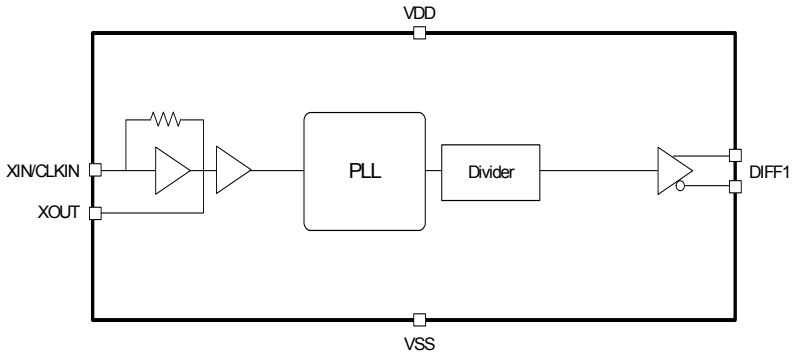


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (extended)	$V_{DD(extended)}$	3.3 V ± 5%	3.13	3.3	3.46	V
Supply Voltage (commercial)	$V_{DD(commercial)}$	3.3 V ± 10%	2.97	3.3	3.63	V

Table 2. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	3.3 V ± 10%	2.97	3.30	3.63	V
Operating Supply Current	I_{DD}	Full Active	—	—	13	mA
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	C_{OUT}	Output Pin Capacitance	—	—	5	pF

Table 3. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal						
Long-term Accuracy	L_{ACC}	Measured at V_{DD}/2 differential	—	—	250	ppm
Clock Input						
CLKIN Duty Cycle	T_{DC}	Measured at V_{DD}/2	45	—	55	%
CLKIN Rise and Fall Times	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	—	4.0	V/ns
CLKIN Cycle-to-Cycle Jitter	T_{CCJ}	Measured at V_{DD}/2	—	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at V_{DD}/2	—	—	350	ps
Input High Voltage	V_{IH}	XIN/CLKIN pin	2	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.8	V
Input High Current	I_{IH}	XIN/CLKIN pin, VIN = V_{DD}	—	—	35	uA
Input Low Current	I_{IL}	XIN/CLKIN pin, 0 < VIN <0.8	–35	—	—	uA
DIFF Clocks						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Skew	T_{SKEW}	Measured at 0 V differential	—	—	60	ps
Output Frequency	F_{OUT}	VDD = 3.3 V	—	100	—	MHz
Frequency Accuracy	F_{ACC}	All output clocks	—	—	100	ppm
Slew Rate	$t_{r/f2}$	Measured differentially from ±150 mV	0.6	—	4.0	V/ns

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-to-Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	28	70	ps
PCIe Gen 1 Pk-Pk Jitter, Common Clock	$Pk\text{-}Pk_{GEN1}$	PCIe Gen 1	—	24	86	ps
PCIe Gen 2 Phase Jitter, Common Clock	RMS_{GEN2}	10 kHz < F < 1.5 MHz	—	1.35	3.0	ps
		1.5 MHz < F < Nyquist	—	1.4	3.1	ps
PCIe Gen 3 Phase Jitter, Common Clock	RMS_{GEN3}	Includes PLL BW 2–4 MHz, CDR = 10 MHz	—	0.4	1.0	ps
PCIe Gen 3 Phase Jitter, Separate Reference No Spread, SRNS	RMS_{GEN3_SRNS}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.28	0.71	ps
PCIe Gen 4 Phase Jitter, Common Clock	RMS_{GEN4}	PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz	—	0.4	1.0	ps
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		–0.3	—	—	V
Spread Range	S_{RNG}	Down Spread, -B6 only	—	–0.5	—	%
Modulation Frequency	F_{MOD}	-B6 only	30	31.5	33	kHz
Enable/Disable and Set-up						
Clock Stabilization from Power-up	T_{STABLE}		—	—	3	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Notes:
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 4. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case (TDFN)	$Ø_{JC}$	JEDEC (JESD 51)	—	—	38.3	°C/W
Dissipation, Junction to Case (TSSOP)	$Ø_{JC}$	JEDEC (JESD 51)	—	—	37.0	°C/W
Dissipation, Junction to Ambient (TDFN)	$Ø_{JA}$	JEDEC (JESD 51)	—	—	90.4	°C/W
Dissipation, Junction to Ambient (TSSOP)	$Ø_{JA}$	JEDEC (JESD 51)	—	—	124.0	°C/W

Table 5. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$		—		4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5		4.6	V_{DC}
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000		—	V
Flammability Rating	UL-94	UL (Class)		V–0		

Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

2. Crystal Recommendations

If using a crystal input, the device requires a parallel resonance crystal.

Table 6. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	ESR	Drive	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	12–15 pF	<50 Ω	>150 µW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

2.1. Crystal Loading

Crystal loading is critical in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using two trim capacitors. It is important that the trim capacitors are in series with the crystal.

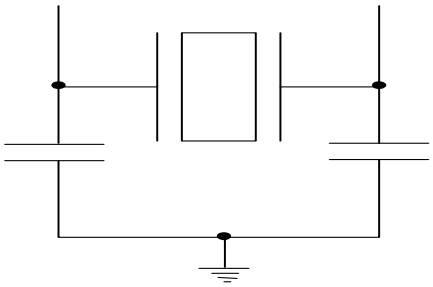


Figure 1. Crystal Capacitive Clarification

2.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both sides is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

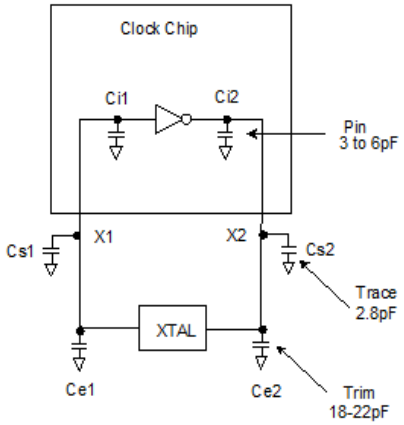


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci: Internal capacitance (lead frame, bond wires, etc.)

3. Test and Measurement Setup

Figures 3 through 5 show the test load configuration for the differential clock signals.

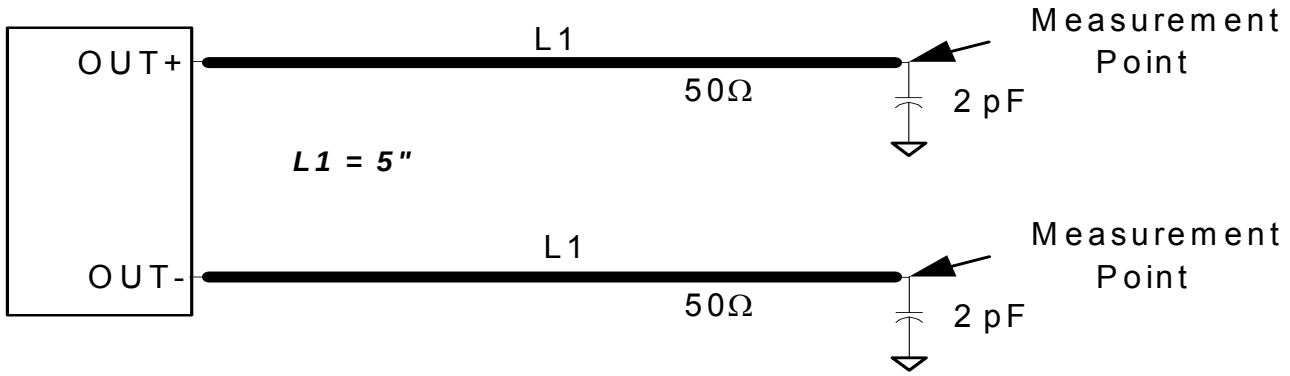


Figure 3. 0.7 V Differential Load Configuration

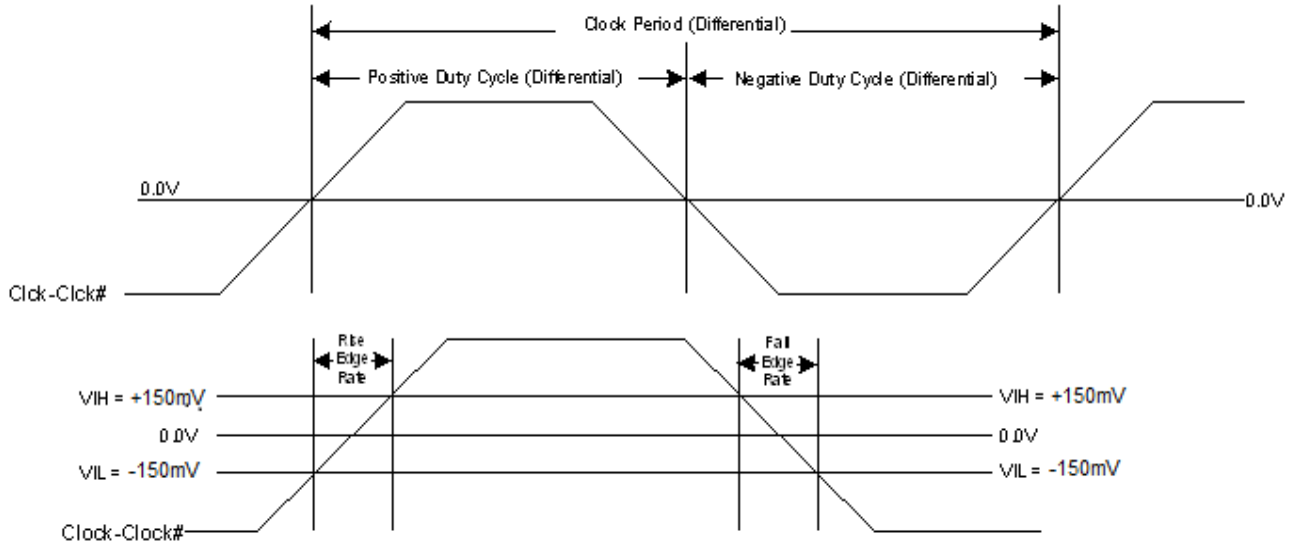


Figure 4. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

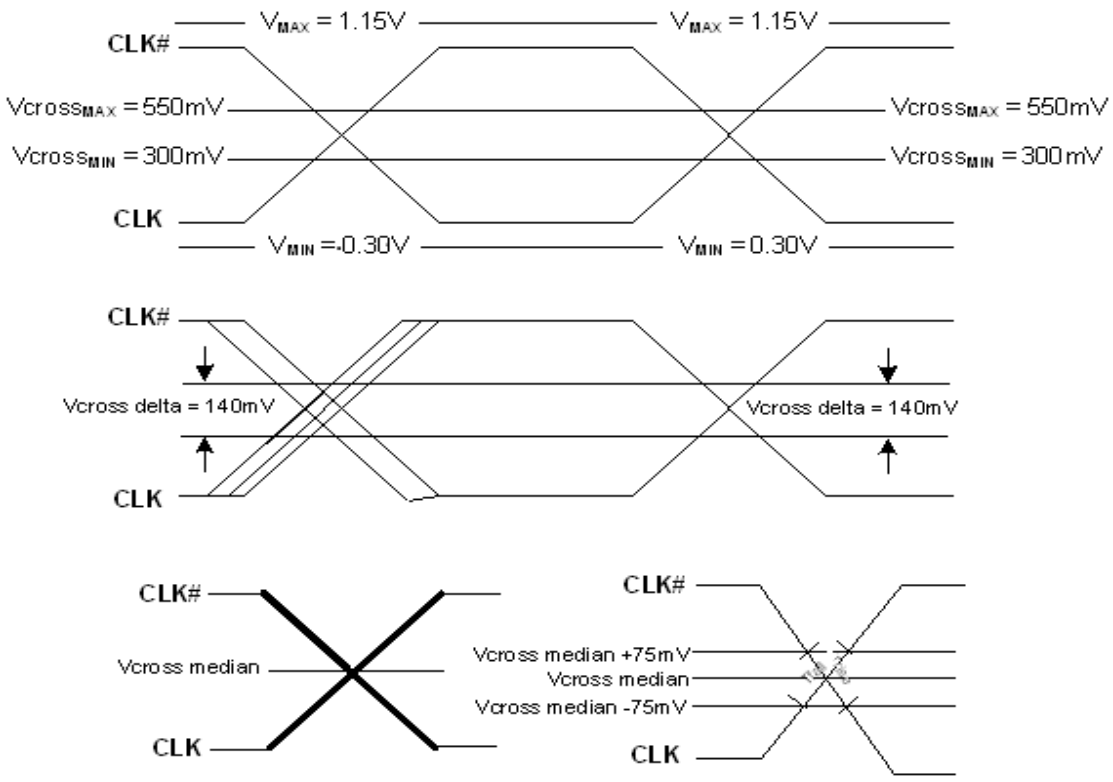


Figure 5. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Pin Descriptions

4.1. 10-Pin TDFN

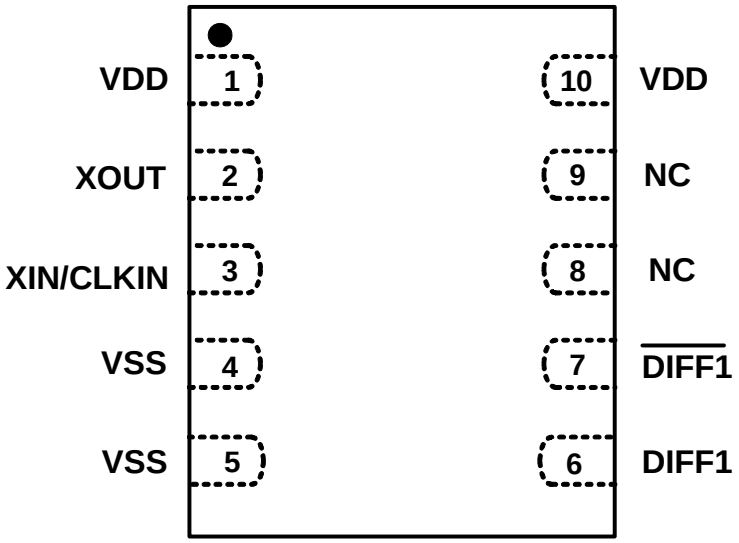


Figure 6. 10-Pin TDFN

Table 7. 10-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V Power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	VSS	GND	Ground.
6	DIFF1	O, DIF	0.7 V, 100 MHz differentials clock output.
7	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differentials clock output.
8	NC	NC	No Connect. Do not connect this pin to anything.
9	NC	NC	No Connect. Do not connect this pin to anything.
10	VDD	PWR	3.3 V Power supply

4.2. 8-Pin TSSOP

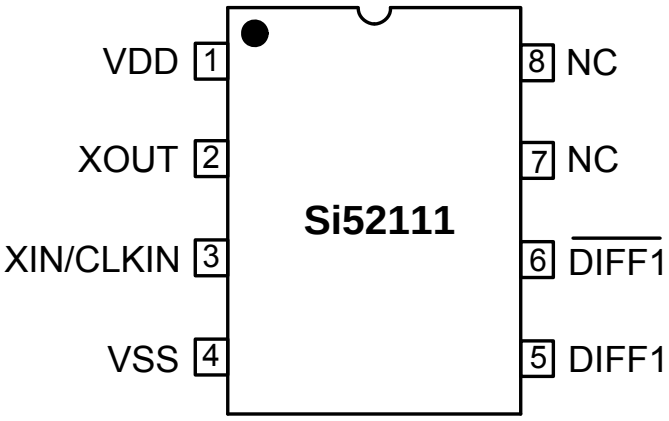


Figure 7. 8-Pin TSSOP

Table 8. 8-Pin TSSOP Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V Power supply.
2	XOUT	O	25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input).
3	XIN/CLKIN	I	25.00 MHz crystal input or 3.3 V, 25 MHz clock Input.
4	VSS	GND	Ground.
5	DIFF1	O, DIF	0.7 V, 100 MHz differentials clock.
6	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differentials clock.
7	NC		No Connect. Do not connect this pin to anything.
8	NC		No Connect. Do not connect this pin to anything.

5. Ordering Guide

Part Number	Spread Option	Package Type	Temperature
Si52111-B5-GM2	No Spread	10-pin TDFN	Extended, –40 to 85 °C
Si52111-B5-GM2R	No Spread	10-pin TDFN—Tape and Reel	Extended, –40 to 85 °C
Si52111-B5-GT	No Spread	8-pin TSSOP	Extended, –40 to 85 °C
Si52111-B5-GTR	No Spread	8-pin TSSOP - Tape and Reel	Extended, –40 to 85 °C
Si52111-B6-GM2	–0.5% Spread	10-pin TDFN	Extended, –40 to 85 °C
Si52111-B6-GM2R	–0.5% Spread	10-pin TDFN—Tape and Reel	Extended, –40 to 85 °C
Si52111-B6-GT	–0.5% Spread	8-pin TSSOP	Extended, –40 to 85 °C
Si52111-B6-GTR	–0.5% Spread	8-pin TSSOP - Tape and Reel	Extended, –40 to 85 °C

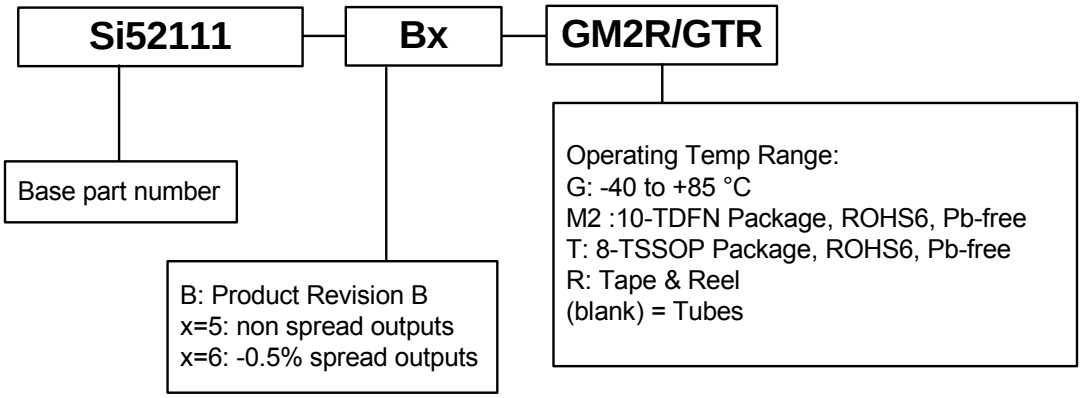


Figure 8. Ordering Information

6. Package Outlines

6.1. TDFN Package

Figure 9 illustrates the package details for the 10-pin TDFN. Table 9 lists the values for the dimensions shown in the illustration.

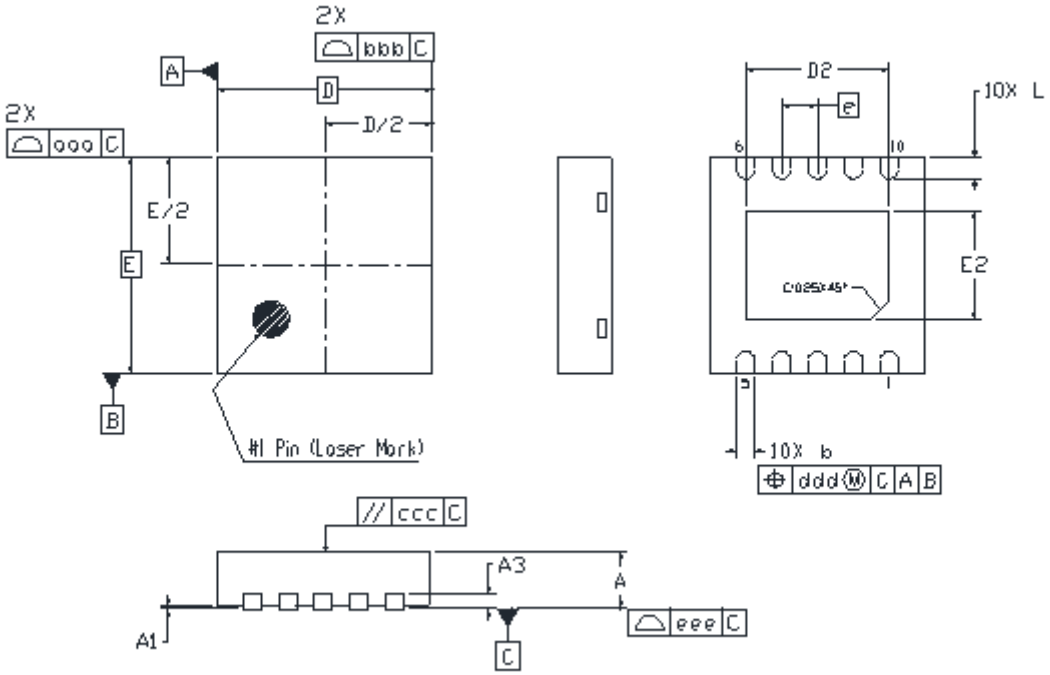


Figure 9. 10-Pin TDFN Package Drawing

Table 9. TDFN Package Diagram Dimensions

Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		3.00 BSC.	
D2	1.90	2.00	2.10
e		0.50 BSC	
E		3.00 BSC	
E2	1.40	1.50	1.60
L	0.25	0.30	0.35
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.10	
eee		0.08	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
4. This drawing conforms to the JEDEC Solid State Outline MO-229.

6.2. TSSOP Package

Figure 10 illustrates the package details for the 8-pin TSSOP. Table 10 lists the values for the dimensions shown in the illustration.

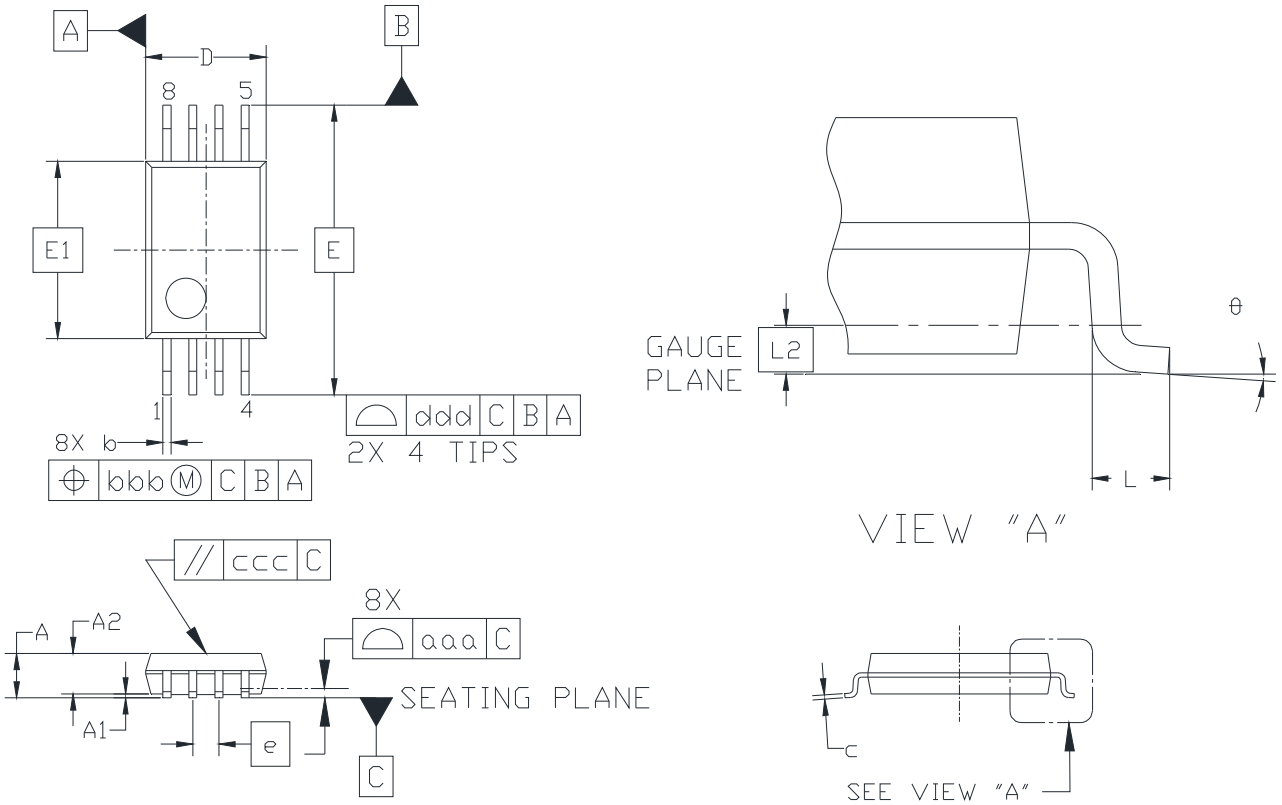


Figure 10. 8-Pin TSSOP Package Drawing

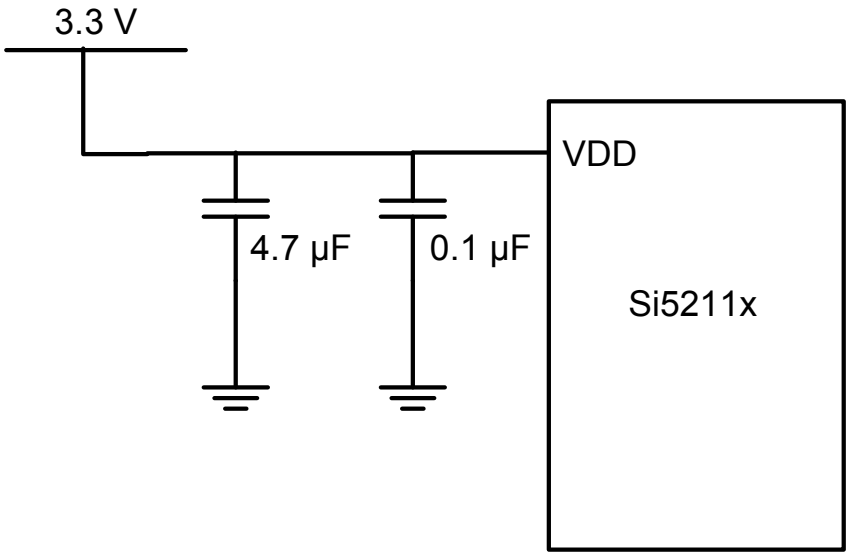
Table 10. TSSOP Package Diagram Dimensions

Symbol	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Recommended Design Guideline



Note: FB Specifications:
DC resistance 0.1–0.3 Ω
Impedance at 100 MHz ≥ 1000 Ω

Figure 11. Recommended Application Schematic

Document Change List

Revision 1.0 to Revision 1.1

- Added “4.2. 8-Pin TSSOP” pin description on page 12.

Revision 1.1 to Revision 1.2

- Updated Features on page 1.
- Updated Description on page 1.
- Updated Table 3, “AC Electrical Specifications,” on page 4.

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