阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

CPRI and 10G Ethernet Data Recovery IC with Amp/EQ from 614.4 Mbps to 10.3125 Gbps

Data Sheet

ADN2905

FEATURES

Serial CPRI data rates
- **614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps, 3.072 Gbps, 4.9152 Gbps, 6.144 Gbps, and 9.8304 Gbps**

Ethernet data rates: 1.25 Gbps and 10.3125 Gbps
No reference clock required
Jitter performance superior to the SFF-8431 jitter specifications
Optional equalizer or 0 dB EQ input mode
Quantizer sensitivity: 200 mV p-p typical (equalizer mode)
Sample phase adjust (5.65 Gbps or greater)
Output polarity invert
I²C to access optional features
Loss of lock (LOL) indicator
PRBS generator/detector
Application aware power
- **349.5 mW at 9.8304 Gbps, 0 dB EQ input mode**
- **287.7 mW at 6.144 Gbps, 0 dB EQ input mode**
- **249.3 mW at 3.072 Gbps, 0 dB EQ input mode**

Power supply: 1.2 V, flexible 1.8 V to 3.3 V, and 3.3 V
4 mm × 4 mm, 24-lead LFCSP

APPLICATIONS

SFF-8431-compatible
Ethernet: 10GE, 1GE, and CPRI: OS/L.6 up to OS/L.96

GENERAL DESCRIPTION

The ADN2905 provides the receiver functions of quantization and multirate data recovery at 614.4 Mbps, 1.2288 Gbps, 1.25 Gbps, 2.4576 Gbps, 3.072 Gbps, 4.9152 Gbps, 6.144 Gbps, 9.8304 Gbps, and 10.3125 Gbps, used in Common Public Radio Interface (CPRI) and gigabit Ethernet applications. The ADN2905 automatically locks to all the specified CPRI and Ethernet data rates without the need for an external reference clock or programming. The ADN2905 jitter performance exceeds the jitter requirement specified by SFF-8431.

The ADN2905 provides manual sample phase adjustment. Additionally, the user can select an equalizer or a 0 dB EQ as the input. The equalizer is either adaptive or can be manually set.

The ADN2905 also supports pseudorandom binary sequence (PRBS) generation, bit error detection, and input data rate readback features.

The ADN2905 is available in a compact 4 mm × 4 mm, 24-lead chip scale package (LFCSP). All ADN2905 specifications are defined over the ambient temperature range of −40°C to +85°C, unless otherwise noted.

FUNCTIONAL BLOCK DIAGRAM

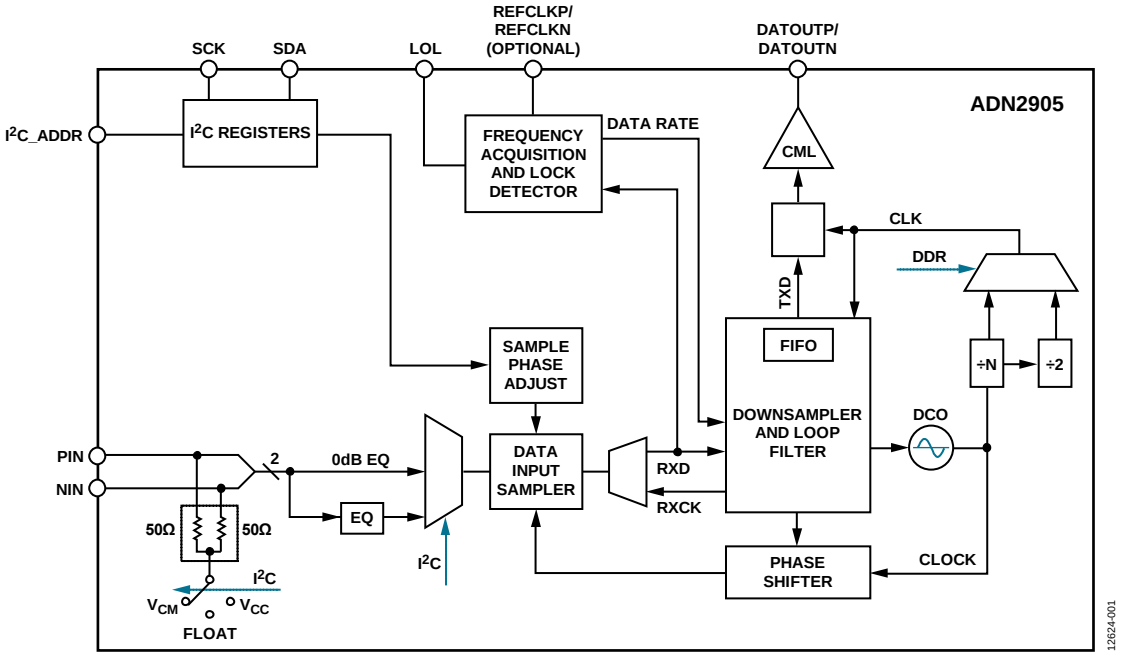


Figure 1.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADN2905* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADN2905/ADN2913/ADN2915/ADN2917 Evaluation Board

DOCUMENTATION

Data Sheet

- ADN2905: CPRI and 10G Ethernet Data Recovery IC with Amp/EQ from 614.4 Mbps to 10.3125 Gbps Data Sheet

User Guides

- UG-877: ADN2905/ADN2913/ADN2915/ADN2917 Evaluation Board Setup and Applications

DESIGN RESOURCES

- ADN2905 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADN2905 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

1/16—Rev 0. to Rev. A

Changes to Figure 5 ... 8
Updated Outline Dimensions ... 27
Changes to Ordering Guide ... 27

12/14—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = VCC_{MIN} to VCC_{MAX}, VCC1 = $VCC1_{MIN}$ to $VCC1_{MAX}$, VDD = VDD_{MIN} to VDD_{MAX}, VEE = 0 V, input data pattern = PRBS $2^{23} - 1$, ac-coupled (to 100 Ω differential termination load), I^2C register default settings, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MULTIRATE SUPPORT RANGE		0.6144		10.3125	Gbps
INPUT—DC CHARACTERISTICS					
Peak-to-Peak Differential Input	PIN – NIN, see Figure 29			1.0	V
Input Resistance	Differential	95	100	105	Ω
0 dB EQ INPUT—CML COMPLIANT					
Input Voltage Range	At PIN or NIN, dc-coupled, RX_TERM_FLOAT = 1 (floated)	0.5		VCC	V
Input Common-Mode Level	DC-coupled (see Figure 28), 600 mV p-p differential, RX_TERM_FLOAT = 1 (floated)	0.65		VCC − 0.15	V
Differential Input Sensitivity					
CPRI × 16, 9.8304 Gbps	AC-coupled, RX_TERM_FLOAT = 0 (V_{CM} = 1.2 V), bit error rate (BER) = 1×10^{-12}		250		mV p-p
EQUALIZER INPUT PATH					
Differential Input Sensitivity	15 inch FR-4, 100 Ω differential transmission line, adaptive EQ on				
CPRI × 16, 9.8304 Gbps	BER = 1×10^{-12}		200		mV p-p
INPUT—AC CHARACTERISTICS					
S11	At 7.5 GHz, differential return loss, see Figure 8		−12		dB
LOSS OF LOCK (LOL) DETECT					
Digital Control Oscillator (DCO) Frequency Error for LOL Assert	With respect to nominal, data collected in lock to reference (LTR) mode		1000		ppm
DCO Frequency Error for LOL Deassert	With respect to nominal, data collected in LTR mode		250		ppm
LOL Assert Response Time	2.4576 Gbps		51		µs
	9.8304 Gbps		18		µs
ACQUISITION TIME					
Lock to Data (LTD) Mode	2.4576 Gbps		0.5		ms
	9.8304 Gbps		0.5		ms
Optional LTR Mode[1]			6.0		ms
DATA RATE READBACK ACCURACY					
Coarse Readback			±5		%
Fine Readback	In addition to reference clock accuracy		±100		ppm
POWER SUPPLY VOLTAGE					
VCC		1.14	1.2	1.26	V
VDD		2.97	3.3	3.63	V
VCC1		1.62	1.8	3.63	V
POWER SUPPLY CURRENT	0 dB EQ input mode, clock output disabled				
VCC	2.4576 Gbps		182.0		mA
	3.072 Gbps		159.1		mA
	4.9152 Gbps		180.8		mA
	6.144 Gbps		190.5		mA
	9.8304 Gbps		217.3		mA
VDD	2.4576 Gbps		8.6		mA
	3.072 Gbps		9.0		mA
	4.9152 Gbps		8.8		mA
	6.144 Gbps		8.9		mA
	9.8304 Gbps		9.1		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCC1	2.4576 Gbps		31.7		mA
	3.072 Gbps		16.2		mA
	4.9152 Gbps		31.8		mA
	6.144 Gbps		16.1		mA
	9.8304 Gbps		32.8		mA
TOTAL POWER DISSIPATION	0 dB EQ input mode, clock output disabled				
	2.4576 Gbps		305.7		mW
	3.072 Gbps		249.3		mW
	4.9152 Gbps		304.5		mW
	6.144 Gbps		287.7		mW
	9.8304 Gbps		349.5		mW
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] This typical acquisition specification applies to all selectable reference clock frequencies in the range of 11.05 MHz to 176.8 MHz.

JITTER SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = VCC_{MIN} to VCC_{MAX}, VCC1 = $VCC1_{MIN}$ to $VCC1_{MAX}$, VDD = VDD_{MIN} to VDD_{MAX}, VEE = 0 V, input data pattern = PRBS $2^{23} - 1$, ac-coupled to 100 Ω differential termination load, I^2C register default settings, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TRANSMITTER JITTERS						
Deterministic Jitter	T_DJ	CPRI = 9.8304 Gbps, K28.5 + D5.6 and K28.5 + D16.2		6.98		ps
Random Jitter	T_RJ	CPRI = 9.8304 Gbps, K28.5 + D5.6 and K28.5 + D16.2		0.36		ps
Duty Cycle Distortion	T_DCD	CPRI = 9.8304 Gbps, K28.5 + D5.6 and K28.5 + D16.2		0.57		ps
Total Jitter	TJ	SFF-8431, 64B/66B, 10.3125 Gbps		13.6		ps
Data Dependent Jitter	DDJ	SFF-8431, PRBS $2^9 - 1$, 10.3125 Gbps		7.37		ps
Data Dependent Pulse Width Shrinkage	DDPWS	SFF-8431, PRBS $2^9 - 1$, 10.3125 Gbps		4.58		ps
Uncorrelated Jitter	UJ	SFF-8431, 64B/66B, 10.3125 Gbps		0.14		ps
RECEIVER JITTERS						
Total Jitter Tolerance	TJT	SFF-8431, 10.3125 Gbps		82.4		ps
99% Jitter	J2	SFF-8431, 10.3125 Gbps		55.5		ps
Data Dependent Pulse Width Shrinkage	DDPWS	SFF-8431, 10.3125 Gbps		33.7		ps

OUTPUT AND TIMING SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = VCC_{MIN} to VCC_{MAX}, VCC1 = $VCC1_{MIN}$ to $VCC1_{MAX}$, VDD = VDD_{MIN} to VDD_{MAX}, VEE = 0 V, input data pattern = PRBS $2^{23} - 1$, ac-coupled to 100 Ω differential termination load, I^2C register default settings, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CML OUTPUT CHARACTERISTICS						
Data Differential Output Swing		9.8304 Gbps, DATA_SWING[3:0] = 0xC (default)	535	600	672	mV p-p
		9.8304 Gbps, DATA_SWING[3:0] = 0xF (maximum)	668	724	771	mV p-p
		9.8304 Gbps, DATA_SWING[3:0] = 0x4 (minimum)	189	219	252	mV p-p
Output Voltage						
High	V_{OH}	DC-coupled	VCC – 0.05	VCC – 0.025	VCC	V
Low	V_{OL}	DC-coupled	VCC – 0.36	VCC – 0.325	VCC – 0.29	V
CML OUTPUT TIMING CHARACTERISTICS						
Rise Time		20% to 80%, at 9.8304 Gbps, DATOUTN/DATOUTP	17.4	32.6	46.5	ps
		20% to 80%, at 9.8304 Gbps, CLKOUTN/CLKOUTP	22.2	28.3	33.1	ps
Fall Time		80% to 20%, at 9.8304 Gbps, DATOUTN/DATOUTP	17.5	33	49.1	ps
		80% to 20%, at 9.8304 Gbps, CLKOUTN/CLKOUTP	23.9	29.2	33.7	ps
Setup Time, Full Rate Clock	t_S	See Figure 2		0.5		UI
Hold Time, Full Rate Clock	t_H	See Figure 2		0.5		UI
Setup Time, DDR Mode	t_S	See Figure 3		0.5		UI
Hold Time, DDR Mode	t_H	See Figure 3		0.5		UI
I^2C INTERFACE DC CHARACTERISTICS		LVTTL				
Input Voltage						
High	V_{IH}		2.0			V
Low	V_{IL}				0.8	V
Input Current		$V_{IN} = 0.1 \times VDD$ or $V_{IN} = 0.9 \times VDD$	−10.0		+10.0	µA
Output Low Voltage	V_{OL}	$I_{OL} = 3.0$ mA			0.4	V
I^2C INTERFACE TIMING		See Figure 14				
SCK Clock Frequency					400	kHz
SCK Pulse Width High	t_{HIGH}		600			ns
SCK Pulse Width Low	t_{LOW}		1300			ns
Start Condition Hold Time	$t_{HD;STA}$		600			ns
Start Condition Setup Time	$t_{SU;STA}$		600			ns
Data Setup Time	$t_{SU;DAT}$		100			ns
Data Hold Time	$t_{HD;DAT}$		300			ns
SCK/SDA Rise/Fall Time[1]	t_R/t_F		$20 + 0.1C_b$		300	ns
Stop Condition Setup Time	$t_{SU;STO}$		600			ns
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1300			ns
LVTTL DC INPUT CHARACTERISITICS (I^2C_ADDR)						
Input Voltage						
High	V_{IH}		2.0			V
Low	V_{IL}				0.8	V
Input Current						
High	I_{IH}	$V_{IN} = 2.4$ V			5	µA
Low	I_{IL}	$V_{IN} = 0.4$ V	−5			µA
LVTTL DC OUTPUT CHARACTERISITICS (LOS/LOL)						
Output Voltage						
High	V_{OH}	$I_{OH} = 2.0$ mA	2.4			V
Low	V_{OL}	$I_{OL} = -2.0$ mA			0.4	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE CLOCK CHARACTERISTICS		Optional LTR mode				
Input Compliance Voltage (Single-Ended)	V_{CM}	No input offset, no input current, see Figure 21, ac-coupled input	0.55		1.0	V
Minimum Differential Input Drive		See Figure 21, ac-coupled, differential input		100		mV p-p
Reference Frequency			11.05		176.8	MHz
Required Accuracy[2]		AC-coupled, differential input		100		ppm

[1] C_b is the total capacitance of one bus line in picofarads (pF). If mixed with high speed (HS) mode devices, faster rise/fall times are allowed (refer to the Philips *I²C Bus Specification*, Version 2.1).
[2] Required accuracy in dc-coupled mode is guaranteed by design as long as the clock common-mode voltage output matches the reference clock common-mode voltage range.

TIMING DIAGRAMS

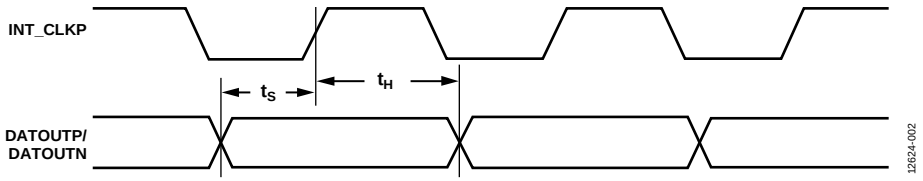


Figure 2. Data to Clock Timing (Full Rate Clock Mode)

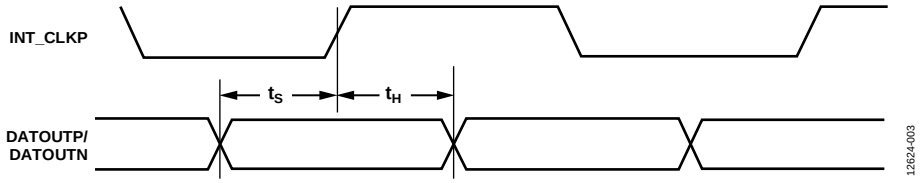


Figure 3. Data to Clock Timing (Half-Rate Clock/DDR Mode)

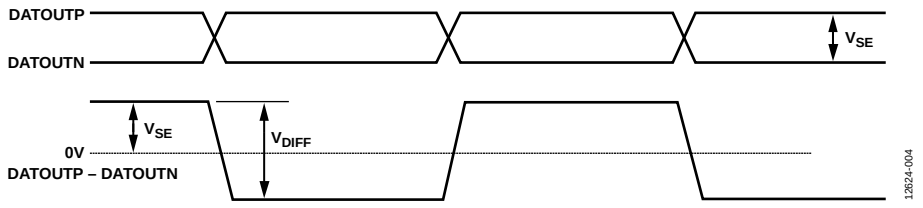


Figure 4. Single-Ended vs. Differential Output Amplitude Relationship

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage (VCC = 1.2 V)	1.26 V
Supply Voltage (VDD and VCC1 = 3.3 V)	3.63 V
Maximum Input Voltage (REFCLKP/REFCLKN, NIN/PIN)	1.26 V
Minimum Input Voltage (REFCLKP/REFCLKN, NIN/PIN)	VEE− 0.4 V
Maximum Input Voltage (SDA, SCK, I^2C_ADDR)	3.63 V
Minimum Input Voltage (SDA, SCK, I^2C_ADDR)	VEE − 0.4 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

Thermal resistance is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages, for a 4-layer board with the exposed paddle soldered to VEE.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JB}[2]	θ_{JC}[3]	Unit
24-Lead LFCSP	45	5	11	°C/W

[1] Junction to ambient.
[2] Junction to base.
[3] Junction to case.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

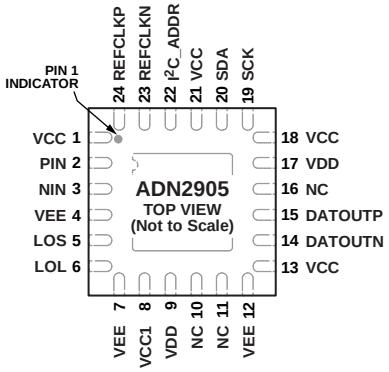


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	VCC	P	1.2 V Supply for Limiting Amplifier.
2	PIN	AI	Positive Differential Data Input (CML).
3	NIN	AI	Negative Differential Data Input (CML).
4	VEE	P	Ground for Limiting Amplifier.
5	LOS	DO	Loss of Signal Output (Active High).
6	LOL	DO	Loss of Lock Output (Active High).
7	VEE	P	Digital Control Oscillator (DCO) Ground.
8	VCC1	P	1.8 V to 3.3 V DCO Supply.
9	VDD	P	3.3 V High Supply.
10	NC	N/A	No Connect. Do not connect to this pin. Leave this pin floating
11	NC	N/A	No Connect. Do not connect to this pin. Leave this pin floating
12	VEE	P	Ground for CML Output Drivers.
13	VCC	P	1.2 V Supply for CML Output Drivers.
14	DATOUTN	DO	Negative Differential Retimed Data Output (CML).
15	DATOUTP	DO	Positive Differential Retimed Data Output (CML).
16	NC	DI	No Connect. Tie this pin to VEE (ground).
17	VDD	P	3.3 V High Supply.
18	VCC	P	1.2 V Core Digital Supply.
19	SCK	DI	Clock for I^2C.
20	SDA	DIO	Bidirectional Data for I^2C.
21	VCC	P	1.2 V Core Supply.
22	I^2C_ADDR	DI	I^2C Address Setting. Sets the device I^2C address to 0x80 when I^2C_ADDR = 0. Sets the device I^2C address to 0x82 when I^2C_ADDR = 1.
23	REFCLKN	DI	Negative Reference Clock Input (Optional).
24	REFCLKP	DI	Positive Reference Clock Input (Optional).
N/A	EPAD	P	Exposed Pad (VEE). The exposed pad on the bottom of the device package must be connected to VEE electrically. The exposed pad works as a heat sink.

[1] P is power, AI is analog input, DI is digital input, DO is digital output, DIO is digital input/output, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, VCC = 1.2 V, VCC1 = 1.8 V, VDD = 3.3 V, VEE = 0 V, input data pattern = PRBS $2^{15} - 1$, ac-coupled inputs and outputs, unless otherwise noted.

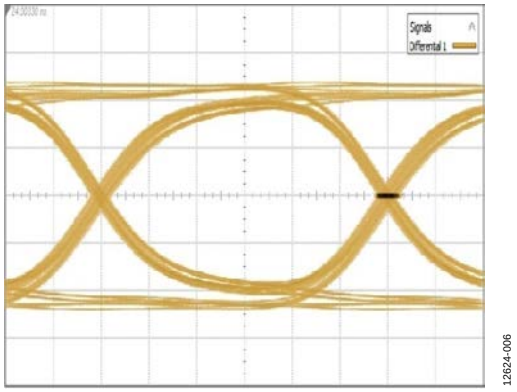


Figure 6. Output Eye Diagram at CPRI × 16 = 9.8304 Gbps, Time = 16.95 ps/div, Amplitude = 116 mV/div

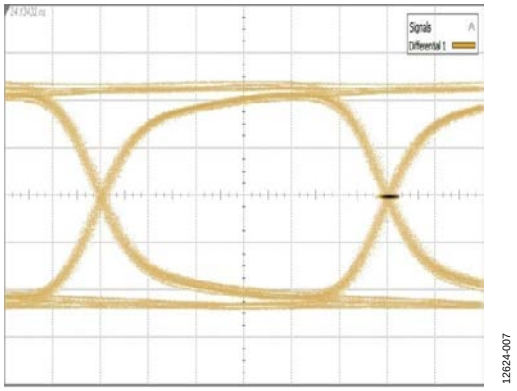


Figure 7. Output Eye Diagram at CPRI × 12 = 6.144 Gbps, Time = 27.13 ps/div, Amplitude = 118 mV/div

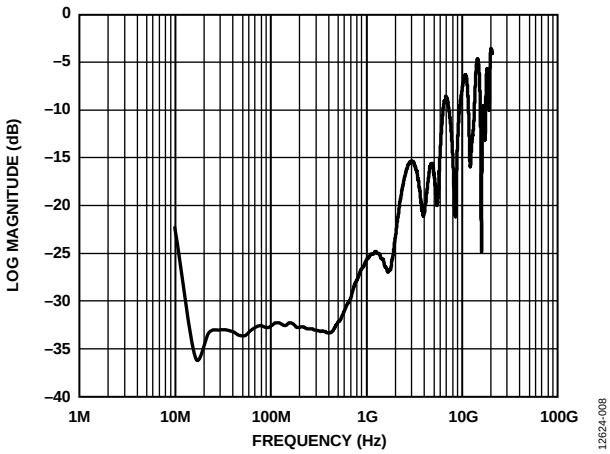


Figure 8. Typical S11 Spectrum Performance

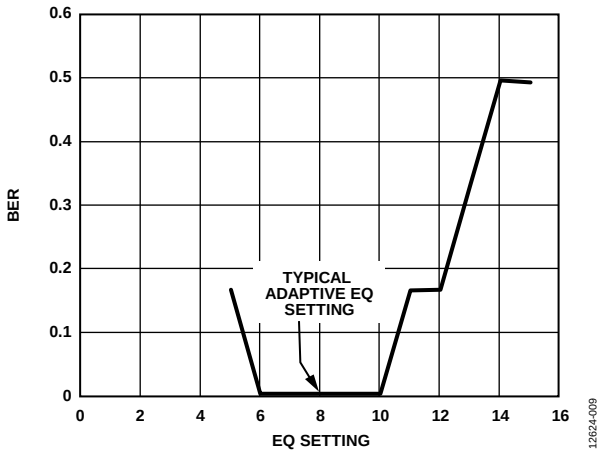


Figure 9. BER in Equalizer Mode vs. EQ Compensation at CPRI × 16 = 9.8304 Gbps (with a Signal of 400 mV p-p Differential, on 15 inch FR4 Traces, with Variant EQ Compensation, Including Adaptive EQ)

I²C INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTIONS

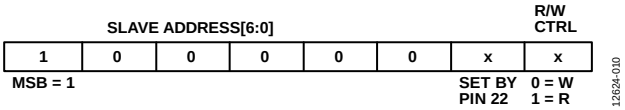


Figure 10. Slave Address Configuration

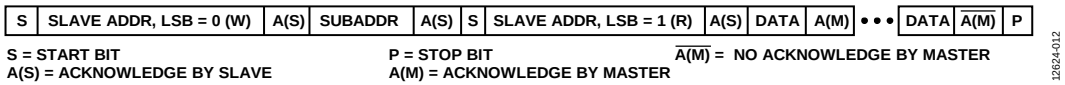


Figure 11. I²C Read Data Transfer

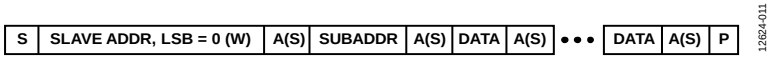


Figure 12. I²C Write Data Transfer

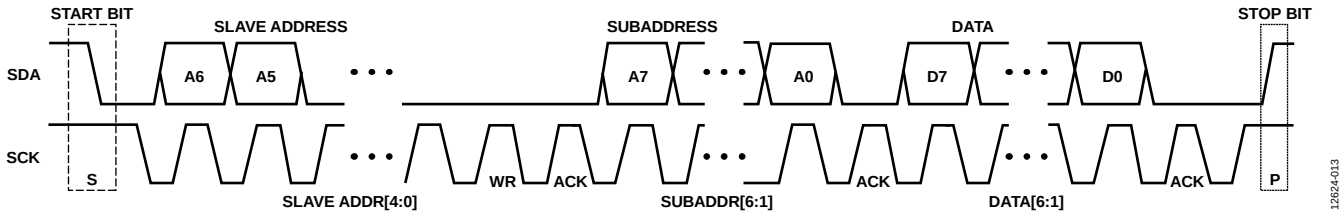


Figure 13. I²C Data Transfer Timing

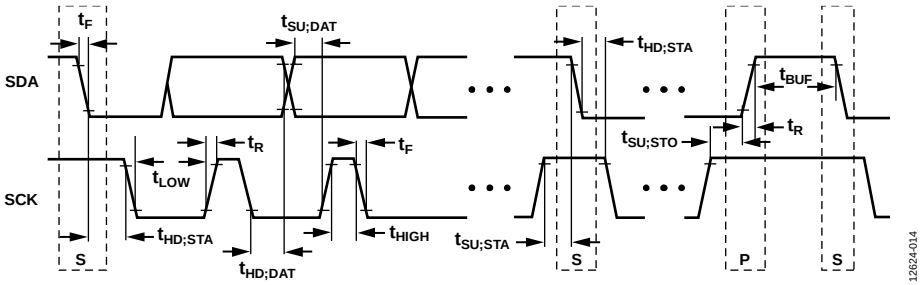


Figure 14. I²C Interface Timing Diagram

REGISTER MAP

Writing to register bits other than those clearly labeled is not recommended and may cause unintended results.

Table 7. Internal Register Map[1, 2]

Reg. Name	R/W	Addr. (Hex)	Default (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
Readback/Status											
FREQMEAS0	R	0x0	N/A	FREQ0[7:0] (RATE_FREQ[7:0])							
FREQMEAS1	R	0x1	N/A	FREQ1[7:0] (RATE_FREQ[15:8])							
FREQMEAS2	R	0x2	N/A	FREQ2[7:0] (RATE_FREQ[23:16])							
FREQ_RB1	R	0x4	N/A	VCOSEL[7:0]							
FREQ_RB2	R	0x5	N/A	X	FULLRATE	DIVRATE[3:0]				VCOSEL[9:8]	
STATUSA	R	0x6	N/A	X	X	Reserved	LOL status	Reserved	Static LOL	X	RATE_MEAS_COMP
General Control											
CTRLA	R/W	0x8	0x10	0	CDR_MODE[2:0]			0	Reset static LOL	RATE_MEAS_EN	RATE_MEAS_RESET
CTRLB	R/W	0x9	0x08	SOFTWARE_RESET	INIT_FREQ_ACQ	CDR bypass	LOL config	1	Reserved	0	0
CTRLC	R/W	0xA	0x05	0	0	0	0	0	REFCLK_PDN	0	1
FLL Control											
LTR_MODE	R/W	0xF	0x00	0	LOL data	FREF_RANGE[1:0]		DATA_TO_REF_RATIO[3:0]			
DPLL Control											
DPLLA	R/W	0x10	0x1C	0	0	0	EDGE_SEL[1:0]		TRANBW[2:0]		
DPLLD	R/W	0x13	0x02	0	0	0	0	0	Reserved to 0	DLL_SLEW[1:0]	
Phase	R/W	0x14	0x00	0	0	0	0	SAMPLE_PHASE[3:0]			
LA_EQ	R/W	0x16	0x08	RX_TERM_FLOAT	INPUT_SEL[1:0]		ADAPTIVE_EQ_EN	EQ_BOOST[3:0]			
Output Control											
OUTPUTA	R/W	0x1E	0x00	0	0	Data squelch	DATOUT_DISABLE	1	DDR_DISABLE	DATA_POLARITY	Reserved
OUTPUTB	R/W	0x1F	0xCC	DATA_SWING[3:0]				Reserved			
PRBS Control											
PRBS Gen 1	R/W	0x39	0x00	0	0	DATA_CID_BIT	DATA_CID_EN	0	DATA_GEN_EN	DATA_GEN_MODE[1:0]	
PRBS Gen 2	R/W	0x3A	0x00	DATA_CID_LENGTH[7:0]							
PRBS Gen 3	R/W	0x3B	0x00	PROG_DATA[7:0]							
PRBS Gen 4	R/W	0x3C	0x00	PROG_DATA[15:8]							
PRBS Gen 5	R/W	0x3D	0x00	PROG_DATA[23:16]							
PRBS Gen 6	R/W	0x3E	0x00	PROG_DATA[31:24]							
PRBS Rec 1	R/W	0x3F	0x00	0	0	0	0	DATA_RECEIVER_CLEAR	DATA_RECEIVER_ENABLE	DATA_RECEIVER_MODE[1:0]	
PRBS Rec 2	R	0x40	0x00	PRBS_ERROR_COUNT[7:0]							
PRBS Rec 3	R	0x41	0x00								PRBS_ERROR
PRBS Rec 4	R	0x42	N/A	DATA_LOADED[7:0]							
PRBS Rec 5	R	0x43	N/A	DATA_LOADED[15:8]							
PRBS Rec 6	R	0x44	N/A	DATA_LOADED[23:16]							
PRBS Rec 7	R	0x45	N/A	DATA_LOADED[31:24]							

Reg. Name	R/W	Addr. (Hex)	Default (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
ID/Revision											
REV	R	0x48	0x54	Rev[7:0]							
ID	R	0x49	0x15	ID[7:0]							
HI_CODE	R	0x20	0xAD	Reserved							
LO_CODE	R	0x21	0x63	Reserved							

[1] X means don't care.
[2] N/A means not applicable.

Table 8. Status Register, STATUSA (Address 0x6)

Bit(s)	Bit Name	Bit Description
D5	Reserved	X
D4	LOL status	0 = locked 1 = frequency acquisition mode
D3	Reserved	X
D2	Static LOL	0 = no LOL event since last reset 1 = LOL event since last reset; clear using the reset static LOL bit
D0	RATE_MEAS_COMP	Rate measurement complete 0 = frequency measurement incomplete 1 = frequency measurement complete; clear using the RATE_MEAS_RESET bit

Table 9. Control Register, CTRLA (Address 0x8)

Bit(s)	Bit Name	Bit Description
D7	Reserved	Reserved to 0.
[D6:D4]	CDR_MODE[2:0]	CDR modes. 000 = lock to data (LTD). 010 = lock to reference (LTR). 001, 011 = reserved.
D3	Reserved	Reserved to 0.
D2	Reset static LOL	In factory default mode, this bit is set to 0. In the static LOL mode, write 1 and then write 0 to clear static LOL bit (D2 of the status register).
D1	RATE_MEAS_EN	Fine data rate measurement enable. Set to 1 to initiate a rate measurement.
D0	RATE_MEAS_RESET	Rate measurement reset. Set to 1 to clear a rate measurement.

Table 10. Control Register, CTRLB (Address 0x9)

Bit(s)	Bit Name	Bit Description
D7	SOFTWARE_RESET	Software reset. Write a 1 followed by a 0 to reset the device.
D6	INIT_FREQ_ACQ	Initiate frequency acquisition. Write a 1 followed by a 0 to initiate a frequency acquisition (optional).
D5	CDR bypass	CDR bypass. 0 = CDR enabled. 1 = CDR bypassed.
D4	LOL config	LOL configuration. 0 = normal LOL. 1 = static LOL.
D3	Reserved	Reserved to 1.
D2	Reserved	Reserved to 0.
[D1:D0]	Reserved	Reserved to 0.

Table 11. Control Register, CTRLC (Address 0xA)

Bit(s)	Bit Name	Bit Description
[D7:D3]	Reserved	Reserved to 0.
D2	REFCLK_PDN	Reference clock power-down. Write a 0 to enable the reference clock.
D1	Reserved	Reserved to 0.
D0	Reserved	Reserved to 1.

Table 12. Lock to Reference Clock Mode Programming Register, LTR_MODE[1] (Address 0xF)

Bit(s)	Bit Name	Bit Description
D7	Reserved	Reserved to 0
D6	LOL data	LOL data 0 = CLK vs. reference clock during tracking 1 = CLK vs. data during tracking
[D5:D4]	FREF_RANGE[1:0]	f_{REF} range 00 = 11.05 MHz to 22.1 MHz 01 = 22.1 MHz to 44.2 MHz 10 = 44.2 MHz to 88.4 MHz 11 = 88.4 MHz to 176.8 MHz
[D3:D0]	DATA_TO_REF_RATIO[3:0]	Data to reference ratio 0000 = ½ 0001 = 1 0010 = 2 N = $2^{(n-1)}$ 1010 = 512

[1] Where DIV_f_{REF} is the divided down reference referred to the 11.05 MHz to 22.1 MHz band (see the Reference Clock (Optional) section). $Data\ Rate/2^{(LTR\_MODE[3:0]-1)} = REFCLK/2^{LTR\_MODE[5:4]}$

Table 13. DPLL Control Register, DPLLA (Address 0x10)

Bit(s)	Bit Name	Bit Description
[D7:D5]	Reserved	Reserved to 0.
[D4:D3[	EDGE_SEL[1:0]	Edge for phase detection. See the Edge Select section for further details. 00 = rising and falling edge data. 01 = rising edge data. 10 = falling edge data. 11 = rising and falling edge data.
[D2:D0]	TRANBW[2:0]	Transfer bandwidth. Scales transfer bandwidth. Default value is 4, resulting in the CPRI × 16: 9.8304 Gbps default BW shown in Table 2. See the Transfer Bandwidth section for further details. *Transfer BW = Default Transfer BW* × (*TRANBW[2:0]*/4)

Table 14. DPLL Control Register, DPLLD (Address 0x13)

Bit(s)	Bit Name	Bit Description
[D7:D2]	Reserved	Reserved to 0.
[D1:D0]	DLL_SLEW[1:0]	DLL slew. Sets the BW of the DLL. See the DLL Slew section for further details.

Table 15. Phase Control Register, Phase (Address 0x14)

Bit(s)	Bit Name	Bit Description
[D7:D4]	Reserved	Reserved to 0.
[D3:D0]	SAMPLE_PHASE[3:0]	Adjusta the phase of the sampling instant for data rates above 5.65 Gbps in steps of 1/32 UI. This register is in twos complement notation. See the Sample Phase Adjust section for further details.

Table 16. Input Stage Programming Register, LA_EQ (Address 0x16)

Bit(s)	Bit Name	Bit Description
D7	RX_TERM_FLOAT	Receiver (Rx) termination float. 0 = termination common-mode driven. 1 = termination common-mode floated.
[D6:D5]	INPUT_SEL[1:0]	Input stage select. 01 = equalizer. 10 = 0 dB EQ mode. 00, 11 = undefined.
D4	ADAPTIVE_EQ_EN	Enable adaptive EQ. 0 = manual EQ control. 1 = adaptive EQ enabled.
[D3:D0]	EQ_BOOST[3:0]	Equalizer gain. These bits set the EQ gain. See the Passive Equalizer section for further details.

Table 17. Output Control Register, OUTPUTA (Address 0x1E)

Bit(s)	Bit Name	Bit Description
[D7:D6]	Reserved	Reserved to 0
D5	Data squelch	Squelch 0 = normal data 1 = squelch data
D4	DATOUT_DISABLE	Data output disable 0 = data output enabled 1 = data output disabled
D3	Reserved	Reserved to 1
D2	DDR_DISABLE	Double data rate 0 = DDR clock enabled 1 = DDR clock disabled
D1	DATA_POLARITY	Data polarity 0 = normal data polarity 1 = flip data polarity
D0	Reserved	Reserved to 0

Table 18. Output Swing Register, OUTPUTB (Address 0x1F)

Bit(s)	Bit Name	Bit Description
[D7:D4]	DATA_SWING[3:0]	Adjust data output amplitude. Step size is approximately 50 mV differential. Default register value is 0xCH. Typical differential data output amplitudes are 0x1 to 0x3 = invalid. 0x4 = 200 mV. 0x5 = 250 mV. 0x6 = 300 mV. 0x7 = 345 mV. 0x8 = 390 mV. 0x9 = 440 mV. 0xA = 485 mV. 0xB = 530 mV. 0xC = 575 mV. 0xD = 610 mV. 0xE = 640 mV. 0xF = 655 mV.
[D3:D0]	Reserved	Default = 0xCH.

THEORY OF OPERATION

The ADN2905 implements a data recovery for CPRI data rates from 614.4 Mbps to 9.8304 Gbps. The front end is configurable to either equalize or 0 dB EQ the nonreturn-to-zero (NRZ) input waveform to full-scale digital logic levels, or to pass a full digital logic signal.

The user can choose from two input stages to process the data: a high-pass passive equalizer with up to 10 dB of boost at 5 GHz, or 0 dB EQ mode with approximately 250 mV p-p sensitivity at CPRI rate 9.8304 Gbps.

When the input signal is corrupted due to FR-4 or other impairments in the printed circuit board (PCB) traces, a passive equalizer can be one of the signal integrity options. The equalizer high frequency boost is configurable through the I^2C registers, in place of the factory default settings. A user enabled adaptation is included that automatically adjusts the equalizer to achieve the widest eye opening. The equalizer can be manually set for any data rate, but adaptation is available only at data rates greater than 5.5 Gbps.

When a signal is presented to the data recovery, the ADN2905 acts as a delay-locked and phase-locked loop (PLL) circuit for clock recovery and data retiming from an NRZ encoded data stream. Input data is sampled by a high speed clock. A digital downsampler accommodates data rates spanning three orders of magnitude. Downsampled data is applied to a binary phase detector.

The phase of the input data signal is tracked by two separate feedback loops. A high speed, delay-locked loop (DLL) path cascades a digital integrator with a digitally controlled phase shifter on the digital control oscillator (DCO) clock to track the high frequency components of jitter. A separate phase control loop, composed of a digital integrator and DCO, tracks the low frequency components of jitter. The initial frequency of the DCO is set by a third loop that compares the DCO frequency with the input data frequency. This third loop also sets the decimation ratio of the digital downsampler.

The delay-locked and phase-locked loops together track the phase of the input data. For example, when the clock lags the input data, the phase detector drives the DCO to a higher frequency and decreases the delay of the clock through the phase shifter; both of these actions reduce the phase error between the clock and data. Because the loop filter is an integrator, the static phase error is driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and, therefore, does not appear in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is eliminated.

The delay-locked and phase-locked loops simultaneously provide wideband jitter accommodation and narrow-band jitter filtering. The simplified block diagram in Figure 15 shows that Z(s)/X(s) is a second-order, low-pass jitter transfer function that provides excellent filtering. The low frequency pole is formed by dividing the gain of the PLL by the gain of the DLL, where the upsampling and zero-order hold in the DLL has a gain approaching N at the transfer bandwidth of the loop. Note that the jitter transfer has no zero, unlike an ordinary, second-order phase-locked loop, which means that the main PLL has no jitter peaking. This no jitter peaking feature makes the circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, e(s)/X(s), has the same high-pass form as an ordinary phase-locked loop up to the slew rate limit of the DLL with a binary phase detector. This transfer function is free to be optimized to give excellent wideband jitter accommodation because the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering.

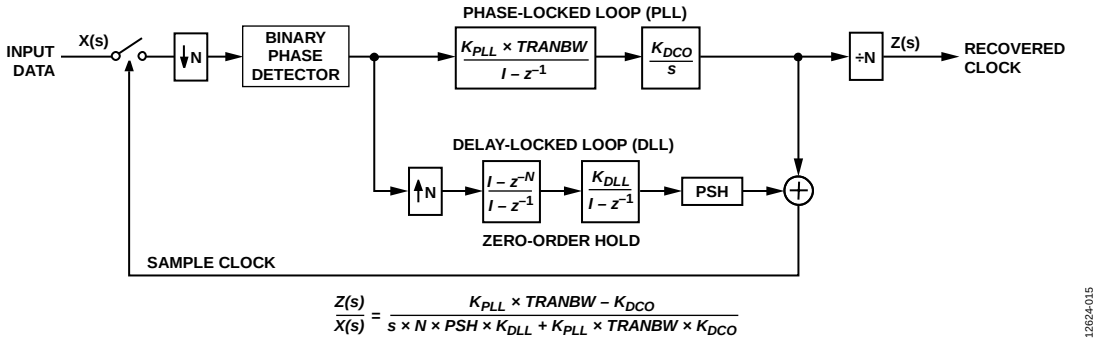


Figure 15. CDR Jitter Block Diagram

The delay-locked and phase-locked loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the oscillator is frequency modulated, and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the DCO tuning range. A wider tuning range provides more accommodation of low frequency jitter. The internal loop control word remains small for small jitter frequency, so that the phase shifter remains close to the center of its range and, therefore, contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the DCO are not large enough to track input jitter. In this case, the DCO control word becomes large and saturates. As a result, the DCO frequency remains at an extreme of its tuning range. The size of the DCO tuning range, therefore, has only a small effect on the jitter accommodation.The delay-locked loop control range is larger; therefore, the phase shifter tracks the input jitter. An infinite range phase shifter is used on the clock. Consequently, the minimum range of timing mismatch between the clock at the data sampler and the retiming clock at the output is limited by the depth of the FIFO to 32 UI.

There are two ways to acquire the data rate. The default mode is for the frequency to lock to the input data, where a finite state machine extracts frequency measurements from the data to program the DCO and loop division ratio so that the sampling frequency matches the data rate to within 250 ppm. The PLL is enabled, driving this frequency difference to 0 ppm. The second mode is to lock to reference (LTR), in which case the user provides a reference clock between 11.05 MHz and 176.8 MHz. Division ratios must be written to a serial port register.

FUNCTIONAL DESCRIPTION

FREQUENCY ACQUISITION

The ADN2905 acquires its frequency from the data over a range of data frequencies from 614.4 Mbps to 9.8304 Gbps. The lock detector circuit compares the frequency of the DCO and the frequency of the incoming data. When these frequencies differ by more than 1000 ppm, the LOL pin is asserted, and a new frequency acquisition cycle is initiated. The DCO frequency is reset to the lowest point of its range, and the internal division rate is set to its lowest value of N = 1, which is the highest octave of data rates. The frequency detector then compares this sampling rate frequency to the data rate frequency and either increases N by a factor of 2 if the sampling rate frequency is greater than the data rate frequency, or increases the DCO frequency if the data rate frequency is greater than the data sampling rate frequency. Initially, the DCO frequency is incremented in large steps to aid fast acquisition. As the DCO frequency approaches the data frequency, the step size is reduced until the DCO frequency is within 250 ppm of the data frequency, at which point LOL is deasserted.

When LOL is deasserted, the frequency-locked loop is turned off. The PLL or DLL pulls in the DCO frequency until the DCO frequency equals the data frequency.

EDGE SELECT

A binary, or Alexander, phase detector drives both the DLL and PLL at all division rates. Duty cycle distortion on the received data leads to a dead band in the phase detector transfer function if phase errors are measured on both rising and falling data transitions. This dead band leads to jitter generation of unknown spectral composition with potentially large peak-to-peak amplitudee.

The recommended usage of the device when the dc offset loop is disabled is to compute phase errors exclusively on either the rising data edges with EDGE_SEL[1:0] (Bits[D4:D3] in Register 0x10) = 1 (decimal) or on the falling data edges with EDGE_SEL[1:0] = 2. The alignment of the clock to the rising data edges with EDGE_SEL[1:0] = 1 is represented by the top two curves in Figure 16. Duty cycle distortion with narrow 1s moves the significant sampling instance where data is sampled to the right of center. The alignment of the clock to the falling data edges with EDGE_SEL[1:0] = 2 is represented by the first and third curves in Figure 16. The significant sampling instance moves to the left of center. Sample phase adjustment for rates above 5.65 Gbps can be used to move the significant sampling instance to the center of the narrow 1 (or narrow 0) for best jitter tolerance.

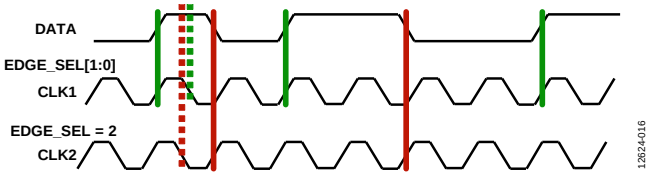


Figure 16. Phase Detector Timing

DLL Slew

Jitter tolerance beyond the transfer bandwidth of the CDR is determined by the slew rate of the delay-locked loop implementing a delta modulator on phase. Setting DLL_SLEW[1:0] = 2, (the default value) in the Register 0x13 configures the DLL to track 0.75 UI p-p jitter at the highest frequency breakpoint at 4 MHz for CPRI = 9.8304 Gbps. DPLLD[1:0] can be set to 0, giving lower jitter generation on the recovered clock and better high frequency jitter tolerance.

Sample Phase Adjustment

The phase of the sampling instant can be adjusted using the I^2C interface when the device operates at data rates of 5.65 Gbps or higher by writing to SAMPLE_PHASE[3:0] (Bits[D3:D0] in Register 0x14). This feature allows the user to adjust the sampling instant to improve the BER and jitter tolerance. Although the default sampling instant chosen by the CDR is sufficient in most applications, when dealing with some degraded input signals, the BER and jitter tolerance performance can be improved by manually adjusting the phase.

A total adjustment range of 0.5 UI is available, with 0.25 UI in each direction, in increments of 1/32 UI. SAMPLE_PHASE[3:0] is a twos complement number. The relationship between data and the sampling clock is shown in Figure 17.

Transfer Bandwidth

The transfer bandwidth can be adjusted using the I^2C interface by writing to the TRANBW[2:0] bitsin Register 0x10. The default value is 4. When set to values below 4, the transfer bandwidth is reduced. When set to values above 4, the transfer bandwidth is increased. The resulting transfer bandwidth (BW) is based on the following formula:

$$Transfer\ BW = Default\ Transfer\ BW \times \left(\frac{TRANBW[2:0]}{4}\right)$$

For example, at CPRI × 16 (9.8304 Gbps), the default transfer bandwidth is approximately 2 MHz. The resulting transfer bandwidth when TRANBW[2:0] is changed is

- TRANBW[2:0] = 1: transfer BW = 500 kHz
- TRANBW[2:0] = 2: transfer BW = 1.0 MHz
- TRANBW[2:0] = 3: transfer BW = 1.5 MHz
- TRANBW[2:0] = 4: transfer BW = 2.0 MHz (default)
- TRANBW[2:0] = 5: transfer BW = 2.5 MHz
- TRANBW[2:0] = 6: transfer BW = 3.0 MHz
- TRANBW[2:0] = 7: transfer BW = 3.5 MHz

Reducing the transfer bandwidth is commonly used in optical transport network (OTN) applications. Never set TRANBW[2:0] to 0, because this makes the CDR open loop. Also note that setting TRANBW[2:0] above 4 can cause a slight increase in jitter generation and potential jitter peaking.

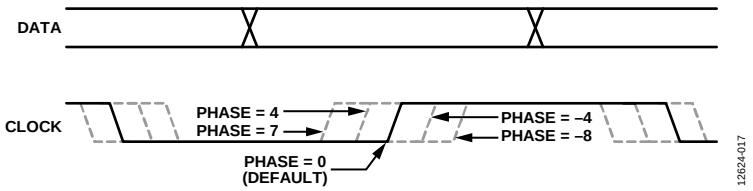


Figure 17. Data vs. Sampling Clock

PASSIVE EQUALIZER

A passive equalizer is available at the input to equalize large signals that have undergone distortion due to PCB traces, vias, or connectors. The adaptive EQ functions only at data rates greater than 5.5 Gbps. Therefore, at rates less than 5.5 Gbps, the EQ must be manually set.

The equalizer can be manually set using the LA_EQ register (Register 0x16). An adaptive loop is also available to optimize the EQ setting based on characteristics of the received eye at the phase detector. If the channel is known in advance, set the EQ manually to obtain the best performance; however, the adaptive EQ finds the best setting in most cases.

Table 19 lists the typical EQ settings for several trace lengths. The values in Table 19 are based on measurements taken on a test board with simple FR-4 traces. Table 20 lists the typical maximum reach in inches of FR-4 of the EQ at several data rates. If a real channel includes lossy connectors or vias, the FR-4 reach length is lower. For any real-world system, it is highly recommended to test several EQ settings with the real channel to ensure the best signal integrity.

Table 19. EQ Settings vs. Trace Length on FR-4

Trace Length (Inches)	Typical EQ Setting
6	10
10	12
15	14
20 to 30	15

Table 20. Typical EQ Reach on FR-4 vs. Maximum Data Rates Supported

Maximum Data Rate (Gbps)	Typical EQ Reach on FR-4 (Inches)
4	30
8	20
10	15
11	10

0 dB EQ

The 0 dB EQ path connects the input signal directly to the digital logic inside the ADN2905. The 0 dB EQ is useful at lower data rates where the signal is large (therefore, the limiting amplifier is not needed, and power can be saved by deselecting the limiting amplifier) and unimpaired (therefore, the equalizer is not needed). The signal swing of the internal digital circuit is 600 mV p-p differential, the minimum signal amplitude that must be provided in 0 dB EQ mode.

In 0 dB EQ mode, the internal 50 Ω termination resistors can be configured in one of two ways, either floated or tied to VCC = 1.2 V (see Figure 22 and Table 23). By setting the RX_TERM_FLOAT bit (Bit D7 in Register 0x16) to 1, these 50 Ω termination resistors are floated internal to the ADN2905 (see Figure 25). By setting the RX_TERM_FLOAT bit to 0, these 50 Ω termination resistors are connected to VCC = 1.2 V (see Figure 26). In both termination cases, the user must ensure a valid common-mode voltage on the input.

When the termination is floated, the two 50 Ω resistors are a purely differential termination. The input must conform to the range of signals shown in Figure 28.

When the termination is connected to a 1.2 V VCC power supply (see Figure 26 and Figure 27), the common-mode voltage is created by the driver circuit and the 50 Ω resistors on the ADN2905. For example, the driver can be an open-drain switched current (see Figure 26), and the 50 Ω resistors return this current to VCC. In Figure 26, the common-mode voltage is created by both the current and the resistors. In this case, ensure that the current is a minimum of 6 mA, which gives a single-ended swing of 300 mV or a differential swing of 600 mV p-p differential, with V_{CM} = 1.05 V (see Figure 28). The maximum current is 10 mA, which gives a single-ended 500 mV swing and a differential 1.0 V p-p swing with V_{CM} = 0.95 V (see Figure 29).

Another possibility is to back terminate the switched current driver, as shown in Figure 27, with the two VCC supplies having the same potential. In this example, the current is returned to VCC by the two 50 Ω resistors in parallel, or 25 Ω, so that the minimum current is 12 mA and the maximum current is 20 mA.

LOCK DETECTOR OPERATION

The lock detector on the ADN2905 has three modes of operation: normal mode, LTR mode, and static LOL mode.

Normal Mode

In normal mode, the ADN2905 is a multiple rate data recovery device that locks onto the CPRI data rate from 614.4 Mbps to 9.8304 Gbps without the use of a reference clock as an acquisition aid. In this mode, the lock detector monitors the frequency difference between the DCO and the input data frequency, and deasserts the loss of lock signal, which appears on LOL (Pin 6) when the DCO is within 250 ppm of the data frequency. This enables the digital PLL (DPLL), which pulls the DCO frequency in the remaining amount and acquires phase lock. When locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is reasserted and control returns to the frequency loop, which begins a new frequency acquisition. The LOL pin remains asserted until the DCO locks onto a valid input data stream to within 250 ppm frequency error. This hysteresis is shown in Figure 18.

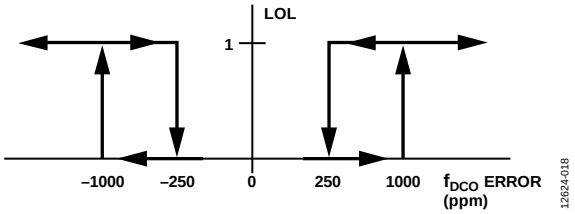


Figure 18. Transfer Function of LOL

LOL Detector Operation Using a Reference Clock (LTR Mode)

In lock to reference (LTR) mode, a reference clock is used as an acquisition aid to lock the ADN2905 DCO. LTR mode is enabled by setting the CDR_MODE[2:0] bits to 2 (Bits[D6:D4] in Register 0x8). The user must also write to the FREF_RANGE[1:0] bits and the DATA_TO_ REF_RATIO[3:0] bits (Bits[D5:D4] and Bits[D3:D0] in Register 0xF) to set the reference frequency range and the divide ratio of the data rate with respect to the reference frequency. Finally, the reference clock power down to the reference clock buffer must be deasserted by writing a 0 to the REFCLK_PDN bit (Bit D2 in Register 0xA). To maintain fastest acquisition, keep Bit D0 in Register 0xA set to 1.

For more details, see the Reference Clock (Optional) section. In LTR mode, the lock detector monitors the difference in frequency between the divided down DCO and the divided down reference clock. The loss of lock signal, which appears on LOL (Pin 6), is deasserted when the DCO is within 250 ppm of the desired frequency. This enables the DPLL, which pulls in the DCO frequency by the remaining amount with respect to the input data and acquires phase lock. When locked, if the frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is reasserted and control returns to the frequency loop, which reacquires lock with respect to the reference clock. The LOL pin remains asserted until the DCO frequency is within 250 ppm of the desired frequency. This hysteresis is shown in Figure 18.

Static LOL Mode

The ADN2905 implements a static LOL feature that indicates whether a loss of lock condition has ever occurred and remains asserted, even if the ADN2905 regains lock, until the static LOL bit (Bit D2 in Register 0x6) is manually reset. If a loss of lock condition occurs, this bit is internally asserted to logic high. The static LOL bit remains high even after the ADN2905 reacquires lock to a new data rate. This bit can be reset by writing a 1, followed by 0, to the reset static LOL bit (Bit D2 in Register 0x8). When reset, the static LOL bit remains deasserted until another loss of lock condition occurs.

Writing a 1 to the LOL configuration bit (Bit D4 in Register 0x9) causes the LOL pin (Pin 6) to become a static LOL indicator. In this mode, the LOL pin mirrors the contents of the static LOL bit (Bit D2 in Register 0x6) and has the functionality described previously. The LOL configuration bit defaults to 0. In this mode, the LOL pin operates in the normal operating mode; that is, it is asserted only when the ADN2905 is in acquisition mode and deasserts when the ADN2905 has reacquired lock.

HARMONIC DETECTOR

The ADN2905 provides a harmonic detector that detects whether the input data has changed to a lower harmonic of the data rate than the one that the sampling clock is currently locked onto. For example, if the input data instantaneously changes from a CPRI × 16 (9.8304 Gbps) to a CPRI × 4 (2.4576 Gbps) bit stream, this can be perceived as a valid CPRI × 16 bit stream because the CPRI × 4 data pattern is exactly 4× slower than the CPRI × 16 pattern. Therefore, if the change in data rate is instantaneous, a 101 pattern at CPRI × 4 (2.4576 Gbps) is perceived by the ADN2905 as a 111100001111 pattern at CPRI × 16 (9.8304 Gbps). If the change to a lower harmonic is instantaneous, a typical inferior CDR may remain locked at the higher data rate.

The ADN2905 implements a harmonic detector that automatically identifies whether the input data has switched to a lower harmonic of the data rate than the one that the DCO is currently locked onto. When a harmonic is identified, the LOL pin is asserted, and a new frequency acquisition is initiated. The ADN2905 automatically locks onto the new data rate, and the LOL pin is deasserted.

The time to detect a lock to harmonic is

$$2^{16} \times (T_D/\rho)$$

where:
$1/T_D$ is the new data rate. For example, if the data rate is switched from CPRI × 16 (9.8304 Gbps) to CPRI × 4 (2.4576 Gbps), T_D = 1/2.4576 GHz.
ρ is the data transition density. Most coding schemes seek to ensure that ρ = 0.5, for example, PRBS and 8B/10B.

When the ADN2905 is placed in lock to reference mode, the harmonic detector is disabled.

OUTPUT DISABLE AND SQUELCH

The ADN2905 offers output disable/squelch. The DATOUTP/DATOUTN outputs can be disabled by setting the DATOUT_DISABLE bit (Bit D4 in Register 0x1E) high. When an output is

disabled, it is fully powered down, saving approximately 30 mW total power.

To set the data output while leaving the clock on, the output data can be squelched by setting the data squelch bit (Bit D5 in Register 0x1E) high. In this mode, the data driver remains powered, but the data itself is forced to be a value of 0 or 1, depending on the setting of the DATA_POLARITY bit (Bit D1 in Register 0x1E).

I²C INTERFACE

The ADN2905 supports a 2-wire, I²C-compatible, serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any devices connected to the bus. Each slave device is recognized by a unique address. The slave address consists of the seven MSBs of an 8-bit word. The upper six bits (Bits[6:1]) of the 7-bit slave address are factory programmed to 100000. The LSB of the slave address (Bit 0) is set by Pin 22, I²C_ADDR. The LSB of the word specifies either a read or write operation (see Figure 10). Logic 1 corresponds to a read operation, whereas Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be used:

1. The master initiates a data transfer by establishing a start condition, defined as a high to low transition on SDA while SCK remains high. This indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is an acknowledge bit.
4. All other devices withdraw from the bus at this point and maintain an idle condition. In the idle condition, the device monitors the SDA and SCK lines waiting for the start condition and the correct transmitted address.

The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2905 acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W bit. The ADN2905 has subaddresses to enable the user-accessible internal registers (see Table 7).

The ADN2905, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Auto-increment mode is supported, allowing data to be read from or written to the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCK high period, issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If the user issues an invalid subaddress, the ADN2905 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while reading back in auto-increment mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. In a no acknowledge condition, the SDA line is not pulled low on the ninth pulse. See Figure 11 and Figure 12 for sample read and write data transfers, respectively, and Figure 13 for a more detailed timing diagram.

REFERENCE CLOCK (OPTIONAL)

A reference clock is not required to perform data recovery with the ADN2905. However, support for an optional reference clock is provided. The reference clock can be driven differentially or single-ended. If the reference clock is not used, float both the REFCLKP and REFCLKN pins.

Two 50 Ω series resistors present a differential load between REFCLKP and REFCLKN. Common mode is internally set to 0.56 × VCC by a resistor divider between VCC and VEE. See Figure 19, Figure 20, and Figure 21 for sample configurations.

The reference clock input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV. The phase noise and duty cycle of the reference clock are not critical, and a 100 ppm accuracy is sufficient.

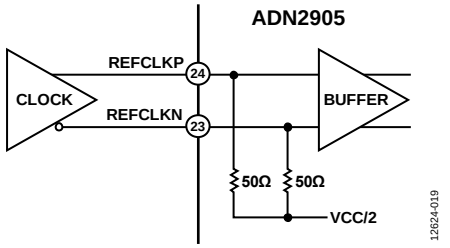


Figure 19. DC-Coupled, Differential REFCLKx Configuration

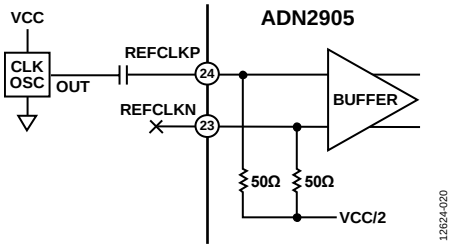


Figure 20. AC-Coupled, Single-Ended REFCLKx Configuration

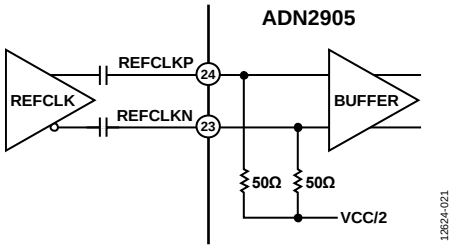


Figure 21. AC-Coupled, Differential REFCLKx Configuration

The reference clock can be used either as an acquisition aid for the ADN2905 to lock onto data, or to measure the frequency of the incoming data to within 0.01%. The modes are mutually exclusive because, in the first use, the user can force the device to lock onto only a known data rate; in the second use, the user can measure an unknown data rate.

Lock to reference mode is enabled by writing a 2 to the CDR_MODE[2:0] bits (Bits[D6:D4] in Register 0x8). An on-chip clock buffer must be powered on by writing a 0 to the REFCLK_PDN bit (Bit D2 in Register 0xA). Fine data rate readback mode is enabled by writing a 1 to the RATE_MEAS_EN bit (Bit D1 in Register 0x8). Enabling lock to reference and data rate readback at the same time causes an indeterminate state and is not supported.

Using the Reference Clock to Lock onto Data

In LTR mode, the ADN2905 locks onto a frequency derived from the reference clock according to the following equation:

$$Data\ Rate/2^{(LTR\_MODE[3:0]-1)} = REFCLK/2^{LTR\_MODE[5:4]}$$

The user must know exactly what the data rate is and provide a reference clock that is a function of this rate. The ADN2905 can still be used as a continuous rate device in this configuration if the user can provide a reference clock that has a variable frequency (see the AN-632 Application Note).

The reference clock can have a frequency from 11.05 MHz to 176.8 MHz. By default, the ADN2905 expects a reference clock of between 11.05 MHz and 22.1 MHz. If the reference clock is between 22.1 MHz and 44.2 MHz, 44.2 MHz and 88.4 MHz, or 88.4 MHz and 176.8 MHz, the user must configure the ADN2905 to use the correct reference frequency range by setting the two bits of FREF_RANGE[1:0] (Bits[D5:D4] in Register 0xF).

Table 21. LTR_MODE Register Settings

FREF_RANGE[1:0]	Range (MHz)	DATA_TO_REF_RATIO[3:0]	Ratio
00	11.05 to 22.1	0000	2^{-1}
01	22.1 to 44.2	0001	2^{0}
10	44.2 to 88.4	n	2^{n-1}
11	88.4 to 176.8	1010	2^{9}

The user can specify a fixed integer multiple of the reference clock to lock onto using the DATA_TO_REF_RATIO[3:0] bits (Bits[D3:D0] in Register 0xF), as follows:

$$DATA\_TO\_REF\_RATIO[3:0] = Data\ Rate \div DIV\_f_{REF}$$

where DIV_f_{REF} represents the divided-down reference referred to the 11.05 MHz to 22.1 MHz band.

For example, if the reference clock frequency is 38.88 MHz and the input data rate is 622.08 Mbps, the FREF_RANGE[1:0] bits are set to 01 to give a divided-down reference clock of 19.44 MHz. DATA_TO_REF_RATIO[3:0] is set to 0110, that is, 6, because

$$622.08\ Mbps/19.44\ MHz = 2^{(6-1)}$$

If the ADN2905 is operating in lock to reference mode, and the user changes the reference frequency, the f_{REF} range or the f_{REF} ratio (Bits[D5:D4] or Bits[D3:D0], respectively, in Register 0xF), this change must be followed by writing a low to high to low transition to the INIT_FREQ_ACQ bit (Bit D6 in Register 0x9) to initiate a new lock to reference command.

By default in lock to reference clock mode, when lock has been achieved and the ADN2905 is in tracking mode, the frequency of the DCO is compared to the frequency of the reference clock. If this frequency error exceeds 1000 ppm, lock is lost, LOL is asserted, and the device relocks to the reference clock while continuing to output a stable clock.

An alternative configuration is enabled by setting LOL data (Bit D6 in Register 0xF) to 1. In this configuration, when the device is in tracking mode, the frequency of the DCO is compared to the frequency of the input data rather than the frequency of the reference clock. If this frequency error exceeds 1000 ppm, lock is lost, LOL is asserted, and the device relocks to the reference clock while continuing to output a stable clock.

Using the Reference Clock to Measure Data Frequency

The user can also provide a reference clock to measure the recovered data frequency. In this case, the user provides a reference clock, and the ADN2905 compares the frequency of the incoming data to the incoming reference clock and returns a ratio of the two frequencies to 0.01% (100 ppm). The accuracy error of the reference clock is added to the accuracy error of the ADN2905 data rate measurement. For example, if a 100 ppm accuracy reference clock is used, the total accuracy of the measurement is 200 ppm.

The reference clock can range from 11.05 MHz and 176.8 MHz. Prior to reading back the data rate using the reference clock, the FREF_RANGE[1:0] bits (Bits[D5:D4] in Register 0xF) must be set to the appropriate frequency range with respect to the reference clock being used according to Table 21.

A fine data rate readback is then executed as follows:

1. Apply the reference clock.
2. Write a 0 to the REFCLK_PDN bit (Bit D2 in Register 0xA) to enable the reference clock circuit.
3. Write to the FREF_RANGE[1:0] bits(Bits[D5:D4] in Register 0xF) to select the appropriate reference clock frequency circuit.
4. Write a 1 to the RATE_MEAS_EN bit (Bit D1 in Register 0x8) to enable the fine data rate measurement capability of the ADN2905. This bit is level sensitive and does not need to be reset to perform subsequent frequency measurements.
5. Write a low to high to low transition to the RATE_MEAS_RESET bit (Bit D0 in Register 0x8) to initiate a new data rate measurement.
6. Read back the RATE_MEAS_COMP bit (Bit D0 in Register 0x6). If the bit is 0, the measurement is not complete. If it is 1, the measurement is complete and the data rate can be read back on the RATE_FREQ[23:0] and FREQ_RB2[6:2] bits (see Table 7). The approximate time for a data rate measurement is given in Equation 2.

Use the following equation to determine the data rate:

$$f_{DATARATE} = \frac{(RATE\_FREQ[23:0] \times f_{REFCLK})}{2^{LTR[5:4]} \times 2^7 \times 2^{FULLRATE} \times 2^{DIVRATE}} \quad (1)$$

where:
$f_{DATARATE}$ is the data rate in Mbps.
RATE_FREQ[23:0] is from FREQ2[7:0] (most significant byte), FREQ1[7:0], and FREQ0[7:0] (least significant byte). See Table 7.
f_{REFCLK} is the reference clock frequency in MHz.
LTR[5:4] = LTR_MODE[5:4].
FULLRATE = FREQ_RB2[6] (Bit D6 in Register 0x5).
DIVRATE = FREQ_RB2[5:2] (Bits[D5:D2] in Register 0x5).

MSB		LSB
D23 to D16	**D15 to D8**	**D7 to D0**
FREQ2[7:0]	FREQ1[7:0]	FREQ0[7:0]

Consider the example of a 1.25 Gbps (GE) input signal and a reference clock source of 32 MHz at the PIN/NIN and REFCLKP/REFCLKN ports, respectively. In this case, the FREF_RANGE[1:0] bits(Bits[D5:D4] in Register 0xF) are 01, and the reference frequency falls into the range of 22.1 MHz to 44.2 MHz. After following Step 1 through Step 6, the readback value of the RATE_FREQ[23:0] bits is 0x13880, which is equal to 8×10^4. The readback value of the FULLRATE bit (Bit D6 in Register 0x5) is 1, and the readback value of the DIVRATE[3:0] bits (Bits[D5:D2] in Register 0x5) is 2. Inserting these values into Equation 1 yields

$$((8 \times 10^4) \times (32 \times 10^6))/(2^1 \times 2^7 \times 2^1 \times 2^2) = 1.25 \text{ Gbps}$$

If subsequent frequency measurements are required, keep the RATE_MEAS_EN bit (Bit D1 in Register 0x8) set to 1. It does not need to be reset. The measurement process is reset by writing a 1 followed by a 0 to the RATE_MEAS_RESET bit (Bit D0 in Register 0x8). This initiates a new data rate measurement. Follow Step 2 through Step 6 to read back the new data rate. Note that a data rate readback is valid only if the LOL pin is low. If LOL is high, the data rate readback is invalid.

Initiating a frequency measurement by writing a low to high to low transition to the RATE_MEAS_RESET bit (Bit D0 in Register 0x8) also resets the RATE_MEAS_COMP bit (Bit D10 in Register 0x6). The approximate time to complete a frequency measurement from the RATE_MEAS_RESET bit being written with a low to high to low transition to when the RATE_MEAS_COMP bit returns high is given by

$$Measurement\ Time = \frac{2^{11} \times 2^{LTR[5:4]}}{f_{REFCLK}} \quad (2)$$

ADDITIONAL FEATURES AVAILABLE VIA THE I²C INTERFACE

Coarse Data Rate Readback

The data rate can be read back over the I²C interface to approximately ±5% without using an external reference clock according to the following formula:

$$Data\ Rate = \frac{f_{DCO}}{2^{FULLRATE} \times 2^{DIVRATE}} \quad (3)$$

where
f_{DCO} is the frequency of the DCO, derived as shown in Table 22.
FULLRATE = FREQ_RB2[6] (Bit D6 in Register 0x5).
DIVRATE = FREQ_RB2[5:2] (Bits[D5:D2] in Register 0x5).

Four oscillator cores, defined by the VCOSEL[9:8] bits (Bits[D1:D0] in Register 0x5), span the highest octave of data rates according to Table 22.

Table 22. DCO Center Frequency vs. VCOSEL[9:8]

Core = (VCOSEL[9:8])	Minimum Frequency (MHz) = MIN_F (Core)	Maximum Frequency (MHz) = MAX_F (Core)
0	5570	7105
1	7000	8685
2	8610	10,330
3	10,265	11,625

Determine f_{DCO} from the VCOSEL[9:0] bits (Bits[D7:D0] in Register 0x4, and Bits[D1:D0] in Register 0x5), using the following formula:

$$f_{DCO} = MIN\_F(core) + \frac{MAX\_F(core) - MIN\_F(core)}{256} \times VCOSEL[9:0] \quad (4)$$

Worked Example

Read back the contents of the FREQ_RB1 and FREQ_RB2 registers. For example, with a CPRI × 16 (9.8304 Gbps) signal presented to the PIN/NIN ports

FREQ_RB1 = 0xBA
FREQ_RB2 = 0x02
FULLRATE (FREQ_RB2[6]) = 0
DIVRATE (FREQ_RB2[5:2]) = 0
Core (FREQ_RB2[1:0]) = 2

Then

f_{DCO} =

$$8610\ \text{Mbps} + \frac{10{,}300\ \text{Mbps} - 8610\ \text{Mbps}}{256} \times 186 = 9837.89\ \text{Mbps}$$

and

$$f_{data} = \frac{9837.89\ \text{Mbps}}{2^0 \times 2^0} = 9.83789\ \text{Gbps}$$

Initiate Frequency Acquisition

A frequency acquisition can be initiated by writing a 1 followed by a 0 to the INIT_FREQ_ACQ bit (Bit D6 in Register 0x9). This initiates a new frequency acquisition while keeping the ADN2905 in the operating mode that was previously programmed in the CTRLA, CTRLB, and CTRLC registers.

PRBS Generator/Receiver

The ADN2905 has an integrated PRBS generator and detector for system testing purposes. The devices are configurable as either a PRBS detector or a PRBS generator.

The following steps configure the PRBS detector:

1. Set the DATA_RECEIVER_ENABLE bit (Bit D2 in Register 0x3F) to 1 while also setting the DATA_RECEIVER_MODE[1:0] bits (Bits[D1:D0] in Register 0x3F]) according to the desired PRBS pattern (0 = PRBS7; 1 = PRBS15; 2 = PRBS31). Setting the DATA_RECEIVER_MODE[1:0] bits to 3 leads to a one shot sampling of recovered data into the DATA_LOADED[15:0] bits.
2. Set the DATA_RECEIVER_CLEAR bit (Bit D3 in Register 0x3F) to 1 followed by 0 to clear the PRBS_ERROR and PRBS_ERROR_COUNT bits.
3. The states of the PRBS_ERROR bit (Bit D0 in Register 0x41) and the PRBS_ERROR_COUNT[7:0] bits (Bits[D7:D0] in Register 0x40) can be frozen by setting the DATA_RECEIVER_ENABLE bits (Bit D2 in Register 0x3F) to 0.

The following steps configure the PRBS generator:

1. Set the DATA_GEN_EN bit(Bit D2 in Register 0x39) to 1 to enable the PRBS generator and set the DATA_GEN_MODE[1:0] bits (Bits[D1:D0] in Register 0x39) for the desired PRBS output pattern (0 = PRBS7; 1 = PRBS15; 2 = PRBS31). An arbitrary 32-bit pattern stored as PROG_DATA[31:0] is activated by setting the DATA_GEN_MODE[1:0] bits to 3.
2. Strings of consecutive identical digits (CIDs) sensed from the DATA_CID_BIT bit (Bit D5 in Register 0x39) can be introduced in the generator by setting the DATA_CID_EN bit (Bit D4 in Register 0x39) to 1. The length of CIDs is 8 × DATA_CID_LENGTH, which is set via Bits[D7:D0] in Register 0x3A.

Table 23. PRBS Settings

PRBS Pattern	DATA_GEN_MODE[1:0]	PRBS Polynomial
PRBS7	0x00	$1 + x^6 + x^7$
PRBS15	0x01	$1 + x^{14} + x^{15}$
PRBS31	0x10	$1 + x^{28} + x^{31}$
PROG_DATA[31:0]	0x11	N/A

Double Data Rate Mode

The default output clock mode is a double data rate (DDR) clock, where the output clock frequency is ½ the data rate. DDR mode allows direct interfacing to FPGAs that support clocking on both rising and falling edges. Setting the DDR_DISABLE bit (Bit D2 in Register 0x1E) to 1 enables full data rate mode. Full data rate mode is not supported for data rates in the highest octave between 5.6 Gbps and 9.8304 Gbps.

CDR Bypass Mode

The CDR in the ADN2905 can be bypassed by setting the CDR bypass bit (Bit D5 in Register 0x9) to 1. In this mode, the ADN2905 feeds the input directly through the input amplifiers to the output buffer, bypassing the CDR. The CDR bypass path is intended for use in testing or debugging a system. Use the CDR bypass path at data rates at or below 3.0 Gbps only.

Transmission Lines

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections: PIN, NIN, DATOUTP, and DATOUTN (also REFCLKP and REFCLKN, if using a high frequency reference clock, such as 155 MHz). It is also necessary for the PIN and NIN input traces to be matched in length, and the DATOUTP and DATOUTN output traces to be matched in length to avoid skew between the differential traces.

The high speed inputs (PIN and NIN) are each internally terminated with 50 Ω to an internal reference voltage (see Figure 26). As with any high speed, mixed-signal circuit, take care to keep all high speed digital traces away from sensitive analog nodes.

The high speed outputs (DATOUTP, DATOUTN) are internally terminated with 50 Ω to VCC.

Soldering Guidelines for Lead Frame Chip Scale Package

The lands on the 24-lead LFCSP are rectangular. The printed circuit board pad for these is 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. Center the land on the pad to ensure that the solder joint size is maximized. The bottom of the lead frame chip scale package has a central exposed pad. The pad on the printed circuit board must be at least as large as this exposed pad. Connect the exposed pad to VEE using plugged vias to prevent solder from leaking

through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

It is highly recommended to include as many vias as possible when connecting the exposed pad to VEE. This minimizes the thermal resistance between the die and VEE, and minimizes the die temperature. It is recommended that the vias be connected to a VEE plane, or planes, rather than a signal trace to improve heat dissipation, as shown in Figure 23.

Placing an external VEE plane on the backside of the board opposite the ADN2905 provides an additional benefit because this allows easier heat dissipation into the ambient environment.

INPUT CONFIGURATIONS

The ADN2905 input stage can work with the signal source in an ac-coupled or dc-coupled configuration. To best fit in a required applications environment, the ADN2905 supports one of following input modes: equalizer, or bypass. The ADN2905 can be configured to use any required input configuration through the I²C bus. Figure 22 shows a block diagram of the input stage circuit.

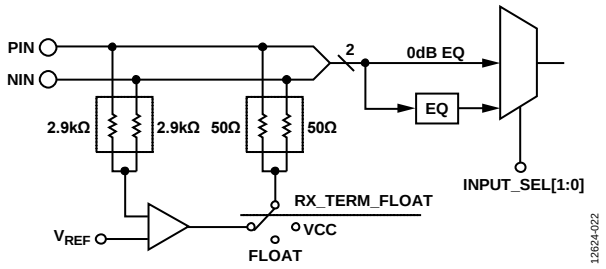


Figure 22. Input Stage Block Diagram

The input signal path is configurable with the INPUT_SEL[1:0] bits (Bits[D6:D5] in Register 0x16). Table 24 shows the INPUT_SEL[1:0] bits and the input signal configuration.

Table 24. Input Signal Configuration

Selected Input	INPUT_SEL[1:0]	RX_TERM_FLOAT = 0	RX_TERM_FLOAT = 1	ADN2905 Availability
Limiting Amplifier	00	V_{REF}	Not defined	Not defined
Equalizer	01	V_{REF}	Not defined	Yes
0 dB EQ	10	VCC	Float	Yes
Not Defined	11	Not defined	Not defined	Not defined

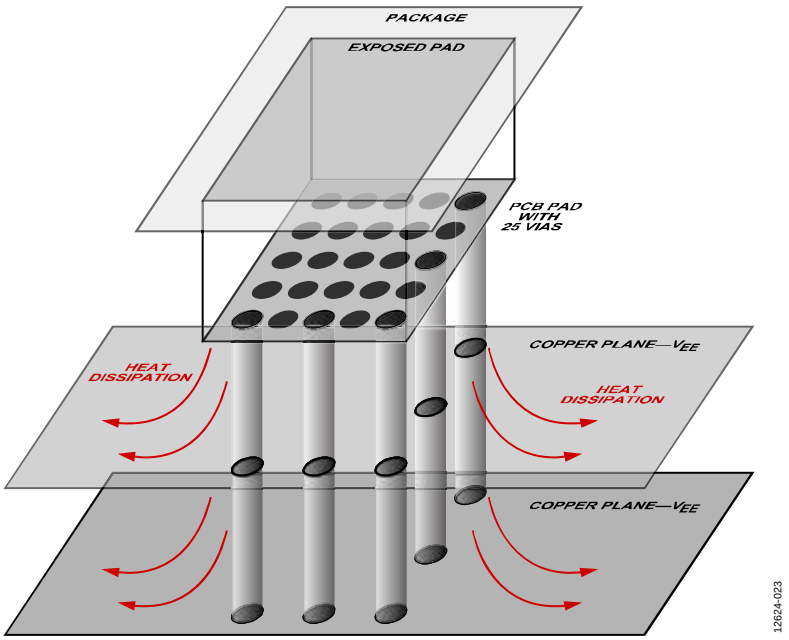


Figure 23. Connecting Vias to VEE

Choosing AC Coupling Capacitors

AC coupling capacitors at the inputs (PIN, NIN) and outputs (DATOUTP, DATOUTN) of the ADN2905 must be chosen such that the device works properly over the full range of data rates used in the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander (see Figure 24), causing pattern dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection may require some trade-offs between droop and PDJ.

For example, assuming that 2% droop is tolerable, the maximum differential droop is 4%.

Normalizing to V p-p,

$$Droop = \Delta\ V = 0.04\ V = 0.5\ V\ p\text{-}p\ (1 - e^{-t/\tau})$$

Therefore,

$$\tau = 12t$$

where:
τ is the RC time constant (C is the ac coupling capacitor, R = 100 Ω seen by C).
t is the total discharge time.

$$t = nT$$

where:
n is the number of CIDs.
T is the bit period.

Calculate the capacitor value by combining the equations for τ and t.

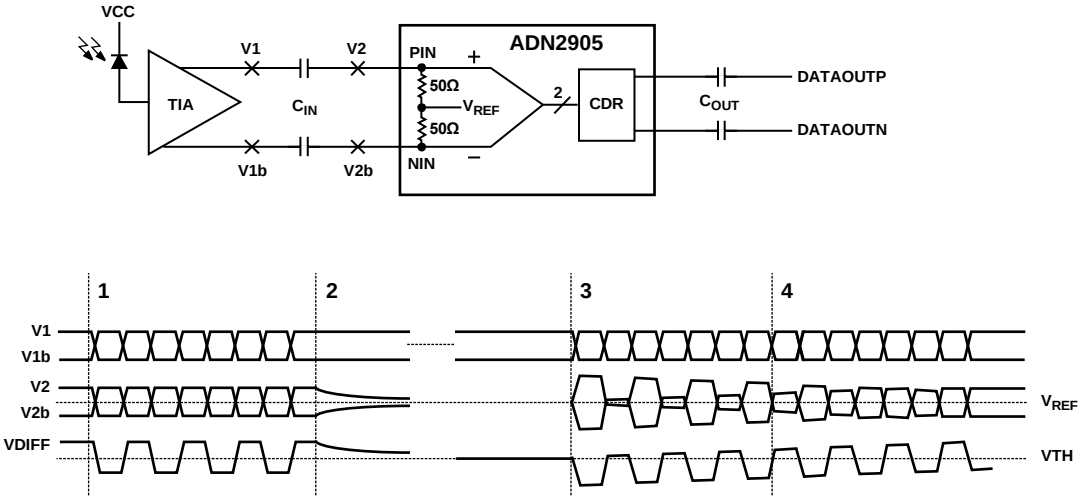
$$C = 12nT/R$$

When the capacitor value is selected, the PDJ can be approximated as

$$PDJ_{ps\ p\text{-}p} = 0.5t_R(1 - e^{(-nT/RC)}/0.6$$

where:
$PDJ_{ps\ p\text{-}p}$ is the amount of pattern dependent jitter allowed, <0.01 UI p-p typical.
t_R is the rise time, which is equal to $0.22/BW$; $BW \approx 0.7$ (bit rate).

Note that this expression for t_R is accurate only for the inputs. The output rise time for the ADN2905 is ~30 ps regardless of data rate.



VDIFF = V2 – V2b
VTH = ADN2905 QUANTIZER THRESHOLD

NOTES
1. DURING THE DATA PATTERNS WITH HIGH TRANSITION DENSITY, DIFFERENTIAL DC VOLTAGE AT V1 AND V2 IS ZERO.
2. WHEN THE TIA OUTPUTS CONSECUTIVE IDENTICAL DIGITS, V1 AND V1b ARE DRIVEN TO DIFFERENT DC LEVELS. V2 AND V2b DISCHARGE TO THE V_{REF} LEVEL, WHICH EFFECTIVELY INTRODUCES A DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS.
3. WHEN THE BURST OF DATA STARTS AGAIN, THE DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS IS APPLIED TO THE INPUT LEVELS, CAUSING A DC SHIFT IN THE DIFFERENTIAL INPUT. THIS SHIFT IS LARGE ENOUGH THAT ONE OF THE STATES, EITHER HIGH OR LOW, DEPENDING ON THE LEVELS OF V1 AND V1b WHEN THE TIA WENT TO CID, IS CANCELLED OUT. THE QUANTIZER DOES NOT RECOGNIZE THIS AS A VALID STATE.
4. THE DC OFFSET SLOWLY DISCHARGES UNTIL THE DIFFERENTIAL INPUT VOLTAGE EXCEEDS THE SENSITIVITY OF THE ADN2905. THE QUANTIZER RECOGNIZES BOTH HIGH AND LOW STATES AT THIS POINT.

12624-024

Figure 24. Example of Baseline Wander

DC-COUPLED APPLICATION

The inputs to the ADN2905 can also be dc-coupled. This can be necessary in burst mode applications with long periods of CIDs and where baseline wander cannot be tolerated. If the inputs to the ADN2905 are dc-coupled, care must be taken not to violate the input range and common-mode level requirements of the ADN2905 (see Figure 28 or Figure 29). If dc coupling is required, and the output levels of the transimpedance amplifier (TIA) do not adhere to the levels shown in Figure 28 or Figure 29, level shifting and/or attenuation must occur between the TIA outputs and the ADN2905 inputs.

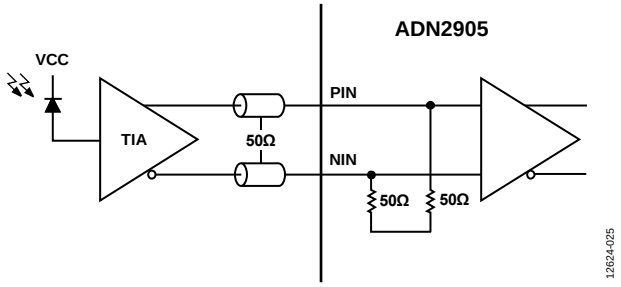


Figure 25. DC-Coupled Application, Bypass Input (Rx Termination Float Mode)

Figure 26 shows the default dc-coupled configuration when using the bypass input. The two terminations are connected directly to VCC in a normal CML fashion, giving a common mode that is set by the dc signal strength from the driving chip. The bypass input has a high common-mode range and can tolerate V_{CM} up to and including VCC.

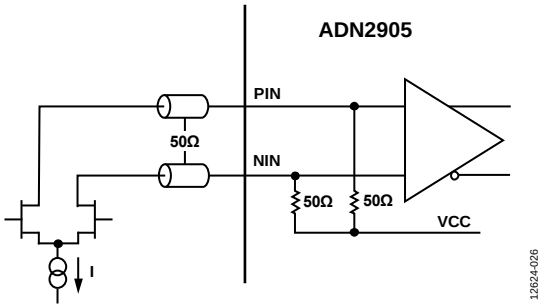


Figure 26. DC-Coupled Application, Bypass Input (Normal Mode)

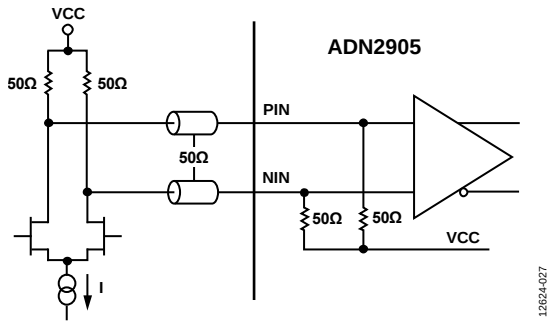


Figure 27. DC-Coupled Application, Bypass Input (Back Terminated Mode)

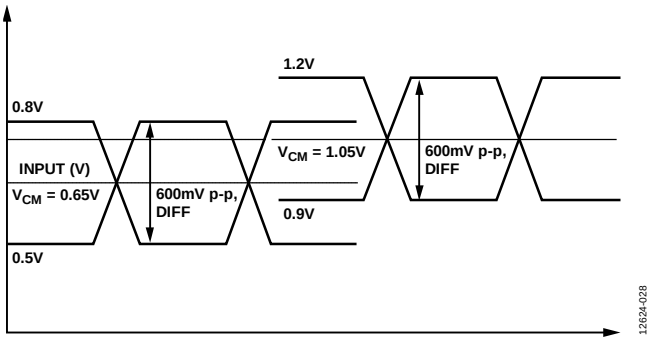


Figure 28. Minimum Allowed DC-Coupled Input Levels

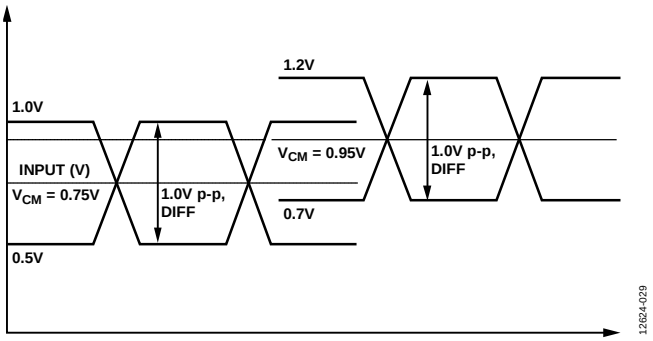


Figure 29. Maximum Allowed DC-Coupled Input Levels

OUTLINE DIMENSIONS

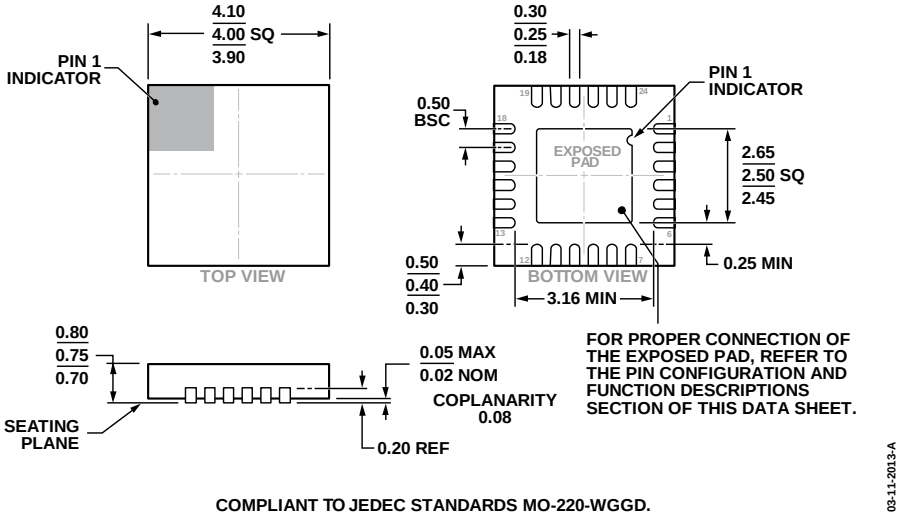


Figure 30. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADN2905ACPZ	−40°C to +85°C	24-Lead LFCSP	CP-24-7	490
ADN2905ACPZ-RL7	−40°C to +85°C	24-Lead LFCSP	CP-24-7	1,500
EVALZ-ADN2905		Evaluation Board		

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).