阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

SYNCHRONOUS ETHERNET WAN PLL and Clock Generation for IEEE-1588

Product Brief
82V3391

FEATURES

HIGHLIGHTS

- Single chip PLL:
  - Features 0.5 mHz to 560 Hz bandwidth
  - Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
  - Exceeds GR-253-CORE (OC-192) and ITU-T G.813 (STM-64) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments
  - Provides clocks for 1 Gigabit and 10 Gigabit Ethernet application
  - Supports clock generation for IEEE-1588 applications

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, Stratum 4E, Stratum 4, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Supports 1PPS input and output
- Employs PLL architecture to feature excellent jitter performance and minimize the number of external components
- Integrates T4 DPLL and T0 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports programmable DPLL bandwidth (0.5 mHz to 560 Hz in 19 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Supports hitless reference switching to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Provides OUT1~OUT7 output clocks whose frequency cover from 1PPS to 644.53125 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS outputs
  - Includes 25.78125 MHz, 128.90625 MHz and 161.1328125 MHz for CMOS outputs
  - Includes 25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, 322.265625 MHz and 644.53125 MHz for differential outputs
- Provides OUT8 for composite clocks and OUT9 for 1.544 MHz/ 2.048 MHz (BITS/SSU)
- Provides IN1 and IN2 for composite clocks
- Provides IN3~IN14 input clocks whose frequencies cover from 2 kHz to 625 MHz
  - Includes 25MHz, 125 MHz and 156.25 MHz for CMOS inputs
  - Includes 25MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential inputs
- Internal DCO can be controlled by an external processor to be used for IEEE-1588 clock generation
- Supports Forced or Automatic operating mode switch controlled by an internal state machine. Automatic mode switch supports Free-Run, Locked and Holdover modes
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz, or 8 kHz frame sync input signal, and a 2 kHz or 8 kHz frame sync output signal
- Provides a 1PPS sync Input signal, and a 1PPS sync output signal
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports AMI, PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262. ITU-T G.813 and ITU-T G.783 Recommendations

OTHER FEATURES

- Multiple microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola, I2C and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 100-pin TQFP package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipment
- Synchronous Ethernet equipment
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipment
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipment

DESCRIPTION

The IDT82V3391 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 3, Stratum 4E, Stratum 4, SMC, EEC-Option1, EEC-Option2 clocks in SONET / SDH / Synchronous Ethernet equipment, DWDM and Wireless base station.

The device supports several types of input clock sources: recovered clock from Synchronous Ethernet, STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

The device consists of T0 and T4 paths. The T0 path is a high quality and highly configurable path to provide system clock for node timing synchronization within a SONET / SDH / Synchronous Ethernet network. The T4 path is simpler and less configurable for equipment synchronization. The T4 path locks independently from the T0 path or locks to the T0 path.

An input clock is automatically or manually selected for T0 and T4 path. Both the T0 and T4 paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

There are 2 high performance APLLs that can be used for low jitter SONET and Ethernet Clocks

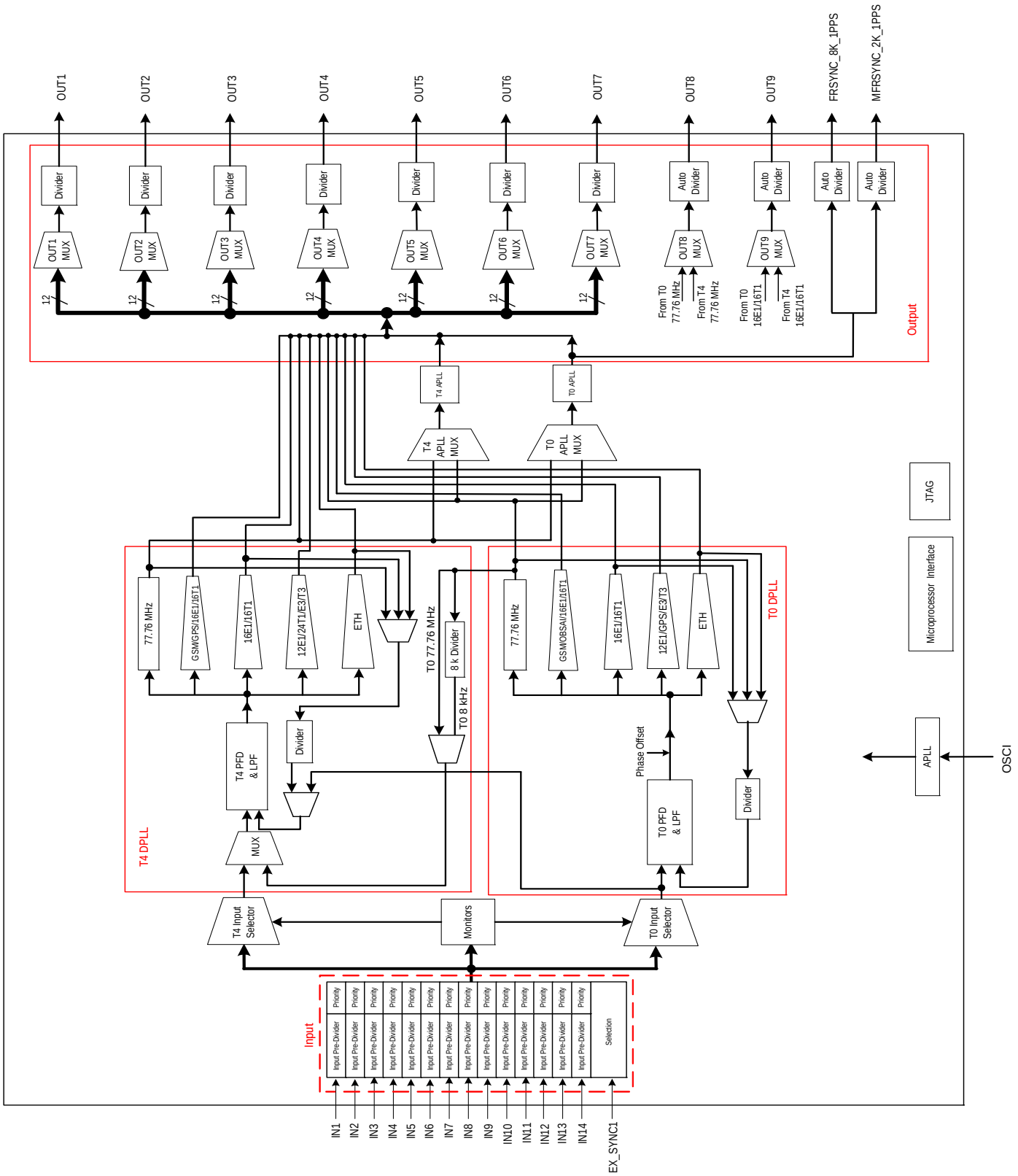
The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz in 19 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A highly stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

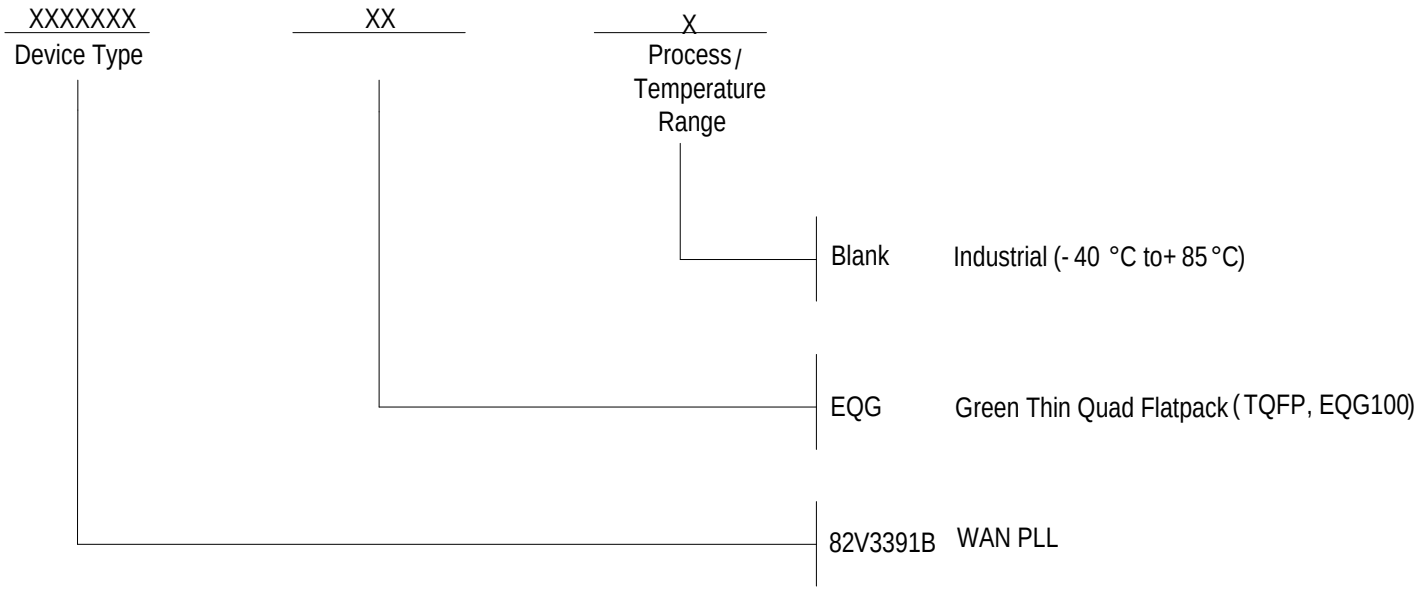
All the read/write registers are accessed through a microprocessor interface. The device supports six microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola, I2C and Serial.

In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION



We've Got Your Timing Solution

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056