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19-Output Differential Zbuffer for PCIe Gen2/3 and QPI

9ZX21901B

Description

The 9ZX21901 is a version of the Intel DB1900Z Differential Buffer with an adjustable external feedback path allowing the user to eliminate trace delays from their design. It is suitable for PCIe Gen3 or QPI applications. The part is backwards compatible to PCIe Gen1 and Gen2. The device maintains low drift for critical QPI applications. In bypass mode, the IDT9ZX21901 can provide outputs up to 400MHz.

Recommended Application

19 output PCIe Gen3/QPI buffer with adjustable feedback for Romley platforms

Output Features

- 19 - 0.7V current mode differential HCSL output pairs

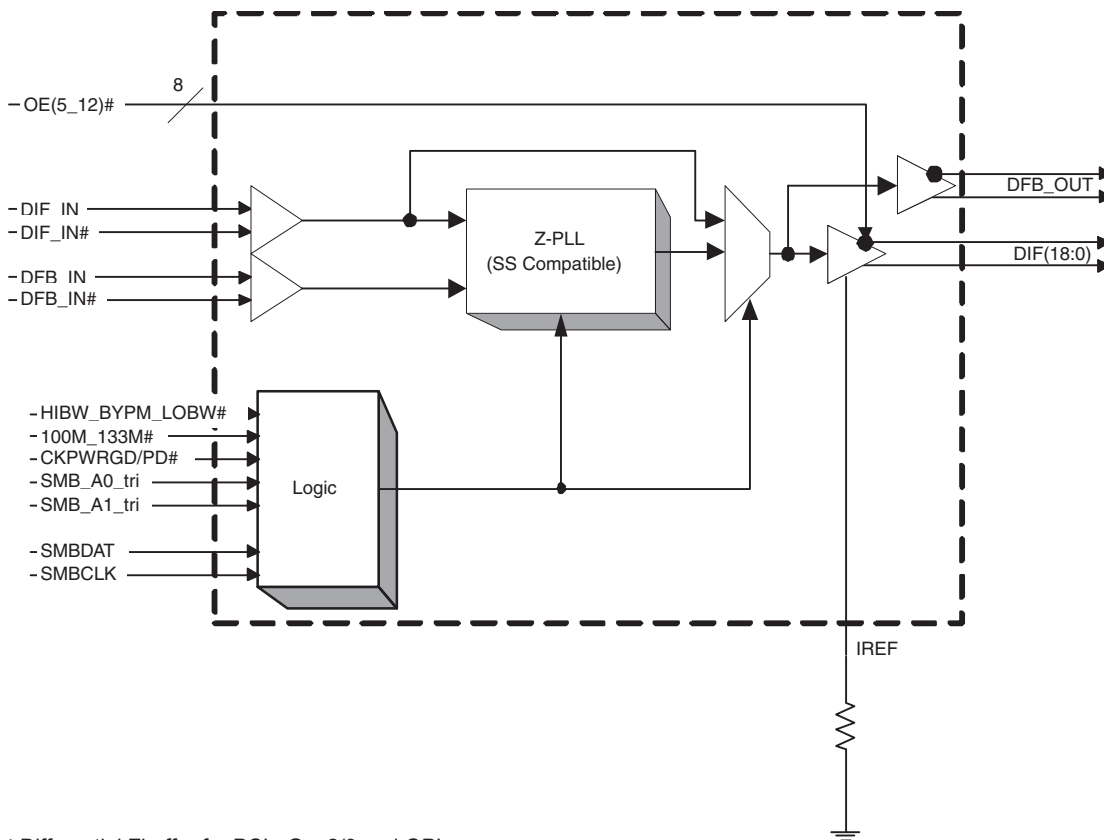
Features/Benefits

- External feedback path; Adjustable input-to-output delay
- 9 Selectable SMBus addresses/ Multiple devices can share same SMBus segment
- 8 dedicated OE# pins/ hardware control of outputs
- PLL or bypass mode/ PLL can dejitter incoming clock
- Selectable PLL BW/ minimizes jitter peaking in downstream PLL's
- Spread spectrum compatible/tracks spreading input clock for EMI reduction
- SMBus Interface/ unused outputs can be disabled
- 100MHz & 133.33MHz PLL mode/ Legacy QPI support
- Undriven differential outputs in Power Down mode for maximum power savings

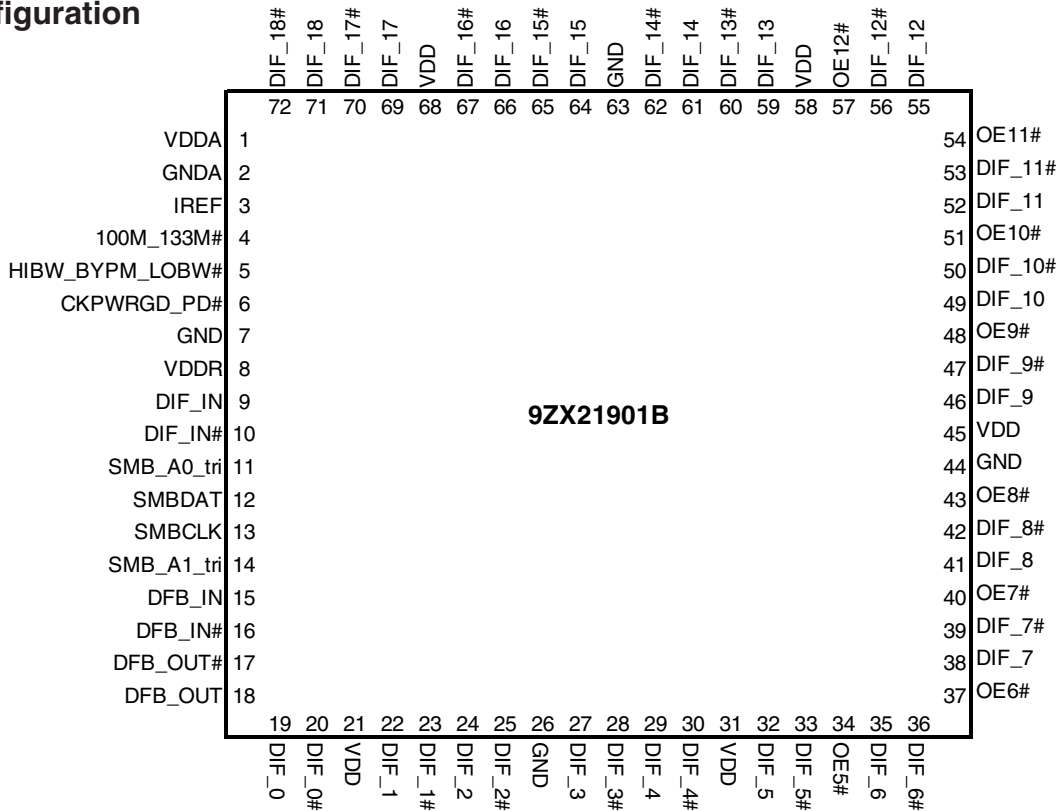
Key Specifications

- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: <65ps
- Input-to-output delay: User adjustable
- Input-to-output delay variation: <50ps
- Phase jitter: PCIe Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms

Functional Block Diagram



Pin Configuration



72-pin MLF

PLL Operating Mode Readback Table

| HiBW_BypM_LoBW# | Byte0, bit 7 | Byte 0, bit 6 |
|-----------------|--------------|---------------|
| Low (Low BW) | 0 | 0 |
| Mid (Bypass) | 0 | 1 |
| High (High BW) | 1 | 1 |

Functionality at Power Up (PLL Mode)

| 100M_133M# | DIF_IN (MHz) | DIF (MHz) |
|------------|--------------|-----------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

PLL Operating Mode

| HiBW_BypM_LoBW# | MODE |
|-----------------|-----------|
| Low | PLL Lo BW |
| Mid | Bypass |
| High | PLL Hi BW |

NOTE: PLL is OFF in Bypass Mode

Tri-level Input Thresholds

| Level | Voltage |
|-------|--------------|
| Low | <0.8V |
| Mid | 1.2<Vin<1.8V |
| High | Vin > 2.2V |

Power Connections

| Pin Number | | Description |
|--------------------|------------|--------------|
| VDD | GND | |
| 1 | 2 | Analog PLL |
| 8 | 7 | Analog Input |
| 21, 31, 45, 58, 68 | 26, 44, 63 | DIF clocks |

9ZX21901 SMBus Addressing

| Pin | | SMBus Address (Rd/Wrt bit = 0) |
|------------|------------|--------------------------------|
| SMB A1 tri | SMB A0 tri | |
| 0 | 0 | D8 |
| 0 | M | DA |
| 0 | 1 | DE |
| M | 0 | C2 |
| M | M | C4 |
| M | 1 | C6 |
| 1 | 0 | CA |
| 1 | M | CC |
| 1 | 1 | CE |

Pin Description

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|-----------------|----------|---|
| 1 | VDDA | PWR | 3.3V power for the PLL core. |
| 2 | GND A | PWR | Ground pin for the PLL core. |
| 3 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 4 | 100M_133M# | IN | Input to select operating frequency 1 = 100MHz, 0 = 133.33MHz |
| 5 | HIBW_BYPM_LOBW# | IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 6 | CKPWRGD_PD# | IN | Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 7 | GND | PWR | Ground pin. |
| 8 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 9 | DIF_IN | IN | 0.7 V Differential TRUE input |
| 10 | DIF_IN# | IN | 0.7 V Differential Complementary Input |
| 11 | SMB_A0_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses. |
| 12 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 13 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 14 | SMB_A1_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses. |
| 15 | DFB_IN | IN | True half of differential feedback input, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. |
| 16 | DFB_IN# | IN | Complementary half of differential feedback input, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. |
| 17 | DFB_OUT# | OUT | Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. |
| 18 | DFB_OUT | OUT | True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. |
| 19 | DIF_0 | OUT | 0.7V differential true clock output |
| 20 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 21 | VDD | PWR | Power supply, nominal 3.3V |
| 22 | DIF_1 | OUT | 0.7V differential true clock output |
| 23 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 24 | DIF_2 | OUT | 0.7V differential true clock output |
| 25 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 26 | GND | PWR | Ground pin. |
| 27 | DIF_3 | OUT | 0.7V differential true clock output |
| 28 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 29 | DIF_4 | OUT | 0.7V differential true clock output |
| 30 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 31 | VDD | PWR | Power supply, nominal 3.3V |
| 32 | DIF_5 | OUT | 0.7V differential true clock output |
| 33 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 34 | OE5# | IN | Active low input for enabling DIF pair 5. 1 =disable outputs, 0 = enable outputs |
| 35 | DIF_6 | OUT | 0.7V differential true clock output |
| 36 | DIF_6# | OUT | 0.7V differential Complementary clock output |

Pin Description (continued)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|--|
| 37 | OE6# | IN | Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs |
| 38 | DIF_7 | OUT | 0.7V differential true clock output |
| 39 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 40 | OE7# | IN | Active low input for enabling DIF pair 7. 1 =disable outputs, 0 = enable outputs |
| 41 | DIF_8 | OUT | 0.7V differential true clock output |
| 42 | DIF_8# | OUT | 0.7V differential Complementary clock output |
| 43 | OE8# | IN | Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs |
| 44 | GND | PWR | Ground pin. |
| 45 | VDD | PWR | Power supply, nominal 3.3V |
| 46 | DIF_9 | OUT | 0.7V differential true clock output |
| 47 | DIF_9# | OUT | 0.7V differential Complementary clock output |
| 48 | OE9# | IN | Active low input for enabling DIF pair 9. 1 =disable outputs, 0 = enable outputs |
| 49 | DIF_10 | OUT | 0.7V differential true clock output |
| 50 | DIF_10# | OUT | 0.7V differential Complementary clock output |
| 51 | OE10# | IN | Active low input for enabling DIF pair 10. 1 =disable outputs, 0 = enable outputs |
| 52 | DIF_11 | OUT | 0.7V differential true clock output |
| 53 | DIF_11# | OUT | 0.7V differential Complementary clock output |
| 54 | OE11# | IN | Active low input for enabling DIF pair 11. 1 =disable outputs, 0 = enable outputs |
| 55 | DIF_12 | OUT | 0.7V differential true clock output |
| 56 | DIF_12# | OUT | 0.7V differential Complementary clock output |
| 57 | OE12# | IN | Active low input for enabling DIF pair 12. 1 =disable outputs, 0 = enable outputs |
| 58 | VDD | PWR | Power supply, nominal 3.3V |
| 59 | DIF_13 | OUT | 0.7V differential true clock output |
| 60 | DIF_13# | OUT | 0.7V differential Complementary clock output |
| 61 | DIF_14 | OUT | 0.7V differential true clock output |
| 62 | DIF_14# | OUT | 0.7V differential Complementary clock output |
| 63 | GND | PWR | Ground pin. |
| 64 | DIF_15 | OUT | 0.7V differential true clock output |
| 65 | DIF_15# | OUT | 0.7V differential Complementary clock output |
| 66 | DIF_16 | OUT | 0.7V differential true clock output |
| 67 | DIF_16# | OUT | 0.7V differential Complementary clock output |
| 68 | VDD | PWR | Power supply, nominal 3.3V |
| 69 | DIF_17 | OUT | 0.7V differential true clock output |
| 70 | DIF_17# | OUT | 0.7V differential Complementary clock output |
| 71 | DIF_18 | OUT | 0.7V differential true clock output |
| 72 | DIF_18# | OUT | 0.7V differential Complementary clock output |

Electrical Characteristics - Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Case Temperature | T _c | | | | 110 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Parameters

T_A = T_{COM}, Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | 33 | | 400 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 100MHz PLL mode | 90 | 100.00 | 105 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 133.33MHz PLL mode | 120 | 133.33 | 140 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | | 12 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DD} SMB | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DD} SMB | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics - DIF_IN Clock Input Parameters

$T_{AMB}=T_{COM}$ unless otherwise indicated, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|-------------|--|-----|-----|-----|---------|-------|
| Input Crossover Voltage - DIF_IN | V_{CROSS} | Cross Over Voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V_{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}, V_{IN} = GND$ | -5 | | 5 | μA | |
| Input Duty Cycle | d_{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J_{DIFin} | Differential Measurement | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM}$, Supply Voltage $V_{DD}/V_{DDA} = 3.3 V \pm 5\%$, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------|--------------------|---|------|-----|------|-------|---------|
| Slew rate | dV/dt | Scope averaging on | 1 | 2.5 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | $\Delta dV/dt$ | Slew rate matching, Scope averaging on | | | 20 | % | 1, 2, 4 |
| Rise/Fall Time Matching | τ_{Trf} | Rise/fall matching, Scope averaging off | | | 125 | ps | 1, 7, 8 |
| Voltage High | V_{High} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 750 | 850 | mV | 1 |
| Voltage Low | V_{Low} | | -150 | | 150 | | 1 |
| Max Voltage | V_{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | | 1150 | mV | 1 |
| Min Voltage | V_{min} | | -300 | | | | 1 |
| Vswing | V_{swing} | Scope averaging off | 300 | | | mV | 1, 2 |
| Crossing Voltage (abs) | V_{cross_abs} | Scope averaging off | 250 | | 550 | mV | 1, 5 |
| Crossing Voltage (var) | ΔV_{cross} | Scope averaging off | | | 140 | mV | 1, 6 |

¹ Guaranteed by design and characterization, not 100% tested in production. $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32mA$.

$I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7V @ Z_O=50\Omega$ (100 Ω differential impedance).

² Measured from differential waveform

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of $V_{cross_min/max}$ (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting V_{cross_delta} to be smaller than V_{cross} absolute.

⁷ Measured from single-ended waveform

⁸ Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics - Current ConsumptionTA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-----------------------|---|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD3.3OP} | All outputs active @100MHz, C _L = Full load; | | 407 | 500 | mA | 1 |
| Powerdown Current | I _{DD3.3PDZ} | All differential pairs tri-stated | | 12 | 36 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.**Electrical Characteristics - Skew and Differential Jitter Parameters**TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|------|-------------|-----------|
| CLK_IN, DIF[x:0] | t _{SPO_PLL} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | -300 | -200 | -100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t _{PD_BYP} | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V | 2.5 | 3.5 | 4.5 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_PLL} | Input-to-Output Skew Variation in PLL mode across voltage and temperature | -50 | 0 | 50 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_BYP} | Input-to-Output Skew Variation in Bypass mode across voltage and temperature | -250 | | 250 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DTE} | Random Differential Tracking error between two 9ZX devices in Hi BW Mode | | 3 | 5 | ps (rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSSTE} | Random Differential Spread Spectrum Tracking error between two 9ZX devices in Hi BW Mode | | 15 | 75 | ps | 1,2,3,5,8 |
| DIF[x:0] | t _{SKREW_ALL} | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode) | | 45 | 65 | ps | 1,2,3,8 |
| PLL Jitter Peaking | j _{peak-hibw} | LOBW#_BYPASS_HIBW = 1 | 0 | 1 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | j _{peak-lobw} | LOBW#_BYPASS_HIBW = 0 | 0 | 1 | 2 | dB | 7,8 |
| PLL Bandwidth | p _{ll_HIBW} | LOBW#_BYPASS_HIBW = 1 | 2 | 3 | 4 | MHz | 8,9 |
| PLL Bandwidth | p _{ll_LOBW} | LOBW#_BYPASS_HIBW = 0 | 0.7 | 1 | 1.4 | MHz | 8,9 |
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 50 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially, Bypass Mode @100MHz | -2 | 0 | 2 | % | 1,10 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | PLL mode | | 24 | 50 | ps | 1,11 |
| | | Additive Jitter in Bypass Mode | | 20 | 50 | ps | 1,11 |

Notes for preceding table:¹ Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input. Feedback path is 695 mils long.² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.³ All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.⁴ This parameter is deterministic for a given device⁵ Measured with scope averaging on to find mean value. DIF_IN slew rate must be matched to DIF output slew rate.⁶ t is the period of the input clock⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.⁸ Guaranteed by design and characterization, not 100% tested in production.⁹ Measured at 3 db down or half power point.¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.¹¹ Measured from differential waveform

Electrical Characteristics - Phase Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------------|-------------------------|--|-----|------|-----|----------|---------|
| Jitter, Phase | t _{jphPCIeG1} | PCIe Gen 1 | | 36 | 86 | ps (p-p) | 1,2,3 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1.2 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 1.9 | 3.1 | ps (rms) | 1,2 |
| | t _{jphPCIeG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.5 | 1 | ps (rms) | 1,2,4 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.31 | 0.5 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.21 | 0.3 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.17 | 0.2 | ps (rms) | 1,5 |
| Additive Phase Jitter, Bypass mode | t _{jphPCIeG1} | PCIe Gen 1 | | 4 | 10 | ps (p-p) | 1,2,3 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.25 | 0.3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.57 | 0.7 | ps (rms) | 1,2,6 |
| | t _{jphPCIeG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.20 | 0.3 | ps (rms) | 1,2,4,6 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.22 | 0.3 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.08 | 0.1 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.08 | 0.1 | ps (rms) | 1,5,6 |

¹ Applies to all outputs.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

⁶ For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)² = (total jitter)² - (input jitter)²

Clock Periods - Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2,3 |
| | 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns | 1,2,4 |

Clock Periods - Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2,4 |

Notes:

- ¹Guaranteed by design and characterization, not 100% tested in production.
- ²All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZX21901 itself does not contribute to ppm error.
- ³Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode
- ⁴Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Power Management Table

| Inputs | | Control Bits/Pins | | | | Outputs | PLL State |
|-------------|-----------------|-------------------|---------|-----------------------|-------------------|-------------------|-----------|
| CKPWRGD_PD# | DIF_IN/ DIF_IN# | SMBus EN bit | OE# Pin | DIF(5:12)/ DIF(5:12)# | Other DIF/ DIF# | DFB_OUT/ DFB_OUT# | |
| 0 | X | X | X | Hi-Z ¹ | Hi-Z ¹ | Hi-Z ¹ | OFF |
| 1 | Running | 0 | X | Hi-Z ¹ | Hi-Z ¹ | Running | ON |
| | | 1 | 0 | Running | Running | Running | ON |
| | | 1 | 1 | Hi-Z ¹ | Running | Running | ON |

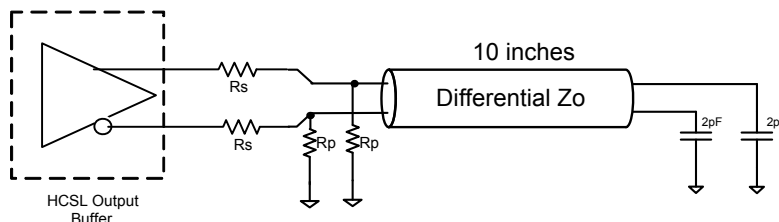
NOTE:

- 1. Due to external pull down resistors, HI-Z results in Low/Low on the True/Complement outputs

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|--------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θJA | Still air | | 26.2 | | °C/W |
| | θJA | 1 m/s air flow | | 23.1 | | °C/W |
| | θJA | 3 m/s air flow | | 19.6 | | °C/W |
| Thermal Resistance Junction to Case | θJC | | | 10.4 | | °C/W |
| Thermal Resistance Junction to Board | θJB | | | 0.3 | | °C/W |

9ZX21901 Differential Test Loads



Differential Output Termination Table

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω) |
|------------|----------|--------|--------------|
| 100 | 475 | 33 | 50 |
| 85 | 412 | 27 | 42.2 or 43.2 |

General SMBus serial interface information for the 9ZX21901B (See also 9ZX21901 SMBus Addressing on page 2)

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $XX_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $XX_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $YY_{(H)}$
- IDT clock will **acknowledge**
- vclock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address $XX_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | X Byte | |
| ◇ | | ACK |
| ◇ | | ◇ |
| ◇ | | ◇ |
| Byte N + X - 1 | | ◇ |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address $XX_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address $YY_{(H)}$ | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | |
| | | Beginning Byte N |
| ACK | | |
| ◇ | | ◇ |
| ◇ | | ◇ |
| ◇ | | ◇ |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

Note: $XX_{(H)}$ is defined by SMBus address select pins

SMBusTable: PLL Mode, and Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------------|----------------------------------|------|---------------------------------------|--------|---------|
| Bit 7 | 5 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode Readback Table | | Latch |
| Bit 6 | 5 | PLL Mode 0 | PLL Operating Mode Rd back 0 | R | | | Latch |
| Bit 5 | 72/71 | DIF_18_En | Output Control overrides OE# pin | RW | Hi-Z | Enable | 1 |
| Bit 4 | 70/69 | DIF_17_En | Output Control overrides OE# pin | RW | Hi-Z | Enable | 1 |
| Bit 3 | 67/66 | DIF_16_En | Output Control overrides OE# pin | RW | Hi-Z | Enable | 1 |
| Bit 2 | | Reserved | | | | | 0 |
| Bit 1 | | Reserved | | | | | 0 |
| Bit 0 | 4 | 100M_133M# | Frequency Select Readback | R | 133MHz | 100MHz | Latch |

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|----------------------------------|------|------|--------|---------|
| Bit 7 | 39/38 | DIF_7_En | Output Control overrides OE# pin | RW | Hi-Z | Enable | 1 |
| Bit 6 | 35/36 | DIF_6_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 5 | 32/33 | DIF_5_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | 29/30 | DIF_4_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | 27/28 | DIF_3_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 2 | 24/25 | DIF_2_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | 22/23 | DIF_1_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | 19/20 | DIF_0_En | Output Control overrides OE# pin | RW | | | 1 |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------|----------------------------------|------|------|--------|---------|
| Bit 7 | 65/64 | DIF_15_En | Output Control overrides OE# pin | RW | Hi-Z | Enable | 1 |
| Bit 6 | 62/61 | DIF_14_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 5 | 60/59 | DIF_13_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | 56/55 | DIF_12_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | 53/52 | DIF_11_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 2 | 50/49 | DIF_10_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | 47/46 | DIF_9_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | 42/41 | DIF_8_En | Output Control overrides OE# pin | RW | | | 1 |

SMBusTable: Output Enable Pin Status Readback Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|---------|-----------------------------|------|-------------|--------------|-----------|
| Bit 7 | 57 | OE_RB12 | Real Time readback of OE#12 | R | OE# pin Low | OE# Pin High | Real time |
| Bit 6 | 54 | OE_RB11 | Real Time readback of OE#11 | R | | | Real time |
| Bit 5 | 51 | OE_RB10 | Real Time readback of OE#10 | R | | | Real time |
| Bit 4 | 48 | OE_RB9 | Real Time readback of OE#9 | R | | | Real time |
| Bit 3 | 43 | OE_RB8 | Real Time readback of OE#8 | R | | | Real time |
| Bit 2 | 40 | OE_RB7 | Real Time readback of OE#7 | R | | | Real time |
| Bit 1 | 37 | OE_RB6 | Real Time readback of OE#6 | R | | | Real time |
| Bit 0 | 34 | OE_RB5 | Real Time readback of OE#5 | R | | | Real time |

SMBusTable: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Vendor & Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|------------------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | B rev = 0001 C Rev = 0010 | | X |
| Bit 6 | - | RID2 | | R | | | X |
| Bit 5 | - | RID1 | | R | | | X |
| Bit 4 | - | RID0 | | R | | | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-------------------|------|--|---|---------|
| Bit 7 | - | | Device ID 7 (MSB) | R | Device ID is 219 decimal or DB hex. | | 1 |
| Bit 6 | - | | Device ID 6 | R | | | 1 |
| Bit 5 | - | | Device ID 5 | R | | | 0 |
| Bit 4 | - | | Device ID 4 | R | | | 1 |
| Bit 3 | - | | Device ID 3 | R | | | 1 |
| Bit 2 | - | | Device ID 2 | R | | | 0 |
| Bit 1 | - | | Device ID 1 | R | | | 1 |
| Bit 0 | - | | Device ID 0 | R | | | 1 |

SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|--|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

SMBusTable: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

| DIF Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing

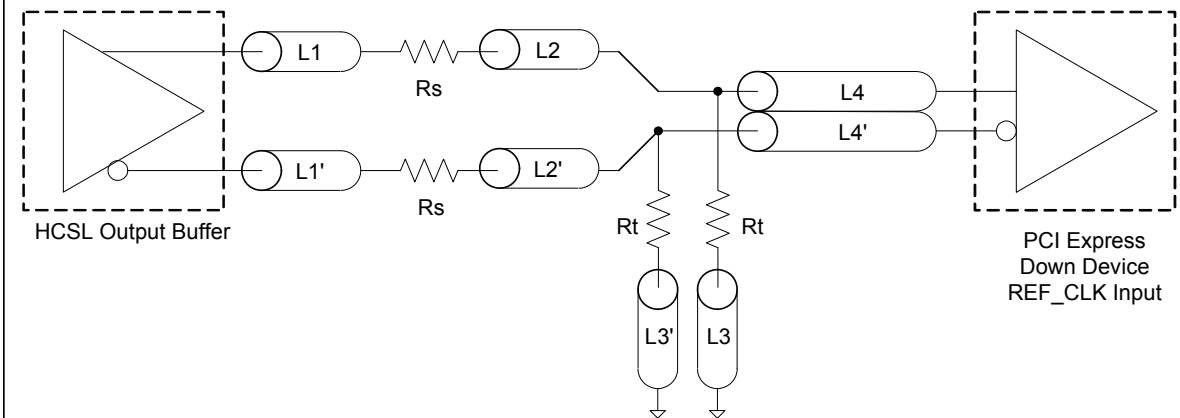
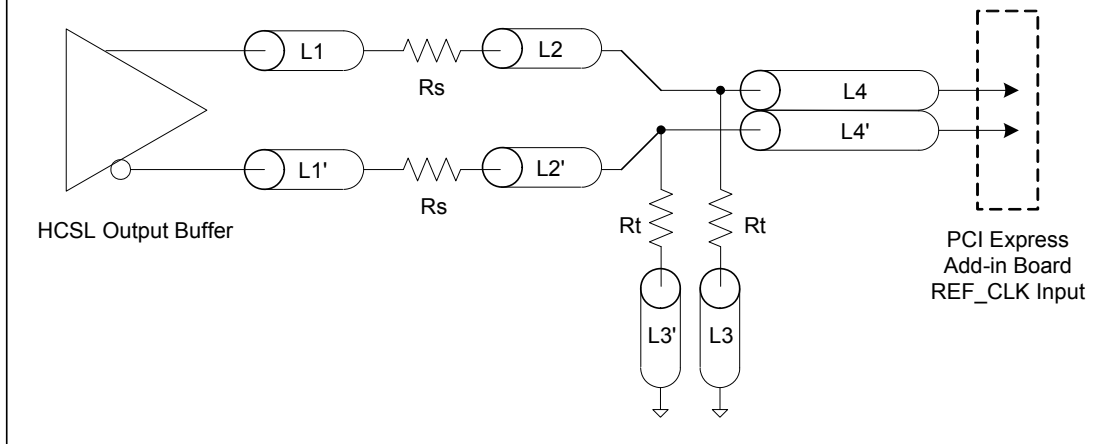


Figure 2: PCI Express Connector Routing



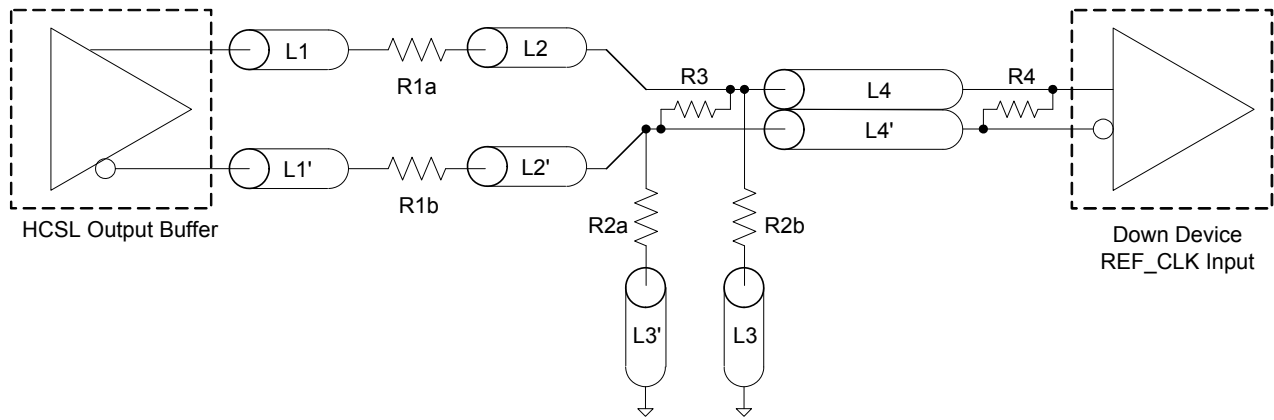
Alternative Termination for LVDS and other Common Differential Signals (figure 3)

| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
|-------|-------|------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

R2a = R2b = R2

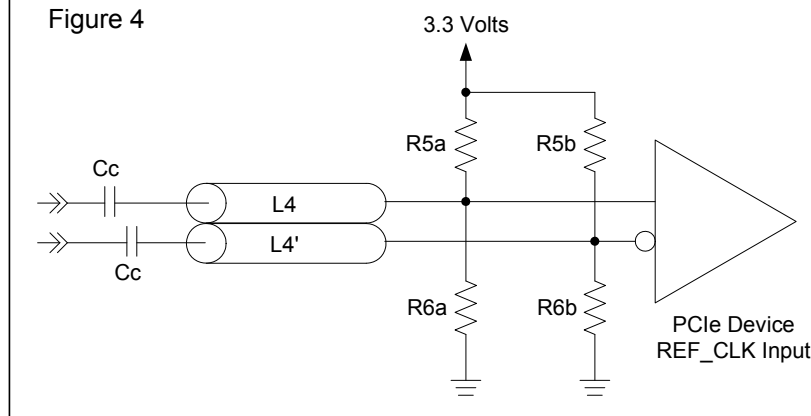
Figure 3



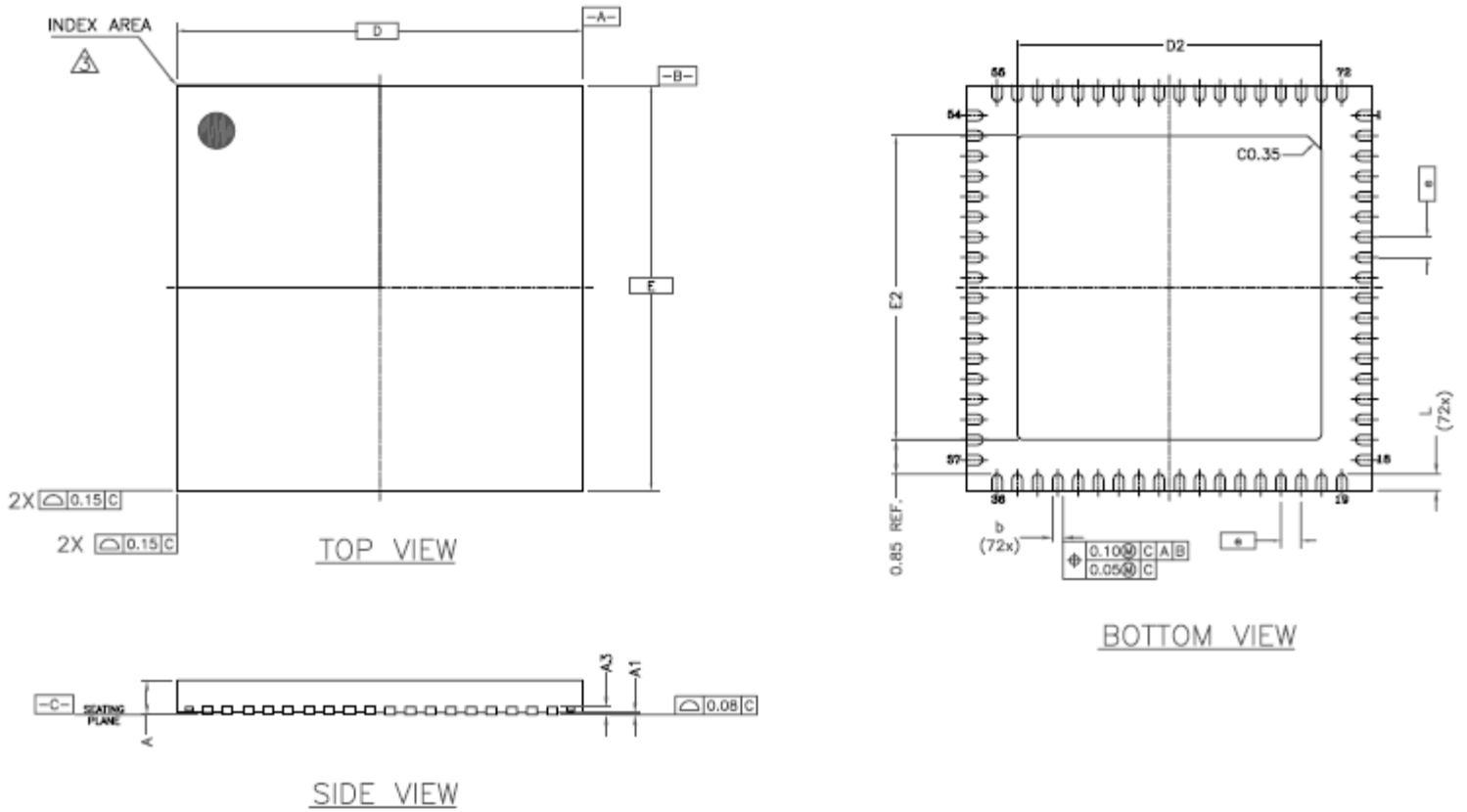
Cable Connected AC Coupled Application (figure 4)

| Component | Value | Note |
|-----------|-------------|------|
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |

Figure 4

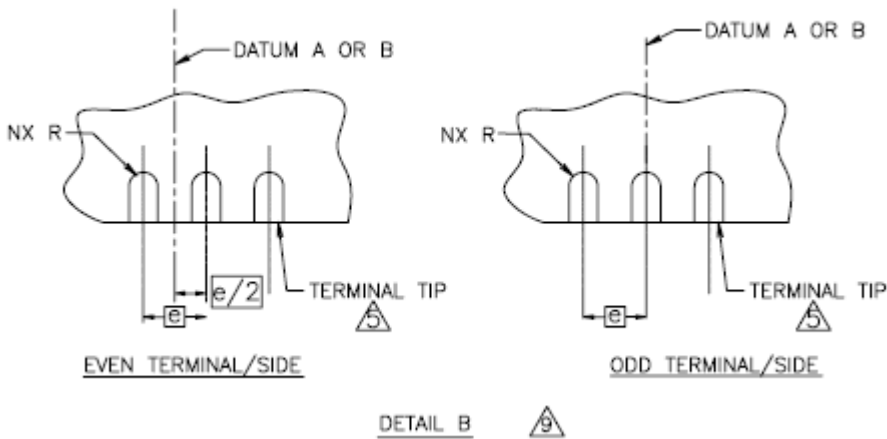


NL72 Package Drawing and Dimensions

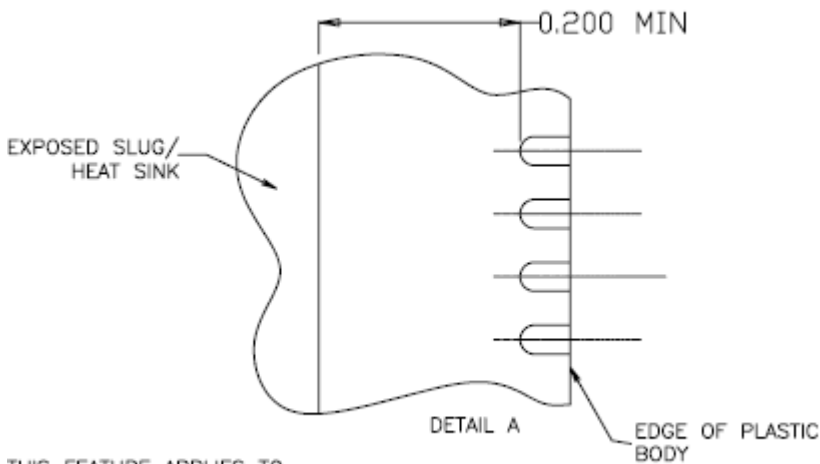


NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)



NL72 Package Drawing and Dimensions (cont.)



THIS FEATURE APPLIES TO ALL ENDS OF THE PKG.

| COMMON DIMENSIONS | | | |
|-------------------|-----------|----------|------|
| DIM SYMBOL | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 REF | — | 0.20 ref | — |
| Ø | 0 | — | 14 |
| T ref. | — | 0.45 | — |
| R1 | — | 0.20 | — |
| R ref, b min/2 | | | |
| NOTES | | | |
| b | 0.18 | 0.25 | 0.30 |
| ⊕ | 0.50 BSC | | |
| d | 10.00 BSC | | |
| E | 10.00 BSC | | |

| SYMBOL | DIMENSION | | | NOTE |
|--------|-----------------|------|------|------|
| | MIN. | NOM. | MAX. | |
| D2 | SEE EPAD OPTION | | | |
| E2 | SEE EPAD OPTION | | | |
| k | 0.20 | — | — | |
| N | | 72 | | 6 |
| Nd | | 18 | | 6 |
| Ne | | 18 | | 6 |

EPAD OPTION:

| SYMBOL | P3 | | |
|--------|------|------|------|
| | MIN. | NOM. | MAX. |
| E2 | 5.80 | 5.90 | 6.00 |
| D2 | 5.80 | 5.90 | 6.00 |

| TOLERANCE OF FORM & POSITION | | |
|------------------------------|--------|--------|
| SYMBOL | pitch | |
| | 0.40mm | 0.50mm |
| aaa | 0.10 | 0.15 |
| bbb | 0.07 | 0.10 |
| ccc | 0.10 | 0.10 |
| ddd | 0.05 | 0.05 |
| NOTES | | |
| 1,2 | | |

LEAD OPTION

| SYMBOL | Z2 | | |
|--------|------|------|------|
| | MIN. | NOM. | MAX. |
| L | 0.30 | 0.40 | 0.50 |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUB. 95 SEC. 4.3 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

Ordering Information

| Part / Order Number | Shipping Package | Package | Temperature |
|---------------------|------------------|------------|-------------|
| 9ZX21901BKLF | Trays | 72-pin MLF | 0 to +70°C |
| 9ZX21901BKLFT | Tape and Reel | 72-pin MLF | 0 to +70°C |

"LF" designates PB-free configuration, RoHS compliant.

Revision History

| Rev. | Issue Date | Who | Description | Page # |
|------|------------|-----|---|------------|
| A | 5/13/2009 | RDW | 1. Slightly modified name of pin 6 and corrected pin description of pin 6, to remove reference to CK505 2. Added Typical numbers to key parameters in electrical characteristics tables. 3. Move to final. | Various |
| B | 8/7/2009 | RDW | 1. Updated Pin 8 name to VDDR to indicate that it is the VDD for the input receiver. 2. Change MAX operating current from 600 to 500mA. | Various |
| C | 8/12/2009 | RDW | 1. Updated VDDR pin description to include 3.3V information. | Various |
| D | 8/14/2009 | RDW | 1. Inserted Pins 19 and 72 into pinout after they were inadvertently removed. | 2 |
| E | 10/7/2009 | RDW | 1. Corrected units from ns to ps for the tDSPO_PLL and tDSPO_BYP parameters | |
| F | 6/22/2010 | RDW | 1. Updated QPI reference to 9.6GTs, added note about variable feedback path 2. Reformatted electrical tables to fit new standard format 3. Merged Phase Jitter Tables into Single Table. 4. Added output termination/test load drawing and table | 1, 5, 6, 9 |
| G | 8/3/2010 | RDW | 1. Updated front page to standard 9ZX format. 2. Clarified that SMBus Address Selection table includes the Read/Write Bit. Minor clarifications to other tables. 3. Added additive phase jitter table for bypass mode. | 1-3, 5-11 |
| H | 3/2/2011 | RDW | 1. Added rise/fall variation spec to HCSL_Out table | 6 |
| J | 12/8/2011 | RDW | 1. Updated tDSPO_BYP parameter from +/-350 to +/-250ps. | 7 |
| K | 4/12/2012 | RDW | 1. Updated Rp values on Output Terminations Table from 43.2 ohms to 42.2 or 43.2 ohms to be consistent with Intel. | 9 |
| L | 12/17/2012 | RG | 1. Updated Abs Max table to include Case Temperature at 110 °C max. 2. Added Thermal Characteristics table | 5, 9 |
| M | 4/15/2013 | RDW | 1. Corrected typo in OE# Latency parameter; changed 1 min. to 3 max. cycles to 4 min. to 12 max. clocks. | 5 |
| N | 1/7/2015 | DC | Updated package drawing and dimensions from PUNCH to SAWN | Various |
| P | 11/19/2015 | RDW | Update Input Clock spec with new standardized table matching PCIe SIG input specs. | 5 |

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For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

408-284-6578
pcclockhelp@idt.com

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

