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# () IDT.

## DATASHEET

## 12-OUTPUT DIFFERENTIAL Z-BUFFER FOR PCIE GEN3 AND QPI

## 9ZX21200

## Description

The 9ZX21200 is a small-footprint 12-output differential buffer that meets all the performance requirements of the Intel DB1200Z specification. The 9ZX21200 is backwards compatible to PCIe Gen1 and Gen2 applications. A fixed, internal feedback path maintains low drift for critical QPI applications. In bypass mode, the 9ZX21200 can provide outputs up to 150MHz.

## **Recommended Application**

12-output PCIe Gen3/ QPI differential buffer for Romley and newer platforms

## **Key Specifications**

- Cycle-to-cycle jitter <50ps
- Output-to-output skew < 65 ps
- Input-to-output delay variation <50ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- QPI 9.6GT/s 12UI phase jitter < 0.2ps RMS

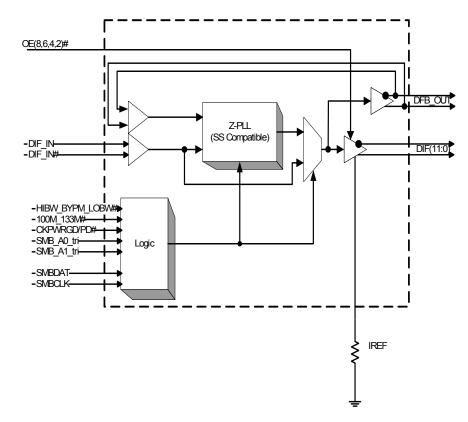
## Features/Benefits

- Space-saving 56-pin package
- · Fixed feedback path for 0ps input-to-output delay
- 9 Selectable SMBus Addresses; Mulitple devices can share the same SMBus Segment
- 4 OE# pins; Hardware control of four outputs
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz or 133MHz PLL mode operation; supports PCIe and QPI applications
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible; tracks spreading input clock for low EMI
- Software control of PLL Bandwidth and Bypass Settings/PLL can dejitter incoming clock (B Rev only)

## **Output Features**

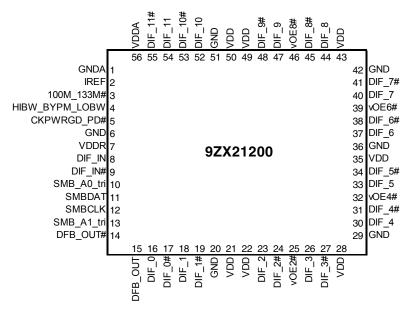
• 12 - 0.7V differential HCSL output pairs

## **Block Diagram**



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## **Pin Configuration**



Notes: Pins with ^ prefix have internal 120K pullup

Pins with v prefix have internal 120K pulldown. Even though the feedback path is fixed, the DFB\_OUT pair still needs a termination network for the part to function.

#### **Power Management Table**

CKPWRGD_PD#	DIF_IN/ DIF_IN#	SMBus EN bit	DIF(11:0)/ DIF(11:0)#	PLL STATE IF NOT IN BYPASS MODE
0	Х	Х	Low/Low	OFF
1	Running	0	Low/Low	ON
1	nunning	1	Running	ON

#### **MLF Power Connections**

	Pin Number	r	<b>.</b>
VDD	VDD	GND	Description
56		1	Analog PLL
7		6	Analog Input
21,35,50	22,28,43,49	20,29,36,42, 51	DIF clocks

#### Functionality at Power-up (PLL mode)

100M_133M#	DIF_IN MHz	DIF(11:0)
1	100.00	DIF_IN
0	1 33.33	DIF_IN

#### PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

#### PLL Operating Mode Table

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW
NOTE: DLL in OFF in By	naca Mada

NOTE: PLL is OFF in Bypass Mode

#### **Tri-Level Input Thresholds**

Level	Voltage
Low	<0.8V
Mid	1.2 <vin<1.8v< th=""></vin<1.8v<>
High	Vin > 2.2V

#### 9ZX21200 SMBus Addressing

Pi	Pin				
SMB_A1_tri	SMB_A0_tri	SMBus Address			
0	0	D8			
0	М	DA			
0	1	DE			
М	0	C2			
М	М	C4			
М	1	C6			
1	0	CA			
1	М	CC			
1	1	CE			

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9ZX21200

## **Pin Descriptions**

2   IREF   OUT   resistor to ground. 4750hm is the standard value for 1000hm differential impedance. Other impedances require different values. See data sheet.     3   100M_133M#   IN   3.3V Input to select operating frequency See Functionality Table for Definition     4   HIBW_BYPM_LOBW#   IN   Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.     5   CKPWRGD_PD#   IN   Trilevel input to select not analy and the probability. See PLL Operating Mode Table for Details.     6   GND   PWR   Ground pin.     7   VDDR   PWR   Ground pin.     8   DIF_IN   IN   0.7 V Differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.     8   DIF_IN   IN   0.7 V Differential TRUE input     9   DIF_IN#   IN   0.7 V Differential Complementary Input     10   SMB_A0_tri   IN   SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus addresses.     11   SMBDAT   I/O   Data pin of SMBUS circuitry, 5V tolerant     12   SMBLA   IN   Clock pin of SMBUS circuitry, 5V tolerant     13   SMB_A1_tri   IN	PIN #	PIN NAME	TYPE	DESCRIPTION
P     REF     OUT     resistor to ground 4750m is the standard value for 100chm differential impedance. Other impedances require different values. See data sheet.       3     10M_133M#     N     3.47 Imput to select dop and prequency see for the post to select Hot Table for Definition and start up on first hot senset.       6     INEW_SPFM_LOBW#     IN     Tribuel imput to select Hot Table for Definition and start up on first hot senset.       7     VDDR     PM     Northe advices to we start Power Down Mode.       8     INE IM     IN     0.77 Imput and the table and start up on first hot senset.       8     INE IM     IN     0.77 Imput and the advices and table and start up on first hot senset.       8     INE IM     IN     0.77 Imput and table and start up on first hot senset.       8     INE IM     IN     0.77 Imput and table and start to table and start up the advice in conjunction with the SMB_AD to decode 1 of 9       10     SMB_AD_1 fm     SMBus addresses     This is in the start end provides incedback signal to the PLL for synchronization with the information and start up addresses.       11     SMBus addresses     The start and start and start up addresses.     The start addresses.       12 </td <td>1</td> <td>GNDA</td> <td>PWR</td> <td></td>	1	GNDA	PWR	
3     3.3 <sup>1</sup> Input to select High Englands       4     Hisky_BYPM_LOBW/     N       5     CKPWRGD_PDe     N       6     BND     PWR       7     VDDR     PWR       8     DRID     PWR       8     DRID     PWR       9     DRIN     Notifies device to sample latched input and start up on first high assertion, or exit Power Down Mode       6     GND     PWR     337 byower for differential ruput dock (receiver). This VDD should be treated as an analog power rail and fillered appropriately.       8     DFL IN     IN     0.7 V Dfferential TRUE input       9     DFL IN     IN     0.7 V Dfferential Complementary input       10     SMB_AD_Ltri     IN     SMBus Addresses.       11     SMBDAT     IO     Data prior SMBUS Scrutzly, SV betrant       12     SMBLAL     IN     SMBus Addresses.       13     SMBLAL     IN     MBus Addresses.     INT intour addresses.       14     DFE_OUT     OUT     Complementary bit of differential feedback cuput, provides feedback signal to the PLL for synchronization with the in the into in conjunction with the SMB_AD to d	2	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances
3     100, TSSMP     11     See Functionally Table for Definition       4     HBW_BYPM_LOBW#     IT     See Functionally Table for Details.       5     CKPWRGD_PW     IN     Trilvevil nput to seeled High BW, Bypass or Low BW mode.       6     GND     PVM     Save power to stable accel house and statu up on first high assertion, or exit Power Down Mode.       6     GND     PVM     Save power to stable accel house and statu up on first high assertion, or exit Power Down Mode.       7     VDDR     PVM     Save power to stable accel house and statu up on first high assertion, or exit Power Down Mode.       8     DIF IM     IN     0.7.V Differential Complementary Input       9     DIF IM     IN     0.7.V Differential Complementary Input       10     SMBLs Address accels     This is a finite with and statu in conjunction with the SMB_AI to decode 1 of 9       11     SMBLs Address acceles     This is a finite with accel to align at a statu and SMBLs address accel input the works in conjunction with the SMB_AI to decode 1 of 9       13     SMBLs Address acceles     This is a finite with acceles to align.       14     OFB_OUT     OUT     OUT     This is a finite with acceles to align.       15				require different values. See data sheet.
4     HIBM_BYPH_LOBUM     IN     Thiskel input to select High BW, Stypess or Low BW mode.       5     CKPWRGD_PDB     IN     Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Made on subsequent assertions. Low end set server Down Mode.       6     GND     PWR     Graund pm.     3.07 power on the minital input clock (receiver). This VDD should be treated as an analog power rail and 3.07 power on the minital input clock (receiver). This VDD should be treated as an analog power rail and 3.07 power on the minital complementary input.       8     DIF. IN     IN     0.72 VDIfferential Complementary input.       10     SMB_Ad_Lin     IN     0.72 VDIfferential Complementary input.       11     SMBDAT     IO     Data pin of SMBUS contury. SV bierant       12     SMBLAL     IN     Clock pin of SMBUS contury. SV bierant       13     SMBLA     IN     SMBUS Addresses on differential feedback cuput, provides feedback signal to the PLL for synchronization with the in final dock to gliminate phase error.       13     SMBLA     OU     OV     The final ddfffferential feedback cuput, provides feedback signal to the PLL for synchronization to clock to gliminate phase error.       14     DFE_10     OU     OV differential Complementary dock output       15	3	100M_133M#	IN	
4     No. By Public LOwer     NN     See PLL Operating Mode <sup>7</sup> table for Details.       5     CKPWRGD_PDF     NN     Notifies device to sample lathed inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.       7     VDDR     PWR     3.7 brown for differential input dock (receiver). This VDD should be treated as an analog power rail and faitered appropriately.       8     DIF_IN     NN     0.7 V Differential TRUE input.       9     DIF_IN     NN     0.7 V Differential TRUE input.       10     SMB_A_0_rti     NN     SMBUS and dressee.       11     SMBCLK     NN     Condumtry Studies and therein input thore when so conjunction with the SMB_AI to decode 1 of 9       SMB_A1_rti     NN     SMBUS and dressee.     Componentary half of differential feedback output, provides feedback signal to the PLL for synchronization with the Intig dock to efficiential beback output, provides feedback signal to the PLL for synchronization with the Intig dock to efficiential beback output.       10     DFE_0     OUT     OUT differential feedback output, provides feedback signal to the PLL for synchronization with the Intig dock output.       10     DFE_1     OUT     OV differential bree dock output.       10     DFE_1     OUT <td< td=""><td></td><td>_</td><td></td><td></td></td<>		_		
5     CAPWR0L_PUP     IN     subsequent asertions. Low enters Power Down Mode.       6     RND     PVM     3/X power for differential input dock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.       8     DIF IN     IN     0.7.V Differential TRUE input       9     DIF IN     IN     0.7.V Differential Complementary Input       10     SMB_AD_th     IN     SMBUs Addresses.       11     SMBDAT     IO     Data info SMBUS Addresses.       12     SMBLAL     IN     Clock pt of SMBUS Addresses.       13     SMBLA     IN     Clock pt of SMBUS Addresses.       14     DFB_OUT#     OUT     SMBUS Addresses.       15     DFB_OUT#     OUT     SMBUS Addresses.       16     DFB_OUT#     OUT     Complementary facto differential feedback cuput, provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.       17     DFB_OUT     OUT     C/V differential Complementary dock output       18     DFT_1     OUT     C/V differential Complementary dock output       19     DFT_1     OUT     C/V differential Complementa	4	HIBW_BYPM_LOBW#	IN	See PLL Operating Mode Table for Details.
6     NDD     PWR     Ground pin.       7     VDDR     PWR     3/X power for differential input dock (receiver). The VDD should be treated as an analog power rail and fittered appropriately.       9     DFI IN     IN     0.7 V Differential Complementary Input.       9     DFI INF     IN     0.7 V Differential Complementary Input.       11     SMB.addresses.     IN     SMB.addresses.       12     SMB.dx Addresses.     IN     SMB.addresses.       13     SMB.A.t.ri     IN     SMB.addresses.       14     DFB_OUT#     OUT     SMB.addresses.       15     DFB_OUT#     OUT     True hail of differential feedback output, provides feedback signal to the PLL for synchronization with height addresses.       16     DFB_OUT     OUT     True hail of differential feedback output, provides feedback signal to the PLL for synchronization with neight addresses.       17     DFB_0     OUT     True hail of differential feedback output.       18     DF1_1     OUT     True hail of differential reserver.       19     DF1_2     OUT     True field of differential reserver.       20     DF2_2     OUT	5	CKPWRGD_PD#	IN	
7     VDDR     PWR Hared appropriately.     3.39 power for differential imput dock (receiver). This VDD should be treated as an analog power rail and Hared appropriately.       8     DIF IN     IN     0.7 U Differential Complementary Input       10     SMB_AO_Iri     IN     0.7 U Differential Complementary Input       10     SMB_AO_Iri     IN     SMBUS documentary Input that works in conjunction with the SMB_A1 to decode 1 of 9       11     SMBDAT     IO     Data pin of SMBUS documentary, EV tolerant       12     SMBCLACH     IN     Cock pin of SMBUS documentary, EV tolerant       13     SMBD_A1_tri     IN     SMBUS Addresses.     Contrained the second tolerant and tolerant a	6	GND	PWR	
B     DIF. IN     IN     D.7.V Differential Complementary Input       9     DIF. IN     IN     0.7.V Differential Complementary Input       10     SMB_AO_tri     IN     SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9       11     SMBDAT     IO     Data pin of SMBUS occurry, SV tolerant       12     SMBLAT_tri     IN     Clock pin of SMBUS occurry, SV tolerant       13     SMBLAT_tri     IN     SMBUS Address bit. This is a tri-level input that works in conjunction with the SMB_AD decode 1 of 9       14     OFB_OUT#     OUT     True half of differential free dack adjuct, provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.       16     DIF_0     OUT     OV     True that of differential free dock output     Provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.       16     DIF_1     OUT     OV differential True dock output     Provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.       17     DIF_6     OUT     0.7V differential True dock output     Provides feedback signal to the PLL for synchronization with the in clock output       10     DIF_6				3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and
9     DIF NM     IN     0.7.0 Differential Complementary Input       10     SMB_ Ad_Lin     IN     SMB us Addresses.       11     SMBDCIX     IN     SMBUS dicates bit. This is a threwin input that works in conjunction with the SMB_A1 to decode 1 of 9       12     SMBCIX     IN     Clock pin of SMBUS circuitry, SV tolerant       13     SMB_A1_tri     IN     SMBUS dicates bit. This is a triveel input that works in conjunction with the SMB_A0 to decode 1 of 9       14     DFB_OUT#     OUT     True half of differential leedback output, provides feedback signal to the PLL for synchronization with the in       15     DFB_OUT#     OUT     Complementary lead ock output       17     DFF 0     OUT     Covid differential leedback output       18     DFF 0     OUT     Covid differential leedback output       19     DFF 0     OUT     Covid differential leedback output       19     DFF 0     OUT     Covid differential leedback output       20     NDD     PVMF     Prover supply, nominal 3.3V       21     NDD     PVMF     Prover supply, nominal 3.3V       22     NDF 2     OUT     7.V di	0		INI	
NBE_A0_th   IN   SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9     11   SMBDAT   I/O   Data pin of SMBUS circuity, SV lolerant     12   SMBLA   I/N   Clock pin of SMBUS circuity, SV lolerant     13   SMB_A1_th   I/N   SMBUS address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9     14   DFB_OUT#   Out   Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.     15   DFB_OUT   Out   Ture half of differential free dock output   provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.     16   DFF_0   Out   0.7V differential Complementary dock output   1000000000000000000000000000000000000	-			
INSERTION     IN     SMBus Addresses.       10     SMBCLK     IN     Obox prior of SMBUS circuity. SV loterant       12     SMBCLK     IN     Clock prior of SMBUS circuity. SV loterant       13     SMBL AL_tri     IN     Clock prior of SMBUS circuity. SV loterant       14     DFB_OUT#     SMBLs Addresses.     Complementary haif of differential feedback output, provides feedback signal to the PLL for synchronization       15     DFB_OUT     OUT     True haif of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.       16     DIF_0     OUT     0.7V differential true clock output       17     DIF 1     OUT     0.7V differential true clock output       18     DIF_1     OUT     0.7V differential true clock output       19     DIF 2     OUT     0.7V differential Complementary dock output       20     VDD     PWR     Power supply, nominal 3.3V       21     VDD     PWR     Power supply, nominal 3.3V       22     VDD     PVR     Power supply, nominal 3.3V       23     DIF 2     OUT     0.7V differential Complementar			1	
12 SMBCLK IN Clock pin of SMBUS circuitry, 5V tolerant:   13 SMB_A1_tri IN Clock pin of SMBUS dire sees.   14 DFB_OUT# SMBus darlerses.   15 DFB_OUT Curry Curry   16 DFB_OUT Curry True half of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.   16 DFF_0 Curr True half of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to eliminate phase error.   17 DIF_1 Curr 0.7V differential true dock output   18 DIF_1 Curr 0.7V differential true dock output   19 DIF_1 Curr 0.7V differential true dock output   10 DVD PWR Power supply, nominal 3.3V   20 VDD PWR Power supply, nominal 3.3V   21 VDD PVR Power supply, nominal 3.3V   22 VDD PVR Power supply, nominal 3.3V   23 DIF_2 OUT 0.7V differential Complementary dock output   24 DIF_3 OUT 0.7V differential Complementary dock output   25 VDD PVR Power supply, nominal 3.3V   26 DIF_4 OUT				SMBus Addresses.
13     SMB_A1_tri     IN     SMBus darderss bit.     This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus darderss bit.       14     OFB_OUT#     OUT     SMBus darderss bit.     The second darderss bit.       15     OFB_OUT#     OUT     Orgenentary half of differential feedback output, provides feedback signal to the PLL for synchronization with input dock to aliminate phase error.       16     DIF_0     OUT     0.7V differential Conglementary dock output       17     DIF_0     OUT     0.7V differential Conglementary dock output       18     DIF_1     OUT     0.7V differential Conglementary dock output       20     ISF.2     OUT     0.7V differential Conglementary dock output       21     VDD     PVM     Power supply, nominal 3.W       22     VDD     PVM     Power supply, nominal 3.W       23     DIF_2     OUT     0.7V differential true dock output       24     DIF_3     OUT     0.7V differential true dock output       25     VDD     PVM     Power supply, nominal 3.W       26     DIF_3     OUT     0.7V differential true dock output       27				
Simple Art_In     IN     SMBLe Addresses.       10     DFB_OUT#     OUT     Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to afiminate phase error.       15     DFB_OUT     OUT     True half of differential teedback output.       17     DIF_O     OUT     0.7V differential to edo ko uput.       18     DIF_1     OUT     0.7V differential true clock output.       19     DIF_1     OUT     0.7V differential true clock output.       19     DIF_1     OUT     0.7V differential true clock output.       19     DIF_1     OUT     0.7V differential true clock output.       20     OD     PWR     Power supphy, nominal 3.3V       20     VDD     PWR     Power supphy, nominal 3.3V       21     VDD     PVRP     Power supphy, nominal 3.3V       22     VDD     PVRP     Power supphy, nominal 3.3V       24     DIF_2#     OUT     0.7V differential true clock output       25     VDE#     IN     Active low input for enabling DIF pair 2.       26     IDF     OUT	12	SMBCLK	IN	
1     DFB_OUT#     OUT     Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to eleminate phase error.       15     DFB_OUT     OUT     True half of differential feedback output, provides feedback signal to the PLL for synchronization with the in clock to eleminate phase error.       16     DIF_0     OUT     0.7V differential True clock output.       17     DIF_0     OUT     0.7V differential True clock output.       18     DIF_1     OUT     0.7V differential Complementary clock output.       20     SND     PVM     Ground pin.       21     VDD     PVM fore supply, nominal 3.3V       22     VDD     PVM Foreer supply, nominal 3.3V       23     DIF_2     OUT     0.7V differential Complementary clock output       24     DIF_2     OUT     0.7V differential Complementary clock output       25     vOEz#     IN     Active low input for enable outputs       26     DIF_3     OUT     0.7V differential Complementary clock output       27     VDD     PVM Forcen dpf n.       30     DIF_4     OUT     0.7V differentinta clock output	13	SMB_A1_tri	IN	
- $   -$	14			Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization
18UPS_UUTUUTclock to eliminate phase error.17DIF 0OUT0.77 differential Complementary clock output18DIF 1OUT0.77 differential Complementary clock output19DIF 10UT0.77 differential Complementary clock output20GNDPWRFournamentary clock output21VDDPWRPower suppy, nominal 3.3V22VDDPWRPower suppy, nominal 3.3V23DIF 2OUT0.77 differential trock clock output24DIF 2OUT0.77 differential cock output25VDE 2*NActive low input for enabling DIF pare 2.26VDE 7*OUT0.77 differential trock clock output27DIF 3*OUT0.77 differential trock clock output28VDE 2*NActive low input for enabling DIF pare 2.29ND 7*7*Mifferential trock clock output29DIF 3*OUT0.77 differential trock clock output20DIF 4OUT0.77 differential trock clock output21DIF 4OUT0.77 differential Complementary clock output22VDDPWRRower suppy, nominal 3.3V23VDE 4*IN1disable outputs, 0 = enable outputs34VDE4#IN1disable outputs, 0 = enable outputs35VDDPWRRower suppy, nominal 3.3V36NDDPWRRower suppy, nominal 3.3V37DIF 6OUT0.77 differential Complementary clock	14	DFB_001#	001	
Image: Constraint of the set of the se	15	DFB OUT	OUT	
17   DIF 0   0.7V differential Complementary clock output     18   DIF 1   0.0T   0.7V differential Complementary clock output     19   DIF 1#   0.0T   0.7V differential Complementary clock output     21   VDD   PWR   Ground pin.     22   VDD   PWR   Prower supply, nominal 3.3V     24   DIF 2   OUT   0.7V differential Complementary clock output     25   VDE 2#   OUT   0.7V differential Complementary clock output     26   DIF 2#   OUT   0.7V differential Complementary clock output     27   DIF 3#   OUT   0.7V differential Complementary clock output     28   VDE2#   IN   Active fock output     29   DIF 3#   OUT   0.7V differential Complementary clock output     20   DIF 4   OUT   0.7V differential Complementary clock output     30   DIF 5   OUT   0.7V differential Complementary clock output     31   DIF 6   OUT   0.7V differential Complementary clock output     32   VDE4#   IN   1-disable outputs 0.0   enal 4     34   DIF 5   OUT				
18   DiF.1   OUT   0.7V differential true dock output     20   GND   PWR   Gound pin.     21   VDD   PWR   Power supply, nominal 3.3V     22   VDD   PWR   Power supply, nominal 3.3V     23   DIF.2   OUT   0.7V differential rue dock output     24   DIF.2   OUT   0.7V differential rue dock output     25   VDD   PWR   Power supply, nominal 3.3V     26   DIF.2   OUT   0.7V differential rue dock output     27   VD2   PWR   Power supply, nominal 3.3V     28   VD2   PWR   Power supply, nominal 3.3V     29   GND   PWR   Ground pin.     30   DIF.3   OUT   0.7V differential rue dock output     31   DIF.4#   OUT   0.7V differential rue dock output     32   vCE4#   IN   Active low input for reabing DF pair 4     1   1   1   disable outputs, 0   = enable outputs     30   DIF.5   OUT   0.7V differential rue dock output   0     34   DIF.5#   OUT				
19   DIF_1#   OUT   0.7V differential Complementary clock output     20   GND   PWR   Ground pin.     21   VDD   PWR   Power supply, nominal 3.3V     22   VDD   PWR   Power supply, nominal 3.3V     23   DIF_2   OUT   0.7V differential to clock output     24   DIF_2#   OUT   0.7V differential to clock output     25   VC2#   N   Active low input for enabling DIF pair 2.     26   DIF_3#   OUT   0.7V differential to clock output     27   DIF_3#   OUT   0.7V differential clock output     28   VDD   PWR   Foreund pin.     29   GND   PWR   Foreund pin.     20   DIF_4   OUT   0.7V differential Complementary clock output     29   GND   PWR   Ground pin.     30   DIF_4   OUT   0.7V differential true clock output     31   DIF_5   OUT   0.7V differential true clock output     32   VDD   PWR   Power supply, nominal 3.3V     33   DIF_6   OUT   0.7V differential true clock				
20GNDPWRProver supply, nominal 3.3V21VDDPWRPower supply, nominal 3.3V23DIF_2OUT0.7V differential rue dock output24DIF_2#OUT0.7V differential rue dock output25VOE2#NActive low input for enabling DIF pair 2. 1 = disable outputs. 0. = enable outputs.26DIF_3#OUT0.7V differential complementary dock output27DIF.3OUT0.7V differential complementary dock output28DIF_4OUT0.7V differential complementary dock output29GNDPWRPower supply, nominal 3.3V29GNDPWRRover supply, nominal 3.3V29GNDPWRRover supply, nominal 3.3V29GNDPWRRound pin.30DIF_4OUT0.7V differential Complementary dock output31DIF_5OUT0.7V differential Complementary dock output32vOE4#INA ctive low input for enabling DIF pair 433DIF_5OUT0.7V differential Complementary dock output34DIF_6#OUT0.7V differential true dock output35VDDPWRRound pin.36GNDPWRRound pin.37DIF_6#OUT0.7V differential true dock output38DIF_6#OUT0.7V differential true dock output39DIF_6#OUT0.7V differential true dock output39DIF_6#OUT0.7V differential true dock output<				
21     VDD     PWR     Power supply, nominal 3.3V       22     VDD     PWR     Power supply, nominal 3.3V       23     DIF_2     OUT     0.7V differential true clock output       24     DIF_2#     OUT     0.7V differential true clock output       25     VDE2#     IN     Active low input for enabling DIF pair 2.       1=disable outputs, 0 = enable outputs     1     1=disable outputs, 0 = enable output       27     DIF_3#     OUT     0.7V differential rue clock output       28     VDD     PWR     Power supply, nominal 3.3V       29     GND     PWR     Ground spin.       30     DIF_4     OUT     0.7V differential true clock output       31     DIF_5     OUT     0.7V differential true clock output       32     VDE4#     IN     Active low input for enabling DIF pair 4       1=disable outputs, 0 = enable outputs     0     0       33     DIF_5     OUT     0.7V differential true clock output       34     DIF_6     OUT     0.7V differential true clock output       35     DDF     PWR				
22     VDD     PVWR     Power supply, nominal 3.3V       24     DIF_2     OUT     0.7V differential complementary clock output       24     DIF_2#     OUT     0.7V differential rue clock output       25     VOE2#     IN     Active low input for enabling DIF pair 2.       26     DIF_3     OUT     0.7V differential rue clock output       26     DIF_3     OUT     0.7V differential rue clock output       27     DIF_3#     OUT     0.7V differential rue clock output       28     VDD     PVWR     Ground pin.       29     GND     PVWR     Ground pin.       20     VCE4#     OUT     0.7V differential complementary clock output       30     DIF_4     OUT     0.7V differential rue clock output       31     DIF_5     OUT     0.7V differential rue clock output       32     VOE4#     IN     Active low input for enabling DIF pair 4       1_disable outputs, 0 = enable outputs     1_disable outputs     0       33     DIF_5     OUT     0.7V differential rue clock output       34     DIF				
23   DIF 2   OUT   0.77 differential Complementary clock output     24   DIF 2#   OUT   0.77 differential Complementary clock output     25   VCE2#   IN   Active Iow input for enabling DIF pair 2.     1=disable outputs.   0= enable outputs     27   DIF.3#   OUT   0.77 differential true clock output     28   VDD   PWR   Power supply, nominal 3.3V     28   GND   PWR   Power supply, nominal 3.3V     29   GND   PWR   Forund plin.     30   DIF_4   OUT   0.77 differential true clock output     30   DIF_5#   OUT   0.77 differential Complementary clock output     31   DIF_5#   OUT   0.77 differential true clock output     32   VOE4#   In   1=disable outputs.0   e outputs     33   DIF_5   OUT   0.77 differential true clock output   e outputs     34   DIF_5#   OUT   0.77 differential true clock output   e outputs     38   DIF 6#   OUT   0.77 differential true clock output   e outputs     39   VCE6#   IN   Activ				
24   DJF $2^{\#}$ QUT   0.7V differential Complementary dock output     25   vGE#   IN   Active low input for enabling DJF pair 2.     26   DJF.3   QUT   0.7V differential true clock output     27   DJF.3#   QUT   0.7V differential Complementary clock output     28   VDD   PWR   Power supply, nominal 3.3V     29   GND   PWR   Ground pin.     30   DJF_4   QUT   0.7V differential Complementary clock output     31   DJF_4   QUT   0.7V differential Complementary clock output     32   vQE4#   IN   Active low input for enabling DJF pair 4     1   -tdisable outputs, 0 = enable outputs   -     33   DJF_5   OUT   0.7V differential Complementary clock output     34   DJF_5#   OUT   0.7V differential Complementary clock output     35   VDD   PWR   Power supply, nominal 3.3V     36   GND   PWR   Power supply, nominal 3.3V     37   DJF_6   OUT   0.7V differential true clock output     38   DJF 6#   OUT   0.7V differential true clock output </td <td></td> <td></td> <td></td> <td></td>				
25 v $VGE2#$ Active low input for enabling DIF pair 2. 1 =disable outputs.26DIF_3OUT 0.7V differential True dock output27DIF_3#OUT 0.7V differential Complementary dock output28VDDPVRR29GNDPVRR29GNDPVRR30DIF_4OUT 0.7V differential Complementary dock output31DIF_4#OUT 0.7V differential true dock output32VOE4#N33DIF_5OUT 0.7V differential Complementary dock output34DIF_5#OUT 0.7V differential Complementary dock output35VDDPVRR36GNDPVRR37DIF_5#OUT 0.7V differential rue dock output38VDDPVRR39VOE6#IN31Active low input for enabling DIF pair 4. 1 = disable outputs, 0 = enable outputs39VOE6#IN39VOE6#IN40DIF_7#OUT 0.7V differential rue dock output30DIF_7#OUT 0.7V differential Complementary dock output39VOE6#IN40DIF 7#OUT 0.7V differential rue dock output41DIF 7#OUT 0.7V differential rue dock output42GNDPVRR44DIF 8OUT 0.7V differential rue dock output45VDDPVRR46VOE8#IN47DIF 9OUT 0.7V differential rue dock output48DIF 8#OUT 0.7V differential rue dock output<				
2VDE2#IN1 =disable outputs.0 = enable outputs26DIF_3OUT0.7V differential true clock output27DIF_3#OUT0.7V differential Complementary clock output28VDDPWRPower supply, nominal 3.3V29GNDPWRPower supply, nominal 3.3V29GNDPWRForund pin.30DIF_4OUT0.7V differential Complementary clock output31DIF_4#OUT0.7V differential Complementary clock output32VOE4#NActive low input for enabling DIF pair 433DIF_5OUT0.7V differential Complementary clock output34DIF_5#OUT0.7V differential Complementary clock output35VDDPWRPower supply, nominal 3.3V36GNDPWRPower supply, nominal 3.3V37DIF_6#OUT0.7V differential Complementary clock output38DIF_6#OUT0.7V differential Complementary clock output39VOE6#NActive low input for enabling DIF pair 6.411-disable outputs, 0 = enable outputs142GNDPVRGround pin.43VDDPVRGround pin.44DIF_7#OUT0.7V differential Complementary clock output44DIF_8#OUT0.7V differential Complementary clock output44DIF_9OUT0.7V differential Complementary clock output45DIF_8#OUT0.7V differential Complementary cl				
26     DiF_3     OUT     0.7V differential rue dock output       27     DIF_3#     OUT     0.7V differential Complementary dock output       28     VDD     PWR     Rower supply, nominal 3.3V       29     GND     PWR     Ground pin.       30     DIF_4     OUT     0.7V differential rue dock output       31     DIF_4     OUT     0.7V differential rue dock output       32     VOE4#     N     Active Iow input for enabling DIF pair 4       33     DIF_5     OUT     0.7V differential rue dock output       34     DIF_5     OUT     0.7V differential rue dock output       35     VDD     PWR     Power supply, nominal 3.3V       36     GND     PWR     Ground pin.       37     DIF_6     OUT     0.7V differential Complementary dock output       38     DIF_6     OUT     0.7V differential Complementary dock output       40     DIF_7     OUT     0.7V differential rue dock output       41     DIF 7#     OUT     0.7V differential Complementary dock output       42     GND	25	vOE2#	IN	
27DiF, $3#$ OUT0.7V differential Complementary clock output28VDDPWRPower supply, nominal 3.3V29GNDPWRGround pin.30DiF_4OUT0.7V differential true clock output31DiF_4#OUT0.7V differential Complementary clock output32vOE##INActive low input for enabling DIF pair 4 1 = disable outputs, 0 = enable outputs33DiF_5OUT0.7V differential true clock output34DiF_5#OUT0.7V differential true clock output35VDDPWRPower supply, nominal 3.3V36GNDPWRGround pin.37DiF_6OUT0.7V differential Complementary clock output38DIF_6#OUT0.7V differential Complementary clock output39vOE6#INActive low input for enabling DIF pair 6. 1 = disable outputs, 0 = enable outputs40DIF_7OUT0.7V differential Complementary clock output41DIF 7#OUT0.7V differential Complementary clock output42GNDPWRPower supply, nominal 3.3V43VDDPWRPower supply, nominal 3.3V44DIF 8#OUT0.7V differential true clock output45VIE0.7V differential true clock output46VDDPWRPower supply, nominal 3.3V47DIF 8#OUT0.7V differential true clock output48DIF 8#OUT0.7V differential Complementary clock output <td< td=""><td>26</td><td>DIF 3</td><td>OUT</td><td></td></td<>	26	DIF 3	OUT	
29GNDPWRGround pin.30DIF_4OUT0.7V differential true clock output31DIF_4#OUT0.7V differential Complementary clock output32vOE4#INActive low input for enabling DIF pair 4 1 = disable outputs, 0 = enable outputs32vOE4#INActive low input for enabling DIF pair 4 1 = disable outputs, 0 = enable outputs34DIF_5OUT0.7V differential true clock output35VDDPWRPower supply, norminal 3.3V36GNDPWRForound pin.37DIF_6OUT0.7V differential true clock output38DIF_6#OUT0.7V differential true clock output39vOE6#NActive low input for enabling DIF pair 6. 1 = disable outputs, 0 = enable outputs40DIF_7OUT0.7V differential true clock output41DIF_7#OUT0.7V differential Complementary clock output42GNDPWRFower supply, norminal 3.3V43VDDPWR B Ground pin.1 = disable outputs, 0 = enable outputs44DIF_8OUT0.7V differential Complementary clock output45DIF_8#OUT0.7V differential Complementary clock output46vOE8#INActive low input for enabling DIF pair 8. 1 = disable outputs, 0 = enable outputs47DIF_9#OUT0.7V differential Complementary clock output48DIF_9#OUT0.7V differential true clock output48DIF_9#OUT0.			OUT	
30   DIF_4   OUT   0.7V differential true clock output     31   DIF_4#   OUT   0.7V differential complementary clock output     32   vOE4#   N   Active low input for enabling DIF pair 4     33   DIF_5   OUT   0.7V differential true clock output     34   DIF_5#   OUT   0.7V differential complementary clock output     35   VDD   PWR   Power supply, nominal 3.3V     36   GND   PWR   Ground pin.     37   DIF_6   OUT   0.7V differential Complementary clock output     38   DIF_6   OUT   0.7V differential Complementary clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     1   -1=disable outputs, 0 = enable outputs   -1     40   DIF_7*   OUT   0.7V differential Complementary clock output     42   GND   PWR   Ground pin.     43   VDD   PWR   Ground pin.     44   DIF.8   OUT   0.7V differential true clock output     44   DIF.8   OUT   0.7V differential true clock output     45   DI	28	VDD	PWR	Power supply, nominal 3.3V
31   DIF_4#   OUT   0.7V differential Complementary clock output     32   vOE4#   IN   Active low input for enabling DIF pair 4     33   DIF_5   OUT   0.7V differential true clock outputs     33   DIF_5#   OUT   0.7V differential Complementary clock output     34   DIF_5#   OUT   0.7V differential Complementary clock output     35   VDD   PWR Power supply, nominal 3.3V     36   GND   PWR Ground pin.     37   DIF_6#   OUT   0.7V differential true clock output     38   DIF_6#   OUT   0.7V differential true clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     1   -1disable outputs, 0 = enable outputs   -     41   DIF_7   OUT   0.7V differential true clock output     42   GND   PWR   Ground pin.     43   VDD   PWR B   Ground pin.     44   DIF_8   OUT   0.7V differential true clock output     45   DIF.8#   OUT   0.7V differential true clock output     46   VOE8#   IN   Active	29	GND	PWR	Ground pin.
32 $VOE4#$ INActive low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs33DIF_5OUT0.7V differential true cock output34DIF_5#OUT0.7V differential true cock output35VDDPWRPower supply, nominal 3.3V36GNDPWRGround pin.37DIF_6OUT0.7V differential true clock output38DIF_6#OUT0.7V differential true clock output39vOE6#INActive low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs40DIF_7OUT0.7V differential true clock output41DIF_7#OUT0.7V differential true clock output42GNDPWRGround pin.43VDDPWRGround pin.44DIF_8OUT0.7V differential complementary clock output45DIF_8#OUT0.7V differential complementary clock output46vOE8#INActive low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs47DIF_9OUT0.7V differential Complementary clock output48DIF_9#OUT0.7V differential true clock output49VDDPWRPower supply, nominal 3.3V50VDDPWRPower supply, nominal 3.3V50VDDPWRPower supply, nominal 3.3V51GNNPWROUT52DIF_9#OUT0.7V differential true clock output53DIF_9#OUT	30	DIF_4	OUT	0.7V differential true clock output
32VOE4#IN1 =disable outputs, 0 = enable outputs33DIF_5OUT0.7V differential true clock output34DIF_5#OUT0.7V differential Complementary clock output35VDDPWRPower supply, nominal 3.3V36GNDPWRGround pin.37DIF_6OUT0.7V differential Complementary clock output38DIF_6#OUT0.7V differential rue clock output39vOE6#INActive low input for enabling DIF pair 6.40DIF_7OUT0.7V differential true clock output41DIF.7#OUT0.7V differential Complementary clock output42GNDPWRGround pin.43VDDPWRGround pin.44DIF.8#OUT0.7V differential true clock output45DIF.8#OUT0.7V differential complementary clock output46vOE8#INActive low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs47DIF.9OUT0.7V differential Complementary clock output48DIF.9#OUT0.7V differential Complementary clock output49VDDPWRRower supply, nominal 3.3V49VDDPWRRower supply, nominal 3.3V50VDDPWRPower supply, nominal 3.3V51GNDPWRRower supply, nominal 3.3V52DIF.10OUT0.7V differential Complementary clock output53DIF.10OUT0.7V differential Co	31	DIF_4#	OUT	0.7V differential Complementary clock output
Image: 1 - disable outputs, 0 = enable outputs30DIF_531DIF_532DIF_534DIF_5#35VDDPWRPower supply, nominal 3.3V36GND37DIF_639VOE6#19VOE6#10Active low input for enabling DIF pair 6.19VOE6#10Active low input for enabling DIF pair 6.101 - disable outputs, 0 = enable outputs40DIF_70UT0.7V differential rue clock output41DIF_70UT0.7V differential Complementary clock output42GND43VDD44DIF_8#0UT0.7V differential Complementary clock output45DIF_8#0UT0.7V differential Complementary clock output46vOE8#47DIF_90UT0.7V differential Complementary clock output48DIF_9#0UT0.7V differential Complementary clock output49VDD40PWR600.7V differential Complementary clock output41DIF_900T0.7V differential Complementary clock output42GND44DIF_900T0.7V differential Complementary clock output45DIF_9#00T0.7V differential Complementary clock output46VOE8#47DIF_9#00DPWR79#Power supply, nom	32	vOF4#	IN	
34   DIF_5#   OUT   0.7V differential Complementary clock output     35   VDD   PWR   Power supply, nominal 3.3V     36   GND   PWR   Ground pin.     37   DIF_6   OUT   0.7V differential true clock output     38   DIF_6#   OUT   0.7V differential Complementary clock output     38   DIF_6#   OUT   0.7V differential Complementary clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     1   adiable outputs, 0 = enable outputs   1   1     40   DIF_7   OUT   0.7V differential Complementary clock output     41   DIF_7#   OUT   0.7V differential Complementary clock output     42   GND   PWR   Ground pin.     43   VDD   PWR   Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential Complementary clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8.     47   DIF_9   OUT   0.7V differential Complementary clock ou				
35   VDD   PWR   Power supply, nominal 3.3V     36   GND   PWR   Ground pin.     37   DIF_6   OUT   0.7V differential true clock output     38   DIF 6#   OUT   0.7V differential Complementary clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     1   -1   abable outputs, 0 = enable outputs     40   DIF_7   OUT   0.7V differential rue clock output     41   DIF 7#   OUT   0.7V differential rue clock output     42   GND   PWR   Ground pin.     43   VDD   PWR   Ground pin.     44   DIF_8   OUT   0.7V differential rue clock output     45   DIF_8   OUT   0.7V differential rue clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8.     1   -disable outputs, 0 = enable outputs   0     47   DIF_9   OUT   0.7V differential rue clock output     48   DIF,9#   OUT   0.7V differential rue clock output     50   VDD   PWR   Power supply, nominal 3.3V				
36   GND   PWR   Ground pin.     37   DIF_6   OUT   0.7V differential true clock output     38   DIF_6#   OUT   0.7V differential complementary clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     1   =disable outputs, 0 = enable outputs   1     40   DIF_7   OUT   0.7V differential true clock output     41   DIF_7#   OUT   0.7V differential complementary clock output     42   GND   PWR   Ground pin.     43   VDD   PWR Bround pin.     44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential true clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8.     1   =disable outputs, 0 = enable outputs   1   =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output   4     48   DIF_9#   OUT   0.7V differential s.3V   5     50   VDD   PWR   Power supply, nominal 3.3V   5				
37   DIF_6   OUT   0.7V differential true clock output     38   DIF_6#   OUT   0.7V differential Complementary clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     1   -disable outputs, 0 = enable outputs     40   DIF_7   OUT   0.7V differential true clock output     41   DIF_7#   OUT   0.7V differential Complementary clock output     42   GND   PWR   Ground pin.     43   VDD   PWR Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential Complementary clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8.     1   -isable outputs, 0 = enable outputs   4     47   DIF_9   OUT   0.7V differential Complementary clock output     48   DIF_9#   OUT   0.7V differential Complementary clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Ground pin.     52   DIF_10   OUT				
38   DIF_6#   OUT   0.7V differential Complementary clock output     39   vOE6#   IN   Active low input for enabling DIF pair 6.     40   DIF_7   OUT   0.7V differential Irue clock outputs     41   DIF_7#   OUT   0.7V differential Irue clock output     42   GND   PWR   Ground pin.     43   VDD   PWR Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential Complementary clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8.     1   -disable outputs, 0   = enable outputs   -     47   DIF_9#   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential Complementary clock output     50   VDD   PWR   Rower supply, nominal 3.3V     51   GND   PWR   Rower supply, nominal 3.3V     52   DIF_10   OUT   0.7V differential true clock output  <				
39   vOE6#   IN   Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs     40   DIF_7   OUT   0.7V differential true clock output     41   DIF_7#   OUT   0.7V differential complementary clock output     42   GND   PWR   Ground pin.     43   VDD   PWR Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential Complementary clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Power supply, nominal 3.3V     51   GND   PWR   Rover supply, nominal 3.3V     51   GND   PWR   Power supply, nominal 3.3V     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V diffe				
39   VOE6#   IN   1 =disable outputs, 0 = enable outputs     40   DIF_7   OUT   0.7V differential true clock output     41   DIF_7#   OUT   0.7V differential Complementary clock output     42   GND   PWR   Ground pin.     42   GND   PWR   Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8.     47   DIF_9   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential true clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Power supply, nominal 3.3V     51   GND   PWR   Power supply, nominal 3.3V     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential true clock output     54   DIF_11   OUT   0.7V differential true clock output     55 <td>38</td> <td>DIF_6#</td> <td>001</td> <td></td>	38	DIF_6#	001	
40   DIF_7   OUT   0.7V differential true clock output     41   DIF_7#   OUT   0.7V differential Complementary clock output     42   GND   PWR   Ground pin.     43   VDD   PWR Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential complementary clock output     45   VOE8#   IN   Active low input for enabling DIF pair 8.     1   =disable outputs, 0 = enable outputs   1   =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output   48     48   DIF_9#   OUT   0.7V differential Complementary clock output   49     49   VDD   PWR   Power supply, nominal 3.3V   50     50   VDD   PWR   Power supply, nominal 3.3V   50     51   GND   PWR   Ground pin.   52     52   DIF_10   OUT   0.7V differential true clock output   53     53   DIF_10#   OUT   0.7V differential true clock output   54     54	39	vOE6#	IN	
41DIF_7#OUT0.7V differential Complementary clock output42GNDPWRGround pin.43VDDPWRPower supply, nominal 3.3V44DIF_8OUT0.7V differential true clock output45DIF_8#OUT0.7V differential Complementary clock output46vOE8#INActive low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs47DIF_9OUT0.7V differential true clock output48DIF_9#OUT0.7V differential Complementary clock output49VDDPWRPower supply, nominal 3.3V50VDDPWRPower supply, nominal 3.3V51GNDPWRGround pin.52DIF_10OUT0.7V differential true clock output53DIF_10#OUT0.7V differential true clock output54DIF_11#OUT0.7V differential true clock output55DIF_11#OUT0.7V differential Complementary clock output56VDDAPWR3.3V power for the PLL core.	40			
42   GND   PWR   Ground pin.     43   VDD   PWR   Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential Complementary clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Ground pin.     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11#   OUT   0.7V differential Complementary clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				
43   VDD   PWR   Power supply, nominal 3.3V     44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential Complementary clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Power supply, nominal 3.3V     51   GND   PWR   Ground pin.     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11#   OUT   0.7V differential Complementary clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				
44   DIF_8   OUT   0.7V differential true clock output     45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential Complementary clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Ground pin.     51   GND   PWR   Ground pin.     52   DIF_10   OUT   0.7V differential Complementary clock output     53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11#   OUT   0.7V differential Complementary clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				
45   DIF_8#   OUT   0.7V differential Complementary clock output     46   vOE8#   IN   Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs     47   DIF_9   OUT   0.7V differential true clock output     48   DIF_9#   OUT   0.7V differential true clock output     49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Ground pin.     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential true clock output     54   DIF_11#   OUT   0.7V differential true clock output     55   VDD   PWR   Ground pin.     52   DIF_10#   OUT   0.7V differential Complementary clock output     53   DIF_11#   OUT   0.7V differential Complementary clock output     54   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				
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48DIF_9#OUT0.7V differential Complementary clock output49VDDPWRPower supply, nominal 3.3V50VDDPWRPower supply, nominal 3.3V51GNDPWRGround pin.52DIF_10OUT0.7V differential true clock output53DIF_10#OUT0.7V differential Complementary clock output54DIF_11OUT0.7V differential true clock output55DIF_11#OUT0.7V differential Complementary clock output56VDDAPWR3.3V power for the PLL core.	47	DIF_9	OUT	
49   VDD   PWR   Power supply, nominal 3.3V     50   VDD   PWR   Power supply, nominal 3.3V     51   GND   PWR   Ground pin.     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11   OUT   0.7V differential true clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				0.7V differential Complementary clock output
51   GND   PWR   Ground pin.     52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11   OUT   0.7V differential true clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.	49	VDD	PWR	Power supply, nominal 3.3V
52   DIF_10   OUT   0.7V differential true clock output     53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11   OUT   0.7V differential true clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				
53   DIF_10#   OUT   0.7V differential Complementary clock output     54   DIF_11   OUT   0.7V differential true clock output     55   DIF_11#   OUT   0.7V differential Complementary clock output     56   VDDA   PWR   3.3V power for the PLL core.				
54 DIF_11 OUT 0.7V differential true clock output   55 DIF_11# OUT 0.7V differential Complementary clock output   56 VDDA PWR 3.3V power for the PLL core.				
55 DIF_11# OUT 0.7V differential Complementary clock output   56 VDDA PWR 3.3V power for the PLL core.				
56 VDDA PWR 3.3V power for the PLL core.				
	56	VDDA	PWR	3.3V power for the PLL core.
	• <b>⊤</b> @ 4		- דואו	BUFFER FOR PCIE GEN3 AND QPI 3 9ZX21200

## **Absolute Maximum Ratings**

Stresses above the ratings listed below can cause permanent damage to the 9ZX21200. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDD, VDDA	VDD for core logic and PLL			4.6	V	1,2
IO Supply Voltage	VDD	VDD for differential IO			4.6	V	1,2
Input Low Voltage	V <sub>IL</sub>		GND-0.5			V	1
Input High Voltage	V <sub>IH</sub>	Except for SMBus interface			$V_{DD}$ +0.5V	V	1
Input High Voltage	VIHSMB	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

## **Electrical Characteristics–Clock Input Parameters**

 $T_A = T_{COM}$ ; Supply Voltage  $V_{DD} = 3.3 V + -5\%$ 

	,						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	VIHDIE	Differential inputs	60.0	800	1150	mV	1
parg. renage		(single-ended measurement)					· ·
Input Low Voltage - DIF IN		Differential inputs	V <sub>SS</sub> - 300	0	300	mV	1
Input Low Voltage - DIF_IN	VILDIF	(single-ended measurement)	Vss- 300 0	300	шv	1	
Input Common Mode Voltage	V <sub>COM</sub>	Common Mode Input Voltage	300		1000	mV	1
- DIF_IN	V COM	Common Mode input voltage	000		1000		'
Input Amplitude - DIF_IN	VSWING	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I <sub>IN</sub>	$V_{IN} = V_{DD}$ , $V_{IN} = GND$	-5		5	uA	1
Input Duty Cycle	d <sub>tin</sub>	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	$J_{DIFIn}$	Differential Measurement	0		125	ps	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through +/-75mV window centered around differential zero

## **Electrical Characteristics–Input/Supply/Common Output Parameters**

 $T_A = T_{COM}$ ; Supply Voltage  $V_{DD} = 3.3 V + -5\%$ 

$T_A = T_{COM}$ ; Supply Voltage V PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	Т <sub>СОМ</sub>	Commmercial range	0		70	°C	1
Input High Voltage	V <sub>IH</sub>	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V <sub>DD</sub> + 0.3	V	1
Input Low Voltage	V <sub>IL</sub>	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
	I <sub>IN</sub>	Single-ended inputs, $V_{IN} = GND$ , $V_{IN} = VDD$	-5		5	uA	1
Input Current	I <sub>INP</sub>	Single-ended inputs $V_{IN} = 0 \text{ V}$ ; Inputs with internal pull-up resistors $V_{IN} = \text{VDD}$ ; Inputs with internal pull-down resistors	-200		200	uA	1
	F <sub>ibyp</sub>	$V_{DD} = 3.3 V$ , Bypass mode	33		150	MHz	2
Input Frequency	F <sub>ipll</sub>	$V_{DD} = 3.3 \text{ V}, 100 \text{MHz PLL} \text{ mode}$	90	100.00	110	MHz	2
	F <sub>ipll</sub>	V <sub>DD</sub> = 3.3 V, 133.33MHz PLL mode	120	133.33	147	MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
	CIN	Logic Inputs, except DIF_IN	1.5		5	pF	1
Capacitance	C <sub>INDIF_IN</sub>	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
Clk Stabilization	T <sub>STAB</sub>	From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.300	1	ms	1,2
Input SS Modulation Frequency	f <sub>MODIN</sub>	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	clocks	1,3
Tdrive_PD#	t <sub>DRVPD</sub>	DIF output enable after PD# de-assertion		16	300	us	1,3
Tfall	t <sub>F</sub>	Fall time of control inputs			10	ns	1,2
Trise	t <sub>R</sub>	Rise time of control inputs			10	ns	1,2
SMBus Input Low Voltage	VILSMB				0.8	V	1
SMBus Input High Voltage	VIHSMB		2.1		V <sub>DDSMB</sub>	V	1
SMBus Output Low Voltage	V <sub>OLSMB</sub>	@ I <sub>PULLUP</sub>			0.4	V	1
SMBus Sink Current	I <sub>PULLUP</sub>	@ V <sub>OL</sub>	4			mA	1
Nominal Bus Voltage	V <sub>DDSMB</sub>	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t <sub>RSMB</sub>	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t <sub>FSMB</sub>	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f <sub>MAXSMB</sub>	Maximum SMBus operating frequency			100	kHz	1,5

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

## **Electrical Characteristics–DIF 0.7V Current Mode Differential Outputs**

TA - TCOM; Oupping Voltage V							
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	2	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		8	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope	660	705	850	mV	1
Voltage Low	VLow	averaging on)	-150	1	150		1
Max Voltage	Vmax	Measurement on single ended signal using		725	1150	mV	1
Min Voltage	Vmin	absolute value. (Scope averaging off)	-300	-22			1
Vswing	Vswing	Scope averaging off	300	1407		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	309	550	mV	1, 5
Crossing Voltage (var)	∆-Vcross	Scope averaging off		22	140	mV	1, 6

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/( $3xR_R$ ). For  $R_R = 412\Omega$  (1%),  $I_{REF} = 2.7mA$ .  $I_{OH} = 6.4 \times I_{REF}$  and  $V_{OH} = 0.7V$  @  $Z_O = 85\Omega$  differential impedance.

<sup>2</sup> Measured from differential waveform

 $T_A = T_{COM}$ ; Supply Voltage VDD = 3.3 V +/-5%

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

<sup>5</sup> Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all Vcross measurements in any particular system. Note that this is a subset of V\_cross\_min/max (V\_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V\_cross\_delta to be smaller than V\_cross absolute.

## **Electrical Characteristics–Current Consumption**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Current	IDDVDD	133MHz, $C_L$ = Full load; VDD rail, Zo=85 $\Omega$		260	275	mA	1
Operating Current	I <sub>DDVDDA</sub>	133MHz, $C_L$ = Full load; VDD rail, Zo=85 $\Omega$		13	20	mA	1
Powerdown Current	I <sub>DDVDDPD</sub>	Power Down, VDD rail, Zo=85 $\Omega$		2	6	mA	1
Powerdown Cunent	I <sub>DDVDDAPD</sub>	Power Down, VDD rail, Zo=85 $\Omega$		1.3	2	mA	1

 $T_A = T_{COM;}$  Supply Voltage VDD = 3.3 V +/-5%

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

## **Electrical Characteristics–Skew and Differential Jitter Parameters**

 $T_A = T_{COM}$ : Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t <sub>SPO_PLL</sub>	Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V	-100	29	100	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t <sub>PD_BYP</sub>	Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V	2.5	3.7	4.5	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t <sub>DSPO_PLL</sub>	Input-to-Output Skew Varation in PLL mode across voltage and temperature	-50		50	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t <sub>DSPO_BYP</sub>	Input-to-Output Skew Varation in Bypass mode across voltage and temperature	-250		250	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t <sub>DTE</sub>	Random Differential Tracking error beween two 9ZX devices in Hi BW Mode		2.9	5	ps (rms)	1,2,3,5,8
CLK_IN, DIF[x:0]	t <sub>DSSTE</sub>	Random Differential Spread Spectrum Tracking error beween two 9ZX devices in Hi BW Mode		14	75	ps	1,2,3,5,8
DIF{x:0]	t <sub>SKEW_ALL</sub>	Output-to-Output Skew across all outputs (Common to Bypass and PLL mode)		32	65	ps	1,2,3,8
PLL Jitter Peaking	j <sub>peak-hibw</sub>	LOBW#_BYPASS_HIBW = 1	0	1.8	2.5	dB	7,8
PLL Jitter Peaking	j <sub>peak-lobw</sub>	LOBW#_BYPASS_HIBW = 0	0	0.7	2	dB	7,8
PLL Bandwidth	рII <sub>нівw</sub>	LOBW#_BYPASS_HIBW = 1	2	3.1	4	MHz	8,9
PLL Bandwidth	pll <sub>LOBW</sub>	LOBW#_BYPASS_HIBW = 0	0.7	1.1	1.4	MHz	8,9
Duty Cycle	t <sub>DC</sub>	Measured differentially, PLL Mode	45	49.6	55	%	1
Duty Cycle Distortion	t <sub>DCD</sub>	Measured differentially, Bypass Mode @100MHz	-2	-0.2	2	%	1,10
Jitter, Cycle to cycle	t	PLL mode		15.7	50	ps	1,11
	τ <sub>jcyc-cyc</sub>	Additive Jitter in Bypass Mode		0.1	50	ps	1,11

#### Notes for preceding table:

<sup>1</sup> Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

<sup>2</sup> Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

<sup>3</sup> All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

<sup>4</sup> This parameter is deterministic for a given device

<sup>5</sup> Measured with scope averaging on to find mean value.

<sup>6.</sup> t is the period of the input clock

<sup>7</sup> Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

<sup>8.</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>9</sup> Measured at 3 db down or half power point.

<sup>10</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

<sup>11</sup> Measured from differential waveform

## **Electrical Characteristics–Phase Jitter Parameters**

 $T_A = T_{COM:}$  Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
	t <sub>jphPCleG1</sub>	PCIe Gen 1		32	86	ps (p-p)	1,2,3
	t <sub>jphPCleG2</sub>	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.8	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.9	3.1	ps (rms)	1,2
Phase Jitter, PLL Mode	t <sub>jphPCleG3</sub>	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.45	1	ps (rms)	1,2,4
		QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.20	0.5	ps (rms)	1,5
	t <sub>jphQPI_SMI</sub>	QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.14	0.3	ps (rms)	1,5
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.12	0.2	ps (rms)	1,5
	t <sub>iphPCleG1</sub>	PCIe Gen 1		0.10	10	ps (p-p)	1,2,3
		PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.13	0.1	ps (rms)	1,2,6
	t <sub>jphPCleG2</sub>	PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.10	0.5	ps (rms)	1,2,6
<i>Additive</i> Phase Jitter, Bypass mode	t <sub>jphPCleG3</sub>	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.10	0.2	ps (rms)	1,2,4,6
Dypace mode	t <sub>jphQPI_SMI</sub>	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.09	0.1	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.09	0.1	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.09	0.1	ps (rms)	1,5,6

<sup>1</sup> Applies to all outputs.

<sup>2</sup> See http://www.pcisig.com for complete specs

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> Subject to final radification by PCI SIG.

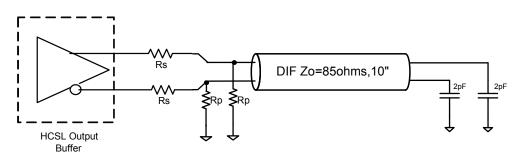
<sup>5</sup> Calculated from Intel-supplied Clock Jitter Tool v 1.6.4

<sup>6</sup> For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)<sup>2</sup> = (total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>

## **Differential Output Terminations**

DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.2 or 43.2

9ZX21200 Differential Test Loads



## Clock Periods–Differential Outputs with Spread Spectrum Disabled

	Center				Measurement	Window				
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC OFF	Freq. MHz	-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter A bs Per Max	Units	Notes
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3
Dii	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

## **Clock Periods–Differential Outputs with Spread Spectrum Enabled**

			Measurement Window							
	•	1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC ON	Center Freq. MHz	-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max	Units	Notes
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
DIF	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

#### Notes:

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZX21200 itself does not contribute to ppm error.

<sup>3</sup> Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

<sup>4</sup> Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

## General SMBus Serial Interface Information for 9ZX21200

#### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time

Index Block Write Operation

• Controller (host) sends a Stop bit

#### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- · Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

	Index Block F	Read O	peration
Co	ntroller (Host)		IDT (Slave/Receiver)
Т	starT bit		
S	lave Address	_	
WR	WRite	_	
		_	ACK
Beg	jinning Byte = N	_	
			ACK
RT	RT Repeat starT		
S	lave Address		
RD	ReaD		
			ACK
			Data Byte Count=X
	ACK		
		_	Beginning Byte N
	ACK		
		fe	0
	0	X Byte	0
	0	×	0
	0		
			Byte N + X - 1
Ν	Not acknowledge		
Р	stoP bit		

Index Block write Operation									
Controll	er (Host)		IDT (Slave/Receiver)						
Т	starT bit								
Slave A	Address	] [							
WR	WRite								
			ACK						
Beginning	g Byte = N								
			ACK						
Data Byte	Count = X								
			ACK						
Beginnir	ig Byte N								
			ACK						
0		$\times$							
0		X Byte	0						
0		ë	0						
			0						
Byte N	+ X - 1								
			ACK						
Р	stoP bit								

Byte	e 0 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	3	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Op	Latch	
Bit 6	3	PLL Mode 0	PLL Operating Mode Rd back 0	R	Readback Table		Latch
Bit 5		Reserved				0	
Bit 4			Reserved				
Bit 3	These bits	PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	S/W Control	0
Bit 2	available in B	PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode		1
Bit 1	rev only.	PLL Mode 0	D PLL Operating Mode 1 RW Readback Table		1		
Bit 0	2	100M_133M#	Frequency Select Readback	R	133MHz	100MHz	Latch

#### SMBusTable: PLL Mode, and Frequency Select Register

#### SMBusTable: Output Control Register

Byte	1 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	42/41	DIF_7_En	Output Control overrides OE# pin	RW			1
Bit 6	38/37	DIF_6_En	Output Control overrides OE# pin	RW			1
Bit 5	34/35	DIF_5_En	Output Control overrides OE# pin	RW			1
Bit 4	30/29	DIF_4_En	Output Control overrides OE# pin	RW	Low/Low	Enable	1
Bit 3	25/26	DIF_3_En	Output Control	RW	LOW/LOW		1
Bit 2	23/24	DIF_2_En	Output Control	RW			1
Bit 1	18/19	DIF_1_En	Output Control	RW			1
Bit 0	16/17	DIF_0_En	Output Control	RW			1

#### SMBusTable: Output Control Register

Byte	e 2	Pin #	Name	Name Control Function		0	1	Default	
Bit 7				Reserved				0	
Bit 6				Reserved					
Bit 5				Reserved					
Bit 4				Reserved					
Bit 3	5	5/54	DIF_11_En	Output Control	RW			1	
Bit 2	5	3/52	DIF_10_En	Output Control	RW	Low/Low	Enable	1	
Bit 1	4	8/47	DIF_9_En	Output Control	RW	LOW/LOW	EndDie	1	
Bit 0	4	6/45	DIF_8_En	Output Control	RW			1	

#### SMBusTable: Reserved Register

Byte 3	Pin #	# Name	Control Function	Туре	0	1	Default	
Bit 7			Reserved				0	
Bit 6			Reserved				0	
Bit 5			Reserved					
Bit 4			Reserved					
Bit 3			Reserved				0	
Bit 2			Reserved					
Bit 1			Reserved					
Bit 0			Reserved				0	

#### SMBusTable: Reserved Register

Byte	e 4	Pin #	Name	Control Function	Туре	0	1	Default	
Bit 7				Reserved				0	
Bit 6				Reserved				0	
Bit 5				Reserved					
Bit 4				Reserved					
Bit 3				Reserved				0	
Bit 2				Reserved					
Bit 1			Reserved						
Bit 0				Reserved				0	

#### SMBusTable: Vendor & Revision ID Register

Byte	5 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-	RID3		R			
Bit 6	-	RID2	REVISION ID	R	A rev = 0000		Х
Bit 5	-	RID1	REVISIONID	R	B rev = 0001		Х
Bit 4	-	RID0		R			Х
Bit 3	-	VID3		R			0
Bit 2	-	VID2	VENDOR ID	R	0001 for IDT/ICS		0
Bit 1	-	VID1	VENDORID	R	000110	101/103	0
Bit 0	-	VID0		R			1

#### SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-	De	evice ID 7 (MSB)	R			1
Bit 6	-		Device ID 6	R			1
Bit 5	-		Device ID 5	R			0
Bit 4	-		Device ID 4	R	1200 is 200 de	0	
Bit 3	-		Device ID 3	R	1200 is 200 de	1	
Bit 2	-		Device ID 2	R			0
Bit 1	-		Device ID 1		1		0
Bit 0	-		Device ID 0	R	]		0

#### SMBusTable: Byte Count Register

Byte	e 7	Pin #	Name	Name Control Function		0	1	Default
Bit 7				Reserved				
Bit 6				Reserved				0
Bit 5				Reserved				0
Bit 4		-	BC4		RW			0
Bit 3		-	BC3	Writing to this register configures how	RW	Default value	is 8 hex, so 9	1
Bit 2		-	BC2	many bytes will be read back.	RW	bytes (0 to 8) w	ill be read back	0
Bit 1		-	BC1	many bytes will be read back.	RW	by de	efault.	0
Bit 0		-	BC0		RW			0

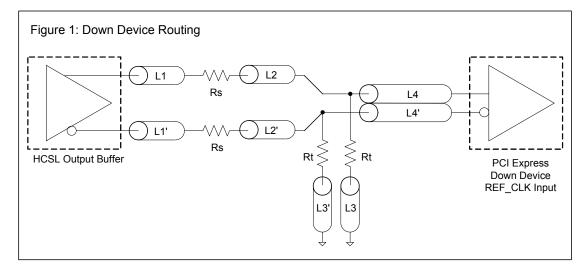
#### SMBusTable: Reserved Register

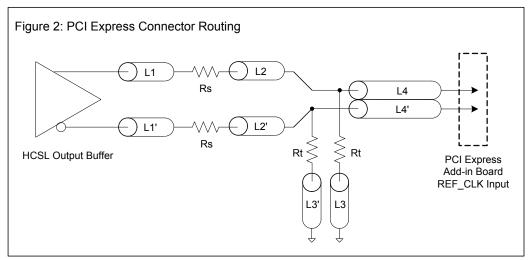
Byte	e 8	Pin #	Name	Control Function	Туре	0	1	Default		
Bit 7				Reserved						
Bit 6				Reserved						
Bit 5				Reserved						
Bit 4				Reserved						
Bit 3				Reserved				0		
Bit 2				Reserved						
Bit 1			Reserved							
Bit 0				Reserved				0		

DIF Reference Clock							
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure				
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1				
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1				
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1				
Rs (100 ohm differential traces)	33	ohm	1				
Rs (85 ohm differential traces)	27	ohm	1				

Down Device Differential Routing			
L4 length, route as coupled microstrip 1000hm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 1000hm differential trace	1.8 min to 14.4 max	inch	1

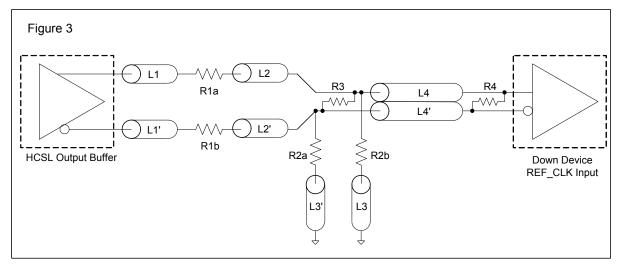
Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 1000hm differential trace	0.225 min to 12.6 max	inch	2



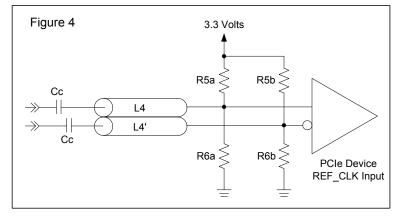


	Alternative Termination for LVDS and other Common Differential Signals (figure 3)									
Vdiff	Vp-р	Vcm	R1	R2	R3	R4	Note			
0.45v	0.22v	1.08	33	150	100	100				
0.58	0.28	0.6	33	78.7	137	100				
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible			
0.60	0.3	1.2	33	174	140	100	Standard LVDS			
R1a = R	R1a = R1b = R1									

R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)						
Component	Value	Note				
R5a, R5b	8.2K 5%					
R6a, R6b	1K 5%					
Сс	0.1 µF					
Vcm	0.350 volts					



#### (Ref) Seating Plane (N<sub>D</sub>-1)x e N<sub>D</sub> & N<sub>E</sub> (Ref) Even Index Area A1 (Typ) A3 If $N_D \& N_E$ 2 Anvil are Even Singulation (N<sub>E</sub>-1)x e Е E2 -- or --(Ref) E2 2 ¥. Top View Sawn Singulation (Ref) Δ $N_D \& N_E$ D е Thermal Base Odd D2 С -D2-0.08 С **Dimensions (mm)** Symbol Min Max 0.8 1.0 А A1 0 0.05 A3 0.25 Reference b 0.18 0.3 0.50 BASIC е D x E BASIC 8.00 x 8.00 D2 MIN./MAX. 4.35 4.65 E2 MIN./MAX. 5.05 5.35 L MIN./MAX. 0.3 0.5 Ν 56 14 ND N<sub>E</sub> 14

## Package Outline and Package Dimensions (56-pin VFQFPN)

## **Ordering Information**

Part / Order Number	Shipping Package	Package	Temperature	Difference
9ZX21200AKLF	Trays	56-pin VFQFPN	0 to +70°C	W/O Byte 0 PLL Control
9ZX21200AKLFT	Tape and Reel	56-pin VFQFPN	0 to +70°C	W/O Byte 0 FEL Control
9ZX21200BKLF	Trays	56-pin VFQFPN	0 to +70°C	With Byte 0 PLL Mode
9ZX21200BKLFT	Tape and Reel	56-pin VFQFPN	0 to +70°C	Control

#### "LF" suffix to the part number designates Pb-Free configuration, RoHS compliant.

#### "A" and "B" are the device revision designators (will not correlate with the datasheet revision).

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IDT® 12-OUTPUT DIFFERENTIAL Z-BUFFER FOR PCIE GEN3 AND QPI

## **Revision History**

Rev.	Issue Date	Issuer	Description	Page #				
			1. Updated electrical tables with char data					
Α	9/13/2011	RDW	2. Fixed minor typographical errors	Various				
			3. Moved to final					
			1. Added B rev functionality description to Features, Benefits					
в	12/8/2011	12/8/2011 RDV	12/8/2011 RD	12/8/2011	12/8/2011	איחם	2. Updated tDSPO_BYP parameter from +/-350ps to +/-250ps	1,7,11,15
				11000	3. Updated SMBus Byte 0 with B rev functionality	1,7,11,13		
			4. Updated ordering information to include B rev					
			1. Updated Power Connections table to be consistent with 9ZXL1230					
С	4/18/2012	RDW	2. Updated Rp values on Output Terminations Table from 43.2 ohms to	2,8				
			42.2 or 43.2 ohms to be consistent with Intel.					
D	4/15/2013	RDW	Corrected typo in OE# Latency parameter; changed 1 min. to 3 max.	5				
	4/13/2013		cycles to 4 min. to 12 max. clocks.	5				

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