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MDB1900ZB

MICREL ®

Zero Delay Buffer
for PCIe (Gen1/Gen2/Gen3),
## SAS, SATA, ESI, and QPI

General Description

The MDB1900ZB is a true zero delay buffer with a fully-integrated, high-performance, low-power, and low-phase noise programmable PLL.

The MDB1900ZB is capable of distributing the reference clocks for PCIe (Gen1/Gen2/Gen3), SATA, ESI, SAS, SMI and Intel® Quickpath Interconnect (QPI). The MDB1900ZB works in conjunction with a CK410B+, CK509B or CK420BQ clock synthesizer to provide reference clocks to multiple agents.

The MDB1900ZB is designed for Intel's DB1900Z specification. The Intel part designation for the MDB1900ZB is identified as G20746-002.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram
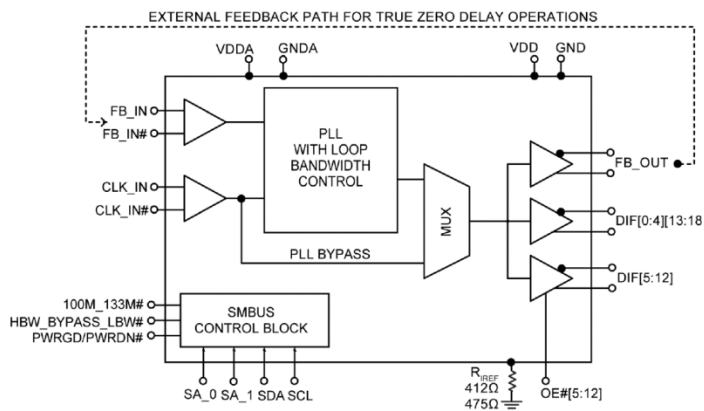
Features

- Supports zero delay (0ps) buffer mode for 100MHz and 133MHz clock frequencies.
- External feedback path for true zero delay operations
- Zero delay (PLL) mode can filter jitter in incoming clock
- Selectable PLL bandwidth for PLL mode
- Supports fanout buffer mode for clock frequencies between 0 and 250MHz
- Differential input reference with HCSL logic (0~0.7V)
- Nineteen differential HCSL-compatible clock output pairs
- Eight dedicated OE# pins to control their assigned output. Glitch free assertion/de-assertion.
- Spread spectrum modulation tolerant for EMI reduction
- SMBus interface for controlling output properties (enable/disable and delay tuning)
- Disabled outputs in power-down mode for maximum power savings
- Nine selectable SMBus addresses so multiple devices can share the same SMBus
- 3.3V or 2.5V operation
- Commercial temperature range (0°C to +70°C)
- 72-pin 10mm × 10mm QFN package
- GREEN, RoHS, and PFOS compliant

Applications

- PCI Express timing (Gen1/2/3) in Intel platforms, specifically the Romley platform
- SATA / SAS timing (storage)
- ESI and SMI systems (storage)
- Intel Quickpath Interconnect

Key Specifications

- Cycle-to-cycle jitter (PLL mode): <35ps
- Output-to-output skew: <35ps
- Input-to-output delay (PLL mode): Fixed at 0ps
- Input-to-output delay variation (PLL mode): 13ps
- Phase Jitter, PCIe Gen3: 0.25ps
- Accumulated Jitter, QPI 9.6Gb/s: <0.15ps

Intel is a registered trademark of Intel Corporation.

Ordering Information

Part Number	Marking	Shipping	Ambient Temperature Range	Package[1]
MDB1900ZBQY TR	MDB1900ZBQ	Tape and Reel	-40°C to +85°C	72-Pin 10mm × 10mm QFN
MDB1900ZBQZ TR	MDB1900ZBQ	Tape and Reel	0°C to +70°C	72-Pin 10mm × 10mm QFN

Note:

1. Device is GREEN, RoHS, and PFOS compliant. Lead finish is 100% matte tin.

Pin Configuration

72-Pin 10mm × 10mm QFN
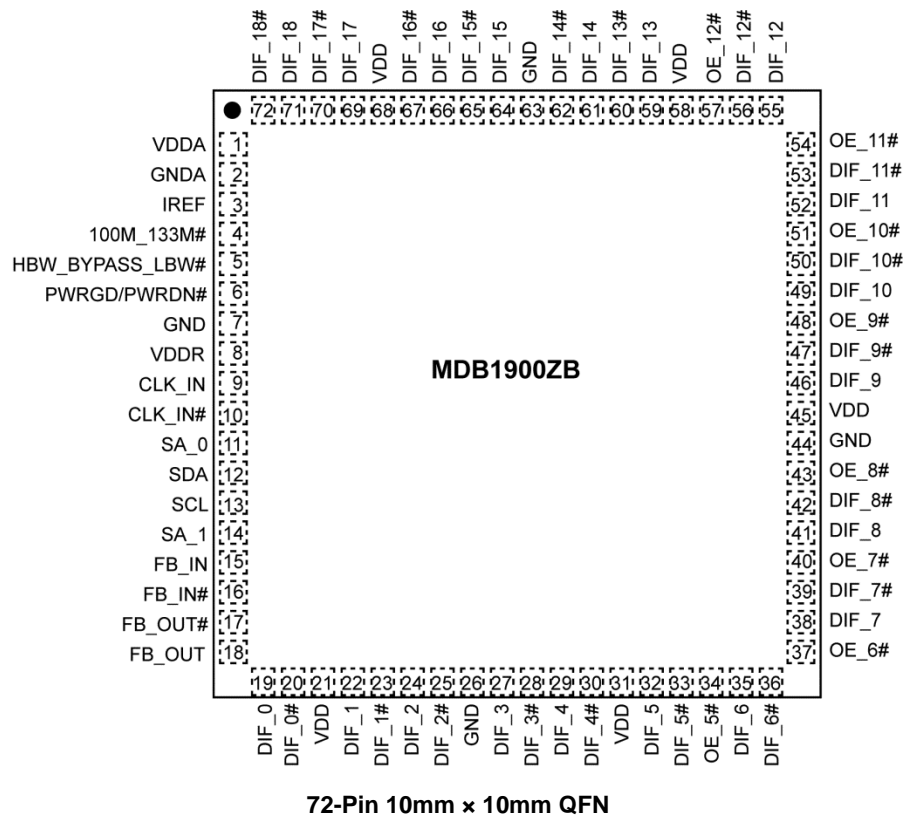
Pin Description

Pin Number	Pin Name	Type[2]	Pin Function
1	VDDA	PWR	3.3V or 2.5V Core Power Supply.
2	GNDA	GND	Core Ground.
3	IREF	I	I_{REF} = (1.1V)/(R_{IREF}). A precision resistor (R_{IREF}) is attached to this pin and to ground to set the reference current for the differential current mode output pairs. R_{IREF} = 475Ω for 100Ω trace, R_{IREF} = 412Ω for 85Ω trace.
4	100M_133M#	I, SE	3.3V LVTTL Input. Input/output frequency select. Logic 1 = 100MHz output (default, 50KΩ pull-up resistor) Logic 0 = 133.33MHz output
5	HBW_BYPASS_LBW#	I, SE	Tri-level input for selecting bypass or PLL bandwidth mode. High = High PLL bandwidth mode Mid = Bypass mode Low = Low PLL bandwidth mode
6	PWRGD/PWRDN#	I, SE	3.3V LVTTL Input for power good and power-down control. 50KΩ pull-down resistor.
7	GND	GND	Ground.
8	VDDR	PWR	3.3V or 2.5V power supply for differential clock input.
9	CLK_IN	I, DIF	0.7V HCSL differential clock input reference. True input pin.
10	CLK_IN#	I, DIF	0.7V HCSL differential clock input reference. Complementary input pin.
11	SA_0	I, SE	Tri-level input to set SMBus address for this device. Works together with SA_1.
12	SDA	I/O	Open Collector SMBus Data I/O Pin (SDATA). 5V tolerant.
13	SCL	I, SE	SMBus Slave Clock Input (SCLK). 5V tolerant.
14	SA_1	I, SE	Tri-level input to set SMBus address for this device. Works together with SA_0.
15	FB_IN	I, DIF	ZDB Feedback, 0.7V differential clock input, true input pin.
16	FB_IN#	I, DIF	ZDB Feedback, 0.7V differential clock input, complementary input pin.
17	FB_OUT	O, DIF	ZDB Feedback, 0.7V differential clock output (HCSL-compatible), true output pin.
18	FB_OUT#	O, DIF	ZDB Feedback, 0.7V differential clock output (HCSL-compatible), complementary output pin.
19	DIF_0	O, DIF	0.7V Differential Clock Output 0 (HCSL-compatible), true output pin.
20	DIF_0#	O, DIF	0.7V Differential Clock Output 0 (HCSL-compatible), complementary output pin.
21	VDD	PWR	3.3V or 2.5V Power Supply.
22	DIF_1	O, DIF	0.7V Differential Clock Output 1 (HCSL-compatible), true output pin.
23	DIF_1#	O, DIF	0.7V Differential Clock Output 1 (HCSL-compatible), complementary output pin.
24	DIF_2	O, DIF	0.7V Differential Clock Output 2 (HCSL-compatible), true output pin.

Note:

2. I = Input
    O = Output
    I/O = Bi-directional
    SE = Single-ended
    DIF = Differential
    PWR = 3.3V or 2.5V power
    GND = Ground

Pin Description (Continued)

Pin Number	Pin Name	Type[2]	Pin Function
25	DIF_2#	O, DIF	0.7V Differential Clock Output 2 (HCSL-compatible), complementary output pin.
26	GND	GND	Ground.
27	DIF_3	O, DIF	0.7V Differential Clock Output 3 (HCSL-compatible), true output pin.
28	DIF_3#	O, DIF	0.7V Differential Clock Output 3 (HCSL-compatible), complementary output pin.
29	DIF_4	O, DIF	0.7V Differential Clock Output 4 (HCSL-compatible), true output pin.
30	DIF_4#	O, DIF	0.7V Differential Clock Output 4 (HCSL-compatible), complementary output pin.
31	VDD	PWR	3.3V or 2.5V power supply.
32	DIF_5	O, DIF	0.7V Differential Clock Output 5 (HCSL-compatible), true output pin.
33	DIF_5#	O, DIF	0.7V Differential Clock Output 5 (HCSL-compatible), complementary output pin.
34	OE_5#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 5 (50kΩ pull-down).
35	DIF_6	O, DIF	0.7V Differential Clock Output 6 (HCSL-compatible), true output pin.
36	DIF_6#	O, DIF	0.7V Differential Clock Output 6 (HCSL-compatible), complementary output pin.
37	OE_6#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 6 (50kΩ pull-down).
38	DIF_7	O, DIF	0.7V Differential Clock Output 7 (HCSL-compatible), true output pin.
39	DIF_7#	O, DIF	0.7V Differential Clock Output 7 (HCSL-compatible), complementary output pin.
40	OE_7#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 7 (50kΩ pull-down).
41	DIF_8	O, DIF	0.7V Differential Clock Output 8 (HCSL-compatible), true output pin.
42	DIF_8#	O, DIF	0.7V Differential Clock Output 8 (HCSL-compatible), complementary output pin.
43	OE_8#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 8 (50kΩ pull-down).
44	GND	GND	Ground
45	VDD	PWR	3.3V or 2.5V power supply.
46	DIF_9	O, DIF	0.7V Differential Clock Output 9 (HCSL-compatible), true output pin.
47	DIF_9#	O, DIF	0.7V Differential Clock Output 9 (HCSL-compatible), complementary output pin.
48	OE_9#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 9 (50kΩ pull-down).
49	DIF_10	O, DIF	0.7V Differential Clock Output 10 (HCSL-compatible), true output pin.
50	DIF_10#	O, DIF	0.7V Differential Clock Output 10 (HCSL-compatible), complementary output pin.

Pin Description (Continued)

Pin Number	Pin Name	Type[2]	Pin Function
51	OE_10#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 10 (50kΩ pull-down).
52	DIF_11	O, DIF	0.7V Differential Clock Output 11 (HCSL-compatible), true output pin.
53	DIF_11#	O, DIF	0.7V Differential Clock Output 11 (HCSL-compatible), complementary output pin.
54	OE_11#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 11 (50kΩ pull-down).
55	DIF_12	O, DIF	0.7V Differential Clock Output 12 (HCSL-compatible), true output pin.
56	DIF_12#	O, DIF	0.7V Differential Clock Output 12 (HCSL-compatible), complementary output pin.
57	OE_12#	I, SE	3.3V LVTTL active-low input for enabling Differential Output 12 (50KΩ pull-down).
58	VDD	PWR	3.3V or 2.5V Power Supply.
59	DIF_13	O, DIF	0.7V Differential Clock Output 13 (HCSL-compatible), true output pin.
60	DIF_13#	O, DIF	0.7V Differential Clock Output 13 (HCSL-compatible), complementary output pin.
61	DIF_14	O, DIF	0.7V Differential Clock Output 14 (HCSL-compatible), true output pin.
62	DIF_14#	O, DIF	0.7V Differential Clock Output 14 (HCSL-compatible), complementary output pin.
63	GND	GND	Ground.
64	DIF_15	O, DIF	0.7V Differential Clock Output 15 (HCSL-compatible), true output pin.
65	DIF_15#	O, DIF	0.7V Differential Clock Output 15 (HCSL-compatible), complementary output pin.
66	DIF_16	O, DIF	0.7V Differential Clock Output 16 (HCSL-compatible), true output pin.
67	DIF_16#	O, DIF	0.7V Differential Clock Output 16 (HCSL-compatible), complementary output pin.
68	VDD	PWR	3.3V or 2.5V Power Supply.
69	DIF_17	O, DIF	0.7V Differential Clock Output 17 (HCSL-compatible), true output pin.
70	DIF_17#	O, DIF	0.7V Differential Clock Output 17 (HCSL-compatible), complementary output pin.
71	DIF_18	O, DIF	0.7V Differential Clock Output 18 (HCSL-compatible), true output pin.
72	DIF_18#	O, DIF	0.7V Differential Clock Output 18 (HCSL-compatible), complementary output pin.
ePad	Exposed Pad	GND	The center pad must be connected to the ground plane both for electrical ground and thermal relief.

Absolute Maximum Ratings[3]

Analog Supply Voltage (V$_{DDA}$) ....+4.6V
I/O Supply Voltage (V$_{DD}$). ....+4.6V
Input Low Voltage (V$_{IL}$)...−0.5V
Input High Voltage (V$_{IH}$) ....+4.6V
Storage Temperature (T$_S$)........................−65°C to +150°C
ESD Rating[5]..2kV

Operating Ratings[4]

Supply Voltage (V$_{DD}$, V$_{DDA}$) .... +2.375V to +3.465V
Ambient Temperature (T$_A$) ....0°C to +70°C
Junction Temperature (T$_J$) ....+125°C
Case Temperature (T$_C$).. +110°C
Thermal Resistance, Junction-to-Ambient (T$_{JA}$)
   Still Air...26°C/W

DC Electrical Characteristics[6]

V$_{DDA}$ = V$_{DD}$ = 3.3V or 2.5 ±5%, T$_A$ = 0°C to +70°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V$_{DDA}$, V$_{DD}$	3.3V or 2.5V Operating Range	3.3V or 2.5V ±5%	2.375		3.465	V
V$_{IH}$	Input High Voltage	V$_{DD}$ = 3.3V. Single-ended inputs, except SMBus and tri-level inputs.	2		V$_{DD}$ + 0.3	V
V$_{IL}$	Input Low Voltage	V$_{DD}$ = 3.3V. Single-ended inputs, except SMBus and tri-level inputs.	GND − 0.3		0.8	V
I$_{IL}$	Input Leakage Current[7]	0 < V$_{IN}$ < V$_{DD}$	−5		5	µA
V$_{IL\_TRI}$	Input Low Voltage (Tri-Level Input)	V$_{DD}$ = 3.3V	0		0.9	V
V$_{IM\_TRI}$	Input Mid Voltage (Tri-Level Input)	V$_{DD}$ = 3.3V	1.3		1.8	V
V$_{IH\_TRI}$	Input High Voltage (Tri-Level Input)	V$_{DD}$ = 3.3V	2.4		V$_{DD}$	V
C$_{IN}$	Input Capacitance[8]		1		4.5	pF
C$_{OUT}$	Output Capacitance[8]		1		4.5	pF
L$_{PIN}$	Pin Inductance				7	nH
I$_{DD\_3.3V}$	Operating Supply Current (I$_{DDA}$ + I$_{DD}$)	All outputs driven.			450	mA
I$_{DD\_3.3PD}$	Power-Down Current	V$_{DD}$ = 3.3V. All differential pairs tri-stated.			43	mA
V$_{DDSMB}$	Nominal SMBus Voltage		2.7		5.5	V
V$_{OLSMB}$	SMBus Output Low Voltage	@ I$_{PULLUP}$			0.4	V
V$_{IHSMB}$	SMBus input High Voltage		2.1		V$_{DDSMB}$	V
V$_{ILSMB}$	SMBus input Low Voltage				0.8	V

Notes:

3. Exceeding the absolute maximum ratings may damage the device.

4. The device is not guaranteed to function outside its operating ratings.

5. Devices are ESD sensitive. Handling precautions are recommended. Human Body Model.

6. Specification for packaged product only.

7. Input leakage current. Does not include inputs with pull-up or pull-down resistors.

8. Capacitance value does not include pin capacitance.

DC Electrical Characteristics[6] (Continued)

$V_{DDA} = V_{DD} = 3.3V$ or 2.5 ±5%, $T_A = 0°C$ to +70°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{PULLUP(SMBUS)}$	Current-Through Pull-Up Resistance or Current Source		100		470	µA
$R_{PULLUP(SMBUS)}$	Pull-Up Resistance Value	V_{DD} = 3.3V ±5%	4.7		27	KΩ
$T_{R(SMBUS)}$	Rise Time for SDA and SCL	$(V_{IL(MAX)} - 0.15)$ to $(V_{IH(MIN)} + 0.15)$			1000	ns
$T_{F(SMBUS)}$	Fall Time for SDA and SCL	$(V_{IH(MIN)} + 0.15)$ to $(V_{IL(MAX)} - 0.15)$			300	ns

AC Electrical Characteristics – (CLK_IN, CLK_IN#) Clock Input Parameters

$V_{DDA} = V_{DD} = 3.3V$ or 2.5V ±5%, $T_A = 0°C$ to +70°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH} (CLK_IN), (CLK_IN#)	Differential Input High Voltage	Statistical measurement on single-ended signal using oscilloscope V_{HIGH} math function.	660		850	mV
V_{IL} (CLK_IN), (CLK_IN#)	Differential Input Low Voltage	Statistical measurement on single-ended signal using oscilloscope V_{LOW} math function.	−150			mV
V_{IHMAX} (CLK_IN), (CLK_IN#)	Differential Input Maximum Voltage (include overshoot)	Statistical measurement on single-ended signal using absolute value.			1150	mV
V_{ILMIN} (CLK_IN), (CLK_IN#)	Differential Input Minimum Voltage (include undershoot)	Statistical measurement on single-ended signal using absolute value.	−300			mV
V_{SWING} (CLK_IN), (CLK_IN#)	Differential Input Swing (include over / undershoot)	Differential input (peak-to-peak).	300		1450	mV
V_{OX} (CLK_IN), (CLK_IN#)	Crossing Point Input Voltage (absolute)		250		550	mV
V_{OXV} (CLK_IN), (CLK_IN#)	Crossing Point Input Voltage (variation)	Variation of crossing over all edges.			140	mV
Edge Rate (CLK_IN), (CLK_IN#)	Minimum (CLK_IN)/(CLK_IN#) Edge Rate[9]	Based on single-ended measurement.	0.35			V/ns
Slew Rise (CLK_IN), (CLK_IN#)	Input Rising Slew Rate[10]	Differential measurement	0.70		4	V/ns

Notes:

9. The minimum input edge rate is 0.35V/ns single-ended or 0.7V/ns differential for both 100MHz and 133.33MHz.

10. The slew rate (0.70V/ns to 4V/ns) measurement on differential waveform for both 100MHz and 133.33MHz.

AC Electrical Characteristics – (CLK_IN, CLK_IN#) Clock Input Parameters (Continued)

$V_{DDA} = V_{DD}$ = 3.3V or 2.5V ±5%, T_A = 0°C to +70°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Slew Fall (CLK_IN), (CLK_IN#)	Input Falling Slew Rate[10]	Differential measurement.	0.70		4	V/ns
DC (CLK_IN), (CLK_IN#)	Input Duty Cycle	Differential measurement.	45		55	%
CY-CY Jitter (CLK_IN), (CLK_IN#)	Cycle-to-cycle Input Jitter				50	ps

Spread Spectrum (SSC) Specification for Clock Input (CLK_IN, CLK_IN#)

Symbol	Parameter	Value
Modulation	Down Spread	(−0.5%) Maximum
Modulation Frequency	Modulation Frequency	30kHz to 33kHz
Modulation Profile	Triangular or Lexmark	(−0.5%) Maximum

AC Electrical Characteristics – HCSL Outputs

$V_{DDA} = V_{DD} = 3.3V$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$.

Symbol	Parameter	Condition (100MHz, 133.33MHz)	Min.	Typ.	Max.	Units
T_{STAB}	Clock Stabilization Time[11]			160	300	µs
$L_{ACCURACY}$	Long Accuracy[12, 13, 14, 15, 16]				100	ppm
T_{ABSMIN}	Absolute Minimum Host CLK Period[12, 16, 17]	When (−0.5%) spread spectrum clock input (SSC_{ON}).	(Period − 0.125ns)			ns
T_{ABSMIN}	Absolute Minimum Host CLK Period[12, 16, 17]	When non-spread spectrum SSC clock input (SSC_{OFF}).	−2.5%			ns
Edge Rate	Edge Rate[18]	Measurement from differential waveform.	1.0	2.5	4.0	V/ns
T_R	Rise Time[19, 20] (see Figure 2)	Single-ended measurement $V_{OL} = 0.175V$, $V_{OH} = 0.525V$.	175	225	700	ps
T_F	Fall Time[19, 20] (see Figure 2)	Single-ended measurement $V_{OH} = 0.525V$, $V_{OL} = 0.175V$.	175	225	700	ps

Notes:

11. This is the time from ramping the power supply, or assertion the PWRGD and when valid CLK_IN input until the time that stable clocks are output from the device (PLL locked).

12. All long-time accuracy and clock period specifications are guaranteed assuming that the input reference (CLK_IN, CLK_IN#) meets the CK410B+ or CK420BQ clock period specifications.

13. The long accuracy is 0ppm, when average only over any integer number of SSC periods.

14. When (SSC_{OFF}), using the frequency counter with the measurement interval equal to or greater than 0.15s, target frequencies are 100,000,000Hz, 133,333,333Hz.

15. When (SSC_{ON}), using the frequency counter with the measurement interval equal to or greater than 0.15s, target frequencies are 99,750,000Hz, 133,000,000Hz.

16. Measurement taken from differential waveform.

17. The average period over any 1µs period of time must be greater than the minimum and less than the maximum specified period.

18. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from (−150mV) to (+150mV) on the differential waveform. Scope is set to average. Signal must be monotonic through the V_{OL} to V_{OH} region for T_R and T_F.

19. Measured from $V_{OL} = 0.175V$ and $V_{OH} = 0.525V$. Only valid for rising clock and falling CLK#. Signal must be monotonic through V_{OL} to V_{OH} region for T_R and T_F. Measurement taken from single-ended waveform. The translation will be (0.5V/ns minimum to 2V/ns maximum) for single-ended edge rate. Refer to Figure 2.

20. Measurement taken from single-ended waveform.

AC Electrical Characteristics – HCSL Outputs (Continued)

$V_{DDA} = V_{DD} = 3.3V$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$.

Symbol	Parameter	Condition (100MHz, 133.33MHz)	Min.	Typ.	Max.	Units
ΔT_R	Rise Time Variation[20, 21]				125	ps
ΔT_F	Fall Time Variation[20, 21]				125	ps
T_{RFM}	Rise and Fall Time Matching[20, 21, 22]	Determined as fraction of $2 \times (T_R - T_F) / (T_R+T_F)$.			20	%
V_{HIGH}	Differential Output High Voltage (typically 0.7V)[20, 23]	Statistical measurement on single-ended signal using oscilloscope math function.	660	700	850	mV
V_{LOW}	Differential Output Low Voltage (typically 0.0V)[20, 24]	Statistical measurement on single-ended signal using oscilloscope math function.	-150	8	50	mV
V_{OVS}	Differential Output Maximum Voltage (include overshoot) (see Figure 3)	Statistical measurement on single-ended signal using absolute value.			V_{HIGH} + 0.3V	V
V_{UDS}	Differential Output Minimum Voltage (include undershoot) (see Figure 3)	Statistical measurement on single-ended signal using absolute value.			V_{LOW} − 0.3V	V
V_{RB}	Ringback Voltage (see Figure 3)	Statistical measurement on single-ended signal using absolute value (−0.5%) SSC input (SSC$_{ON}$).	0.2			V
V_{RB}	Ringback Voltage (see Figure 3)	Statistical measurement on single-ended signal using absolute value non-SSC input (SSC$_{OFF}$).	V_X ±0.2			V
V_{OX} (Absolute)	Absolute Crossing Point Voltages[20, 25]	Statistical measurement on single-ended signal using absolute value.	250		550	mV
Total ΔV_{OX}	Total Variation of V_{OX} Over All Edges[20, 26]	Statistical measurement on single-ended signal using absolute value.			140	mV

Notes:

21. Measured with oscilloscope, averaging off, and using minimum/maximum statistics. Variation is the delta between minimum and maximum.

22. Measured with oscilloscope, averaging on, the difference between the rising edge rate (average) of clock versus the falling edge rate (average) of clock#.

23. A statistical average high value for V_{HIGH} obtained by using the oscilloscope V_{HIGH} math function.

24. A statistical average low value for V_{LOW} obtained by using the V_{LOW} math function.

25. The crossing point should meet the absolute and relative crossing point specifications simultaneously.

26. ΔV_{OX} is defined as the total variation of all crossing voltages of rising CLOCK and falling CLOCK#.

AC Electrical Characteristics – HCSL Outputs (Continued)

$V_{DDA} = V_{DD} = 3.3V$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$.

Symbol	Parameter	Condition (100MHz, 133.33MHz)	Min.	Typ.	Max.	Units
Duty Cycle	Differential Output Duty Cycle[16] (see Figure 4)	Measurement from differential waveform (measured at V_{OX}). PLL Mode	45	50	55	%
Duty Cycle Distortion	Differential Output Duty Cycle Distortion[16, 31] (see Figure 4)	Measurement from differential waveform (measured at V_{OX}). Bypass mode at 100MHz	-2	0	+2	%
T_{SKEW}	Output-to-Output Delay[27, 28] (see Figure 4)	Measured at V_{OX} (common to PLL and bypass mode).		18	35	ps
T_{PD} (CLK_IN) to DIF [18:0]	Input-to-Output Delay[27, 28]	Measured at V_{OX} (PLL mode).	−35	±15	35	ps
ΔT_{PD} (CLK_IN) to DIF_[18:0]	Input-to-Output Delay Variation[27]	Measured at V_{OX} (PLL mode).		13	|75|	ps
CY-CY Jitter DIF_[18:0] DIF#_[18:0]	Cycle-to-Cycle Jitter[16]	PLL mode.		25	35	ps
T_{PD} (CLK_IN) to DIF_[18:0]	Input-to-Output Delay[27]	Measured at V_{OX} (bypass mode).	0.7		4.5	ns
ΔT_{PD} (CLK_IN) to DIF_[18:0]	Input-to-Output Delay Variation[27]	Measured at V_{OX} (bypass mode) absolute.			|225|	ps
T_{DTE}	Random Differential Tracking Error between two devices in Hi BW mode[29]	PLL (HBW) mode, no spread spectrum.			3.5	ps
T_{DSSTE}	P2P Differential Spread Spectrum Tracking Error between two devices in Hi BW mode[30]	PLL (HBW) mode, SSCON.			50	ps

Notes:

27. Measured from differential crossing point (V_{OX}) to differential crossing point (V_{OX}) with scope averaging on to find mean value. V_{OX} (relative) minimum and maximum are derived using the following: V_{OX} (relative) minimum = $0.250 + 0.5 V_{HAVG} − 0.7V$) and V_{OX} (relative) maximum = $0.550 − 0.5 (0.7V − V_{HAVG})$.

28. Measured into fixed 2pF load capacitor. Input to output skew is measured at the first output edge following the corresponding input.

29. This parameter is measured at the outputs of two MDB1900ZB devices in the HBW mode driven by a CK420BQ. The random differential tracking error is the differential phase jitter. It is the accumulated phase jitter, not including the effect of spread spectrum and not shared by the outputs. The jitter is measured into 2pF load cap and from differential cross-point to differential cross-point

30. This is the P2P difference in spread spectrum tracking error between two MDB1900ZB devices in Hi BW mode. The parameter is measured at the output of two MDB1900ZB devices driven by a CK420BQ with SSCON.

31. Duty Cycle Distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

Clock Period − SSC Disabled

SSC$_{OFF}$ Center Frequency MHz	Measurement Window							Units
	1 Clock	1μs	0.1s	0.1s	0.1s	1μs	1 Clock	
	−JITTER$_{c-c}$ Absolute per Minimum	−SSC Short Average Minimum	−ppm Long Average Minimum	0ppm Period	+ppm Long Average Maximum	+SSC Short Average Maximum	+JITTER$_{c-c}$ Absolute per Maximum	
100	9.94900		9.99900	10.00000	10.00100		10.05100	ns
133.0	7.44925		7.49925	7.50000	7.50075		7.55075	ns

Clock Period − SSC Enabled

SSC$_{ON}$ Center Frequency MHz	Measurement Window							Units
	1 Clock	1μs	0.1s	0.1s	0.1s	1μs	1 Clock	
	−JITTER$_{c-c}$ Absolute per Minimum	−SSC Short Average Minimum	−ppm Long Average Minimum	0ppm Period	+ppm Long Average Maximum	+SSC Short Average Maximum	+JITTER$_{c-c}$ Absolute per Maximum	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns
133.0	7.44930	7.44930	7.51805	7.51880	7.51955	7.5830	7.58830	ns

PLL Bandwidth – Peaking and Phase Jitter (SSC$_{OFF}$)

$V_{DDA} = V_{DD} = 3.3V$ or $2.5V$ $\pm5\%$, $T_A = 0°C$ to $+70°C$.

| Symbol	Condition (100MHz, 133.33MHz)	Min.	Typ.	Max.	Units
PLL Jitter Peaking[32]	HBW_BYPASS_LBW# = 0 (low bandwidth)			1.0	dB
	HBW_BYPASS_LBW# = 1 (high bandwidth)			1.0	
PLL Bandwidth[33]	HBW_BYPASS_LBW# = 0 (low bandwidth)	0.70	1.0	1.4	MHz
	HBW_BYPASS_LBW# = 1 (high bandwidth)	2	3.0	4	
Phase Jitter (PCIe Gen1)[34, 36, 37]	PCIe Gen1 (including PLL BW 1.5MHz − 22MHz, damping factor = 0.54, T_D = 10ns, F_{TRK} = 1.5MHz)		16	50	ps$_{(Pk-Pk)}$
Phase Jitter (PCIe Gen2)[36, 37, 39]	PCIe Gen2 (including PLL BW 8MHz − 16MHz, jitter peaking = 3dB, damping factor = 0.54, T_D = 10ns) (low band, F < 1.5MHz)		0.9	1.75	ps$_{RMS}$
	PCIe Gen2 (including PLL BW 8MHz − 16MHz, jitter peaking = 3dB, damping factor = 0.54, T_D = 10ns) (high band, [1.5MHz < F < Nyquist])		1.1	2.0	
Phase Jitter (PCIe Gen3)[35, 36, 37, 39]	PCIe Gen3 (including PLL BW 2MHz − 4MHz, CDR = 10MHz) (low band)		1.9	2.5	ps$_{RMS}$
	PCIe Gen3 (including PLL BW 2MHz − 4MHz, CDR = 10MHz) (high band)		0.25	1.0	
Accumulated Jitter (4.8Gbps QPI)[37, 38, 40]	QPI, accumulated jitter (4.8Gbps or 6.4Gbps, 100MHz or 133MHz, 12 UI)		0.12	0.25	ps$_{RMS}$
Accumulated Jitter (6.4Gbps QPI)[37, 38, 40]	QPI, accumulated jitter (4.8Gbps or 6.4Gbps, 100MHz or 133MHz, 12 UI)		0.14	0.25	ps$_{RMS}$
Accumulated Jitter (8Gbps QPI_SMI)[37, 38]	QPI, accumulated jitter (8Gbps, 100MHz, 12 UI)		0.08	0.20	ps$_{RMS}$
Accumulated Jitter (9.6Gbps QPI_SMI)[37, 38]	QPI, accumulated jitter (9.6Gbps, 100MHz, 12 UI)		0.06	0.15	ps$_{RMS}$
Accumulated Jitter (4MHz SMI)	SMI, 4MHz accumulated jitter		0.06	0.2	ps$_{RMS}$
Accumulated Jitter (16MHz SMI)	SMI, 16MHz accumulated jitter		0.12	0.5	ps$_{RMS}$

Notes:

32. Measured as maximum pass band gain. At frequencies with the loop BW, highest point-of-magnification is called PLL jitter peaking.

33. Measured at 3dB down or half-power point.

34. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.

35. PCIe Gen3 filter characteristics are subject to final ratification by PCI-SIG. Check with PCI-SIG for latest specification.

36. The damping factor damping factor = 0.54 is implying a jitter peaking of 3dB.

37. Post processed evaluation through Intel-supplied Matlab scripts.

38. Measuring on 100MHz output using the template file in the clock jitter tool.

39. Measuring on 100MHz PCIe SRC output using the template file in the clock jitter tool.

40. Measuring on 100MHz, 133.33MHz output using the template file in the clock jitter tool.

PLL Bandwidth – Peaking and Phase Jitter (SSC$_{ON}$)

$V_{DDA} = V_{DD} = 3.3V$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $+70°C$.

| Symbol	Condition (100MHz, 133.33MHz)	Min.	Typ.	Max.	Units
PLL Jitter Peaking[32]	HBW_BYPASS_LBW# = 0 (low bandwidth)			1.0	dB
	HBW_BYPASS_LBW# = 1 (high bandwidth)			1.0	
PLL Bandwidth[33]	HBW_BYPASS_LBW# = 0 (low bandwidth)	0.70	1.0	1.4	MHz
	HBW_BYPASS_LBW# = 1 (high bandwidth)	2	3.0	4	
Phase Jitter (PCIe Gen1)[34, 36, 37]	PCIe Gen1 (including PLL BW 1.5MHz – 22MHz, damping factor = 0.54, T_D = 10ns, F_{TRK} = 1.5MHz)		16	50	ps$_{(Pk-Pk)}$
Phase Jitter (PCIe Gen2)[36, 37, 39]	PCIe Gen2 (including PLL BW 8MHz – 16MHz, Jitter Peaking = 3dB, damping factor = 0.54, T_D = 10ns) (low band, F < 1.5MHz)		1.0	1.75	ps$_{RMS}$
	PCIe Gen2 (including PLL BW 8MHz – 16MHz, Jitter Peaking = 3dB, damping factor = 0.54, T_D = 10ns) (high band, [1.5MHz < F < Nyquist])		1.0	2.0	
Phase Jitter (PCIe Gen3)[35, 36, 37, 39]	PCIe Gen3 (including PLL BW 2MHz – 4MHz, CDR = 10MHz) (low band)		2.7	3.0	ps$_{RMS}$
	PCIe Gen3 (including PLL BW 2MHz – 4MHz, CDR = 10MHz) (high band)		0.28	1.0	
Accumulated Jitter (4.8Gbps QPI)[37, 38, 40]	QPI, accumulated jitter (4.8Gbps or 6.4Gbps, 100MHz or 133MHz, 12 UI)		0.18	0.25	ps$_{RMS}$
Accumulated Jitter (6.4Gbps QPI)[37, 38, 40]	QPI, accumulated jitter (4.8Gbps or 6.4Gbps, 100MHz or 133MHz, 12 UI)		0.20	0.25	ps$_{RMS}$
Accumulated Jitter (8Gbps QPI_SMI)[37, 38]	QPI, accumulated jitter (8Gbps, 100MHz, 12 UI)		0.09	0.20	ps$_{RMS}$
Accumulated Jitter (9.6Gbps QPI_SMI)[37, 38]	QPI, accumulated jitter (9.6Gbps, 100MHz, 12 UI)		0.08	0.15	ps$_{RMS}$
Accumulated Jitter (4MHz SMI)	SMI, 4MHz accumulated jitter		0.12	0.2	ps$_{RMS}$
Accumulated Jitter (16MHz SMI)	SMI, 16MHz accumulated jitter		0.06	0.5	ps$_{RMS}$

Functional Diagram
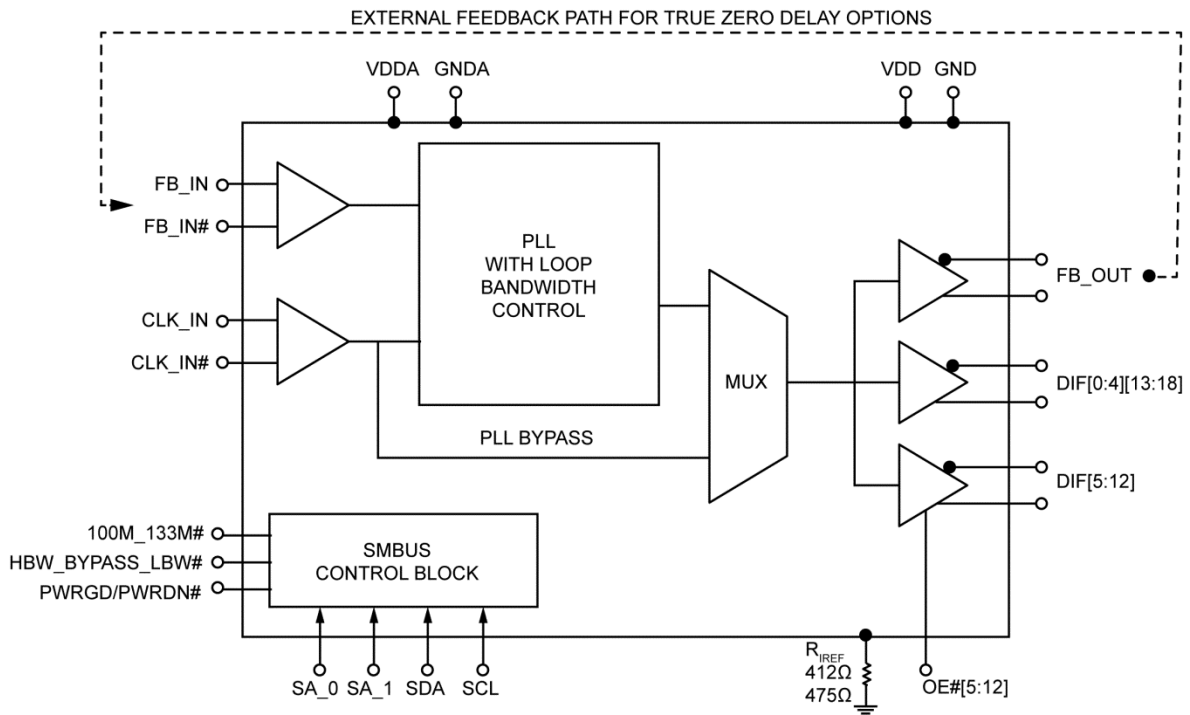
External Feedback (FB_OUT, FB_OUT#) and (FB_IN, FB_IN#) Topology

The MDB1900ZB utilizes external feedback topology to achieve low input-to-output delay variation. Place the shunt and series resistors as close to the (FB_OUT, FB_OUT#) (Pins 18 and 17) as possible (refer to Figure 1).
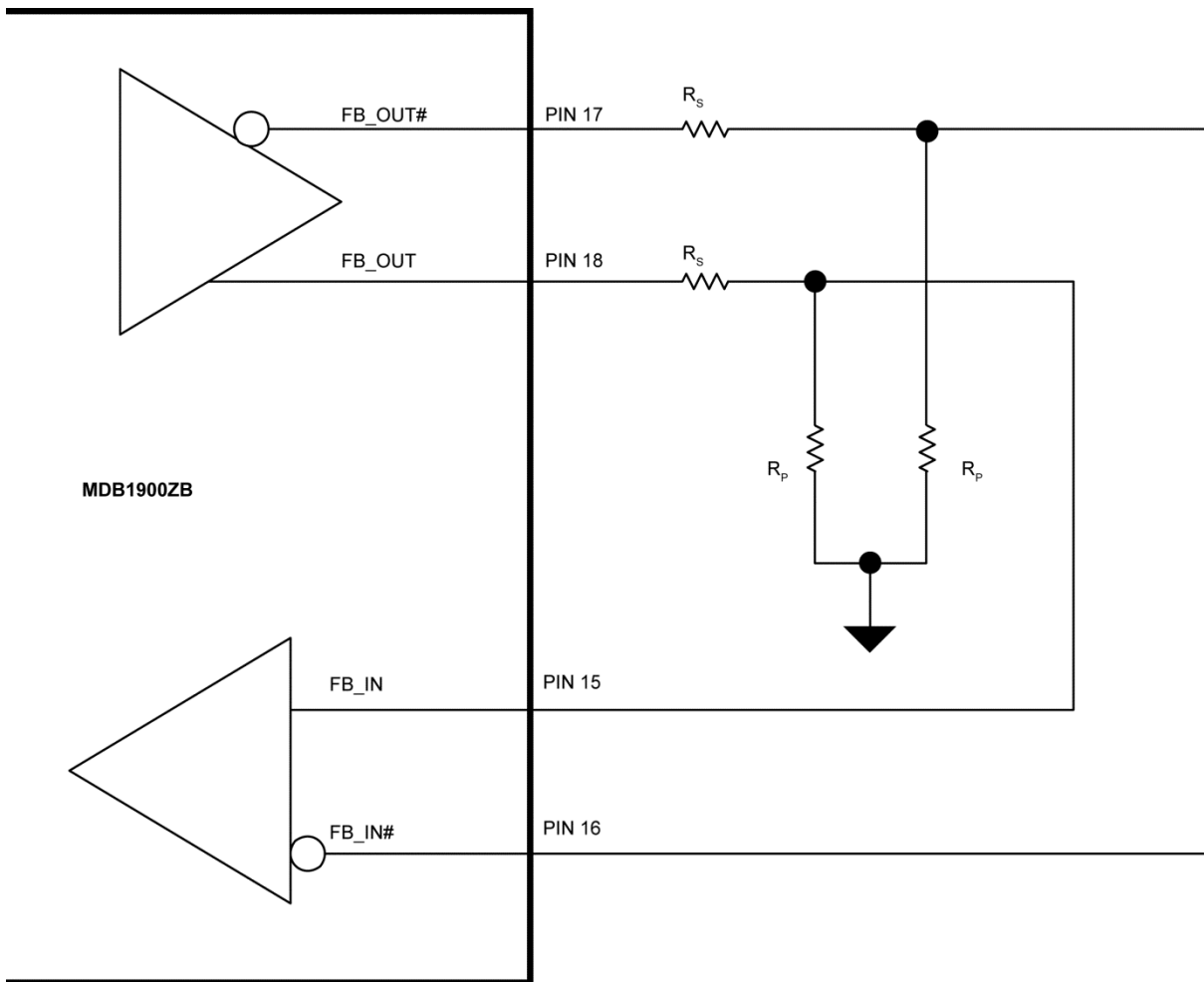
NOTE:
RESISTORS MUST BE LOCATED CLOSE TO FB_OUT AND FB_OUT# PINS.

Figure 1. External Feedback

Table 1. Feedback Series and Shunt Resistors

Board Table Impedance	R_S	R_P	Units
100	33 (5%)	49.9 (1%)	Ω
85	27 (5%)	42.2 (1%)	Ω

Measurements Points for Differential
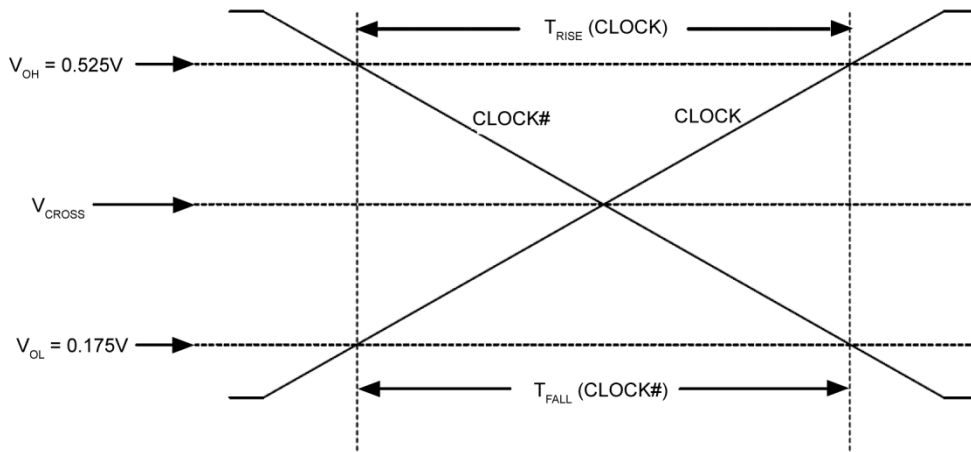
Figure 2. Single-Ended Measurement Points for T_{RISE} and T_{FALL}

$V_{OH} = 0.525V$

V_{CROSS}

$V_{OL} = 0.175V$

T_{RISE} (CLOCK)

CLOCK#   CLOCK

T_{FALL} (CLOCK#)
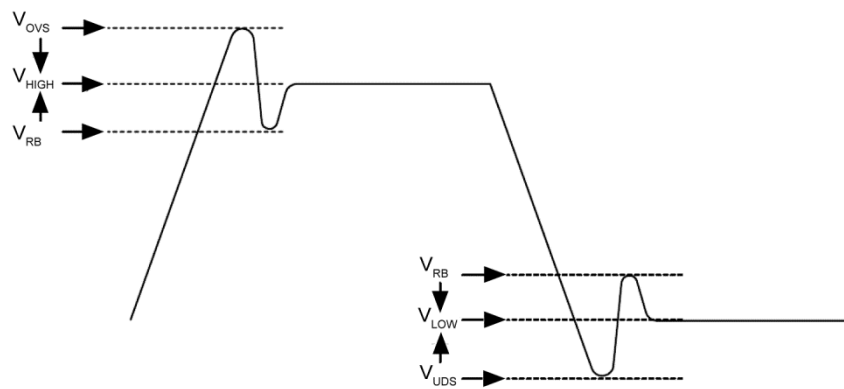
Figure 3. Single-Ended Measurement Points for V_{OVS}, V_{UDS}, and V_{RB}

V_{OVS}
V_{HIGH}
V_{RB}

V_{RB}
V_{LOW}
V_{UDS}
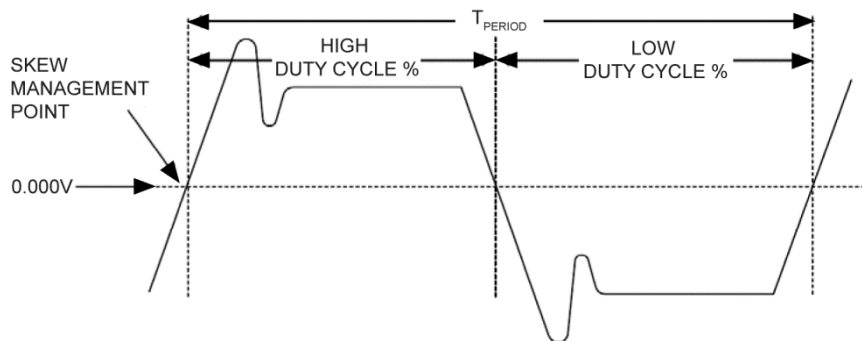
Figure 4. Differential (Clock/Clock#) Measurement Points for T_{PERIOD}, Duty Cycle, and Jitter

T_{PERIOD}

SKEW
MANAGEMENT
POINT

HIGH
DUTY CYCLE %

LOW
DUTY CYCLE %

0.000V

Termination of HCSL [DIF, DIF# (18:0)] Output Buffers for Testing Conditions

All differential output parameters are measured while driving 10in 100Ω or 85Ω differential impedance transmission line segments with 2pF load capacitors at the end of each segment. Measurements are taken across the 2pF load capacitor associated with Clock and Clock# as shown in Figure 5 and Figure 6. For resistive lumped load, board trace impedance and trace length refer to Table 3.

Table 2. I_{REF} and DIF Clock (HCSL) Output Current

Board Trace Impedance Z	Reference R_{IREF} I_{REF} = (1.1V) / (R_{IREF})	Output Current (mA)	V_{OH} at Z
100Ω	R_{IREF} = 475Ω (1%) I_{REF} = 2.32mA	I_{OH} = (6mA × I_{REF})	0.7V @ 50Ω
85Ω	R_{IREF} = 412Ω (1%) I_{REF} = 2.67mA	I_{OH} = (6mA × I_{REF})	0.7V @ 42.2Ω

Table 3. Resistive Lumped Test Loads for HCSL Differential Clocks

Clock	Board Trace Impedance	R_S	R_P	R_{IREF}	Units	Notes
Clocks (100MHz and 133.33MHz) with 50Ω configuration	100	33 (5%)	49.9 (1%)	475 (1%)	Ω	10in. (maximum) into 2pF load with 100Ω differential impedance.
Clocks (100MHz and 133.33MHz) with 42.5Ω configuration	85	27 (5%)	42.2 (1%)	412 (1%)	Ω	10in. (maximum) into 2pF load with 85Ω differential impedance.
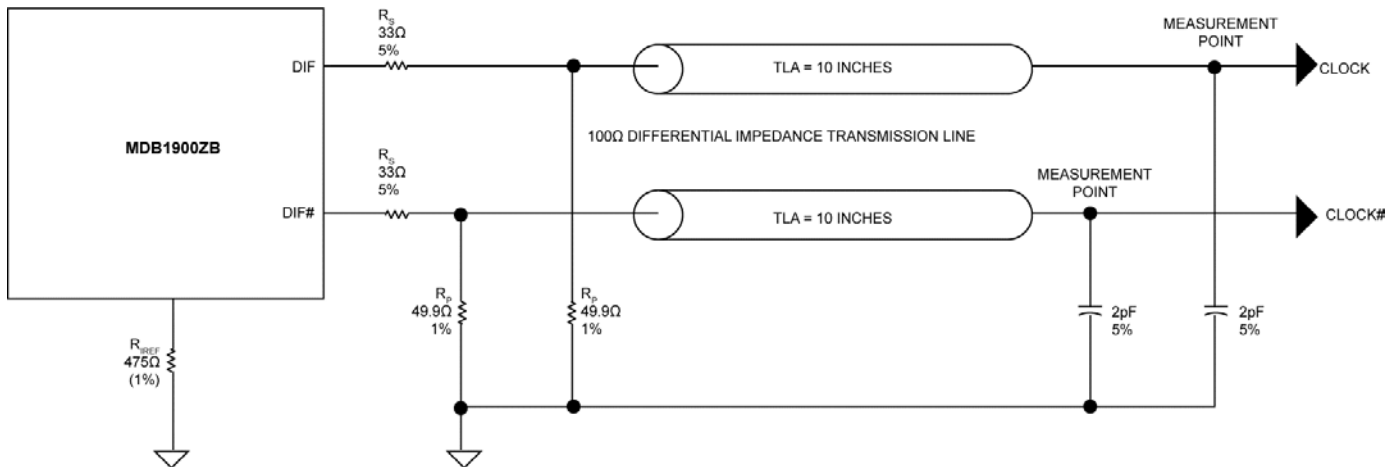
**Figure 5. 0.7V Configuration Test Load Board Termination
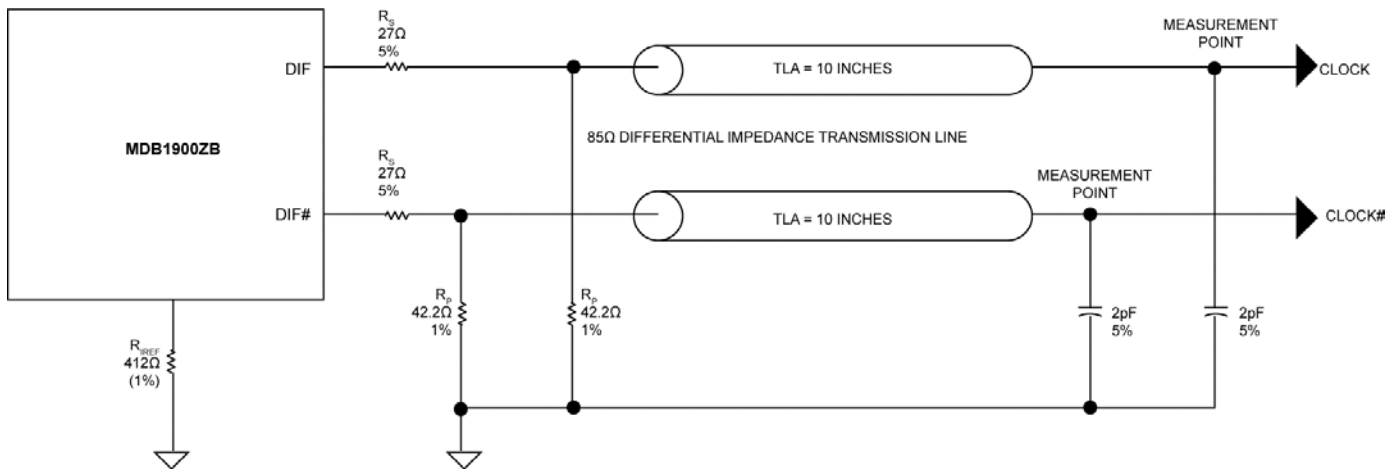with 100Ω Differential Impedance Transmission Line**

**Figure 6. 0.7V Configuration Test Load Board Termination
with 85Ω Differential Impedance Transmission Line**

Functional Description

CLK_IN, CLK_IN# Input Reference

The reference clock (CLK_IN, CLK_IN#) is an HCSL (0.7V) differential input with 100MHz or 133.33MHz frequency from CK410B+, CK509B or CK420BQ clock Synthesizer. The input (CLK_IN, CLK_IN#) has the option to have spread spectrum ON or spread spectrum OFF. The spread spectrum clocking (SSC) has modulation frequency value of 30kHz − 33kHz, with modulation of −0.5% down-spread (maximum). The modulation profile is Triangular or Lexmark.

OE# and Output Enables (Control Registers)

OE# pins are dedicated control pins for DIF [12:5] outputs and are asynchronous asserted-low signals. Each output can be individually enabled or disabled by SMBus control register bits. The output enable bits in the SMBus registers are active high and by default are set to enable.

OE# Assertion (Transition from Logic 1 to Logic 0)

All differential outputs that were tri-stated are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 4 − 12 DIF clock periods.

OE# De-Assertion (Transition from Logic 0 to Logic 1)

The impact of de-asserting OE# is each corresponding differential output will transition from normal operation to tri-state in a glitch free manner. A minimum of four valid clocks will be provided after OE# de-assertion. The maximum latency from the de-assertion to tri-stated outputs is twelve DIF clock periods.

Table 4. OE Functionality

Inputs		OE# Hardware Pins and Control Register Bits				Outputs	
PWRGD/ PWRGD#	CLK_IN/ CLK_IN#	SMBus Enable Bit	OE #	DIF/DIF#_ [12:5]	DIF/DIF#_ [18:13], [4:0]	FB_OUT/ FB_OUT#	PLL State
0	X	X	X	Hi-Z	Hi-Z	Hi-Z	ON
1	Running	0	X	Hi-Z	Hi-Z	Running	ON
		1	0	Running	Running	Running	ON
		1	1	Hi-Z	Running	Running	ON

100M_133M# (Frequency Selection)

The 100M_133M# is a hardware pin which programs the appropriate output frequency. The MDB1900ZB is operated in the 1:1 mode only; therefore the CLK_IN frequency is equal to DIF [18:0] frequency. The frequency selection can be enabled by 100M_133M# pin or by SMBus control register bit.

Note: The default frequency at power-up is 100MHz.

Table 5. Frequency Program

100M_133M#	Optimized Frequency (CLK_IN = DIF_[18:0]}
0	133.33MHz
1	100.00MHz (Default)

PWRGD / PWRDN#

De-assertion of PWRGD (Logic 0) which becomes PWRDN# indicates a power-down mode, which will shut off all clocks cleanly. PWRDN# is asynchronous active low input, and instructs the device to enter power saving mode. PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch-free manner, and all outputs will be tri-stated.

Table 6. PWRGD/PWRGDN# Functionality

PWRGD/ PWRGDN#	DIF_/DIF# [18.0]	Notes
0	Tri-State	Power-Down Mode
1	Normal	Active Mode

PWRGD Assertion

The power-up latency is less than 1.8ms. This is the time from the assertion of the PWRGD pin or the ramping of the power supply and the time from valid CLK_IN input clock until the time that stable clocks are output from the buffer chip (PLL locked).

The assertion and de-assertion of PWRDN# is absolutely asynchronous

Note: It is not recommended to disable (CLK_IN, CLK_IN#) input prior to assertion of PWRDN# and operation in this mode can result in glitches and excessive frequency shifting.
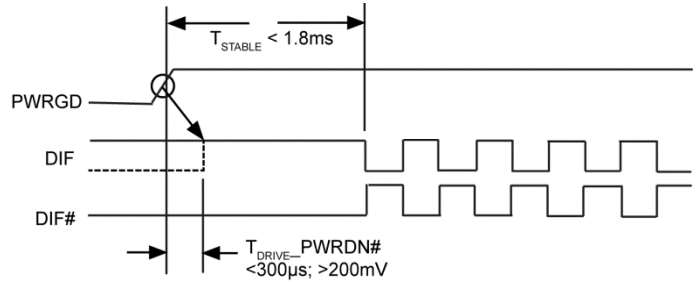

Figure 7. PWRGD Assertion (Power-Down De-Assertion)

PWRDN# Assertion

When PWRDN# is sampled as being asserted by two consecutive rising edges of DIF#, all differential outputs must be tri-stated on the next DIF# high-to-low transition.
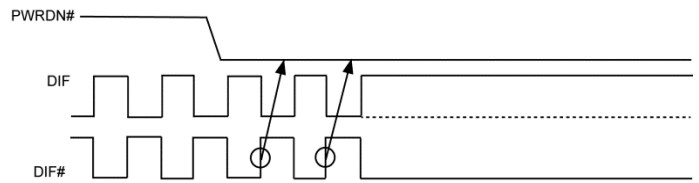

Figure 8. PWRDN# Assertion

HBW_BYPASS_LBW#

The HBW_BYPASS_LBW# is a tri-level function input pin. It is used to select between PLL high-bandwidth, bypass mode and PLL low bandwidth. The PLL HBW, BYPASS and PLL LBW mode may be selected via writing to SMBus register or by asserting the HBW_BYPASS_LBW input pin to the appropriate level per Table 7.

Table 7. PLL Bandwidth and Readback

HBW_BYPASS_LBW#	Mode	Byte 0, Bit 7	Byte 0, Bit 6
L (Low)	LBW (Low PLL Bandwidth)	0	0
M (Mid)	BYPASS (Bypass PLL)	0	1
H (High)	HBW (High PLL Bandwidth)	1	1

SA_0, SA_1 (Address Selection)

SA_0 and SA_1 are tri-level hardware pins that can configure the MDB1900ZB to nine different addresses.

Table 8. SA_0, SA_1, and SMBus Address

SA_1	SA_0	SMBus Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

MDB1900ZB Control Registers

SDA, SCL (Pins 12, 13)

The serial data (SDA) and serial clock (SCL) are dedicated for SMBus application and designed for 400Kb/s (maximum).

The SDA and SCL pins do not have internal pull-up resistors. When the device is in power-down mode, the SDA and SCL inputs are tri-stated and all programming information is retained.

All electrical characteristics meet the standard mode specifications of the SMBus 2.0 specification. For SDA and SCL input specs, refer to the *DC Electrical Characteristics*.

Table 9. Byte 0: Frequency Select, Output Enable, PLL-Mode Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	HBW_BYPASS_LBW# Mode 1	Refer to Table 4		R	Latched at Power-Up	5
6	HBW_BYPASS_LBW# Mode 0			R	Latched at Power-Up	5
5	Output Enable DIF, DIF#_18	Hi-Z	Enable	RW	1	71, 72
4	Output Enable DIF, DIF#_17	Hi-Z	Enable	RW	1	69, 70
3	Output Enable DIF, DIF#_16	Hi-Z	Enable	RW	1	66, 67
2	Reserved	–	–	–	–	–
1	Reserved	–	–	–	–	–
0	100M_133M# Frequency Select	133.33MHz	100MHz	R	Latched at Power-Up	4

Table 10. Byte 1: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Output Enable DIF, DIF#_[7]	Hi-Z	Enabled	RW	1	38, 39
6	Output Enable DIF, DIF#_[6]	Hi-Z	Enabled	RW	1	35, 36
5	Output Enable DIF, DIF#_[5]	Hi-Z	Enabled	RW	1	32, 33
4	Output Enable DIF, DIF#_[4]	Hi-Z	Enabled	RW	1	29, 30
3	Output Enable DIF, DIF#_[3]	Hi-Z	Enabled	RW	1	27, 28
2	Output Enable DIF, DIF#_[2]	Hi-Z	Enabled	RW	1	24, 25
1	Output Enable DIF, DIF#_[1]	Hi-Z	Enabled	RW	1	22, 23
0	Output Enable DIF, DIF#_[0]	Hi-Z	Enabled	RW	1	19, 20

Table 11. Byte 2: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Output Enable DIF, DIF#_[15]	Hi-Z	Enabled	RW	1	64, 65
6	Output Enable DIF, DIF#_[14]	Hi-Z	Enabled	RW	1	61, 62
5	Output Enable DIF, DIF#_[13]	Hi-Z	Enabled	RW	1	59, 60
4	Output Enable DIF, DIF#_[12]	Hi-Z	Enabled	RW	1	55, 56
3	Output Enable DIF, DIF#_[11]	Hi-Z	Enabled	RW	1	52, 53
2	Output Enable DIF, DIF#_[10]	Hi-Z	Enabled	RW	1	49, 50
1	Output Enable DIF, DIF#_[9]	Hi-Z	Enabled	RW	1	46, 47
0	Output Enable DIF, DIF#_[8]	Hi-Z	Enabled	RW	1	41, 42

Table 12. Byte 3: OE# Pin Real-time Readback Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Real-Time Readback of OE_12#	OE_5# Low	OE_5# High	R	Real-Time	57
6	Real-Time Readback of OE_11#	OE_6# Low	OE_6# High	R	Real-Time	54
5	Real-Time Readback of OE_10#	OE_7# Low	OE_7# High	R	Real-Time	51
4	Real-Time Readback of OE_9#	OE_8# Low	OE_8# High	R	Real-Time	48
3	Real-Time Readback of OE_8#	OE_9# Low	OE_9# High	R	Real-Time	43
2	Real-Time Readback of OE_7#	OE_10# Low	OE_10# High	R	Real-Time	40
1	Real-Time Readback of OE_6#	OE_11# Low	OE_11# High	R	Real-Time	37
0	Real-Time Readback of OE_5#	OE_12# Low	OE_12# High	R	Real-Time	34

Table 13. Byte 4: Reserved Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Reserved	–	–	–	–	–
6	Reserved	–	–	–	–	–
5	Reserved	–	–	–	–	–
4	Reserved	–	–	–	–	–
3	Reserved	–	–	–	–	–
2	Reserved	–	–	–	–	–
1	Reserved	–	–	–	–	–
0	Reserved	–	–	–	–	–

Table 14. Byte 5: Vendor/Revision Identification Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Revision Code Bit 3	–	–	R		–
6	Revision Code Bit 2	–	–	R	Vendor Specific (contact factory for details)	–
5	Revision Code Bit 1	–	–	R		–
4	Revision Code Bit 0	–	–	R		–
3	Vendor ID Bit 3	–	–	R	0	–
2	Vendor ID Bit 2	–	–	R	0	–
1	Vendor ID Bit 1	–	–	R	1	–
0	Vendor ID Bit 0	–	–	R	1	–

Table 15. Byte 6: Device ID Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Device ID 7 (MSB)			R	1	–
6	Device ID 6			R	1	–
5	Device ID 5			R	0	–
4	Device ID 4	Device ID is 0xDB (Hex), or 219 (Decimal)		R	1	–
3	Device ID 3			R	1	–
2	Device ID 2			R	0	–
1	Device ID 1			R	1	–
0	Device ID 0			R	1	–

Byte 7: Byte Count Register

Writing to bits [0:4] of Byte 7 configures how many bytes will be read back.

Table 16. Byte 7: Byte Count Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Reserved	–	–	–	–	–
6	Reserved	–	–	–	–	–
5	Reserved	–	–	–	–	–
4	BC4	–	–	RW	0	–
3	BC3	–	–	RW	1	–
2	BC2.	–	–	RW	0	–
1	BC1	–	–	RW	0	–
0	BC0	–	–	RW	0	–

Byte 8, 9, 10: Access and Controls for Optional Advanced Features

Registers 8, 9, and 10 are additional Micrel-defined registers to allow access to and control of optional advanced features. For optional features details, please see the *Optional Features* section.

Optional advanced features use a two level read or write access, wherein the first step is to enter an access code in Byte 8, followed by entering a feature's bit address in Byte 9, and then reading or writing control information in Byte 10.

Byte 8: Advanced Features Access Register

This is a write-only register which defines the access to Register 9 and 10. When value 0xBB('1011'1011) is written to Register 8, then Registers 9 and 10 become accessible. Otherwise, Registers 9 and 10 cannot be either read or written.

Table 17. Byte 8: Advanced Features Access Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	access[7]	–	–	W	–	–
6	access[6]	–	–	W	–	–
5	access[5]	–	–	W	–	–
4	access[4]	–	–	W	–	–
3	access[3]	–	–	W	–	–
2	access[2]	–	–	W	–	–
1	access[1]	–	–	W	–	–
0	access[0]	–	–	W	–	–

Byte 9: Features Bits Address Register

Each optional feature has an associate set of bits and each bit has a unique address. For details of optional features and their associated bit addresses, please see the *Optional Features* section. In order to access a bit, its address has to be written to Register 9.

Table 18. Byte 9. Features Bits Address Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	fbitaddr[7]	–	–	RW	–	–
6	fbitaddr[6]	–	–	RW	–	–
5	fbitaddr[5]	–	–	RW	–	–
4	fbitaddr[4]	–	–	RW	–	–
3	fbitaddr[3]	–	–	RW	–	–
2	fbitaddr[2]	–	–	RW	–	–
1	fbitaddr[1]	–	–	RW	–	–
0	fbitaddr[0]	–	–	RW	–	–

Table 19. Byte 10: Optional Advanced Features Bits Command Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Pin(s)
7	Write Enable	–	–	W	–	–
6	Feature Bit State (Read)	–	–	R	–	–
5	Reserved	–	–	–	–	–
4	Reserved	–	–	–	–	–
3	Reserved	–	–	–	–	–
2	Reserved	–	–	–	–	–
1	Feature Bit State (Write)	–	–	W	–	–
0	Reserved	–	–	–	–	–

Byte 10: Features Bits Command Register

To read or write a feature bit value, first write the 1011 1011 access code to byte 8 followed by the feature bit address to byte 9. The current value of the feature bit will appear in bit 6 of byte 10, where it can be read. To write the value of the feature bit, write the desired value into bit 1 of byte 10 and also set bit 7 of byte 10 to '1' to enable the writing. Next, write '0000 0000' to byte 10 to close writing before changing to another address in byte 9.

Feature Bit Commands

READ: To Read a Current Feature Bit Value

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10).

2. Write the feature bit address to Register 9.

3. Read Register 10, the feature bit state is available in bit 6 of register 10.

Example 1

To read the LSB of the delay on CLK_IN path (delay_clkin[0], Address 132):

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10).

2. Write '1000'0100 to Register 9 (Address 132).

3. Read Register 10, Bit 6 for the value of delay_clkin[0].

Example 2

To read the MSB of output0 (Out0trim[3], Address 143, Default 1):

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10).

2. Write '1000'1111 to Register 9 (Address 143).

3. Read Register 10, Bit 6 for the value of Out0trim[3].

WRITE: To change the Value of a Feature Bit

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10).

2. Write the feature bit address to Register 9.

3. Write '1000'00s0 to Register 10, where s is the feature bit value ('0' or '1').

4. Write '0000'0000 to Register 10 to close the write command.

Example 1

To set (write) the LSB of the delay on CLK_IN path to 1 (delay_clkin[0], Address 132):

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10).

2. Write '1000'0000 to Register 9 (Address 132).

3. Write '1000'0010 to Register 10 for delay_clkin[0]=1 or '1000'0000 for delay_clkin[0]=0.

4. Write '0000'0000 to Register 10.

Example 2

To set (write) the MSB of output0 to 0 (Out0trim[3], Address 143, Default 1).

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10).

2. Write '1000'1111 to Register 9 (Address 143).

3. Write '1000'0010 to register 10 for Out0trim[3]=1 or '1000'0000 for Out0trim[3]=0.

4. Write '0000'0000 to Register 10.
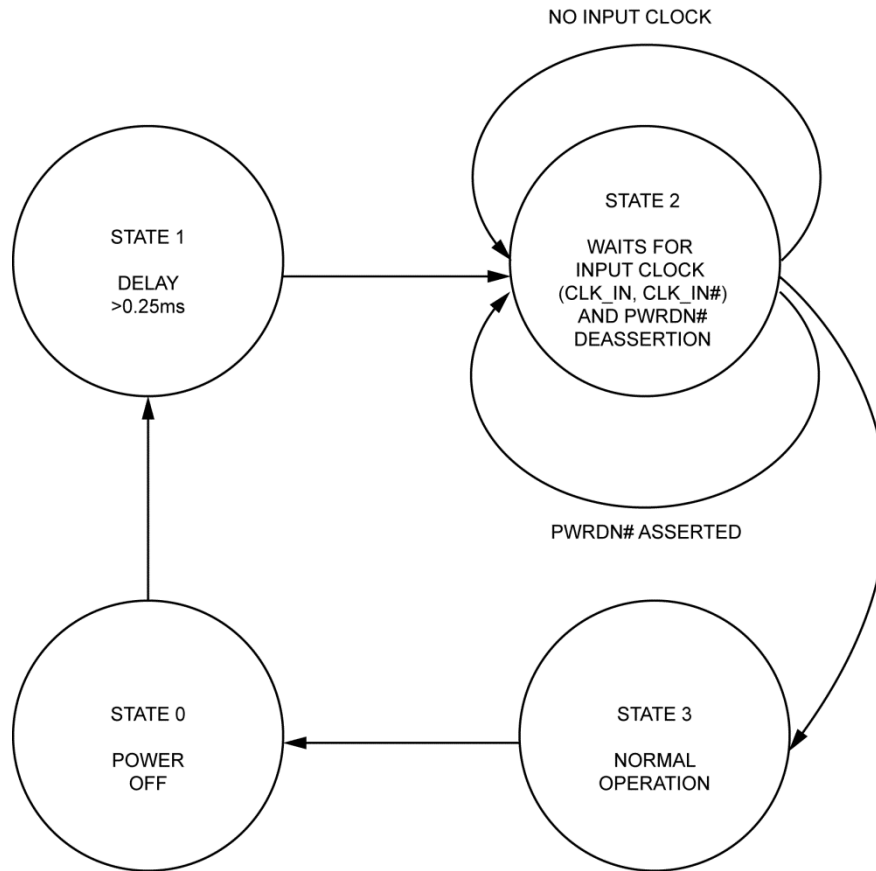
Figure 9. Buffer Power-Up State Diagram

Table 20. Buffer Power-Up State Machine

State	Description
0	Buffer power off.
1	After supply is detected to rise above 1.8 V - 2.0 V, the buffer enters (state 1) and initiates (>0.25ms - 0.3ms) delay.
2	Buffer waits for a valid (CLK_IN, CLK_IN#) and PWRDN# de-assertion.
3	After the PLL locked to input reference (CLK_IN, CLK_IN#), the buffer enters (State 3) and enables all outputs for normal operation. The total power-up latency is < 1.8ms (assuming a valid clock is present on (CLK_IN, CLK_IN#) input. If power is valid and PWRDN# is de-asserted but no input (CLK_IN, CLK_IN#), therefore all DIF,DIF#_[18:0] remain disabled. Only after input clock is detected, valid power, PWRDN# de-asserted with the PLL locked/stable and the DIF, DIF# are enabled.

Optional Features

The MDB1900ZB is 100% compatible with the Intel DB1900Z specification document and can be used in any application where that part is called for. However, Micrel has made available optional features that are largely enabled through three additional registers (Registers 8, 9, and 10). These optional features allow for significant power savings and for coping with PCB manufacturing variability.

2.5V Operation

In addition to the 3.3V (±5%) operation voltage called for by the Intel specification, the MDB1900ZB supports 2.5V (±5%) operation voltage. No changes to registers or power supply filtering components are required to use this feature. Simply connect a 2.5V supply where the 3.3V supply is specified and the part will continue to work correctly, including all output voltages and levels. Switching to 2.5V from 3.3V will save approximately 25% in total power dissipation for this part.

Zero Delay Optimization

The MDB1900ZB has excellent zero delay characteristics that are far better than required by the Intel specification. However, the exact value of the zero delay is partially dependent on the external feedback path and this can vary with the PCB board design and with manufacturing variations in the PCB. To compensate for errors in the PCB design or to relax the manufacturing tolerance required from the PCB board vendor, Micrel has provided the ability to independently add delay into either or both the CLK_IN path and the FB_IN path (see Table 21 and

Table 22).

Table 21. Feature Bit Address [135:132] ≥ DELAY_CLKIN[3:0]

DELAY_CLKIN[3:0]	Additional Delay in CLK_IN Path (Typical Value with Respect to Default)	Unit
'0000 (Default)	–	ps
'0001	18	ps
'0010	29	ps
'0011	50	ps
'0100	68	ps
'0101	88	ps
'0110	101	ps
'0111	121	ps
'1000	141	ps
'1001	163	ps

Table 22. Feature Bit Address [139:136] ≥ DELAY_FB[3:0]

DELAY_FB[3:0]	Additional Delay in FB_IN Path (Typical Value with Respect to Default)	Unit
'0000 (Default)	–	ps
'0001	18	ps
'0010	29	ps
'0011	50	ps
'0100	68	ps
'0101	88	ps
'0110	101	ps
'0111	121	ps
'1000	141	ps
'1001	163	ps

Input Signal Pin Capacitance

The zero delay value is defined not only by the external feedback path but also by the input pin capacitance driven by that feedback path. The input pin capacitance is allowed by the Intel specification to be within a fairly broad range. The Micrel part is always within the low end of the allowed range ensuring a low capacitive load and sharp edge rates. However, the user can adjust the MDB1900ZB so that it presents a larger input capacitance load at CLK_IN, CLK_IN#, FB_IN, FB_IN#.

This feature can be used to ensure compatibility with third-party vendors who can still meet the Intel specification, but have significantly different input capacitances (see Table 23 and Table 24).

Table 23. Feature Bit Address [218:216] ≥ INPUT_CAP_CLKIN[2:0]

INPUT_CAP_CLKIN[2:0]	Input Capacitance (Typical Value)	Unit
'000 (Default)	2.46	pF
'001	2.82	pF
'010	3.24	pF
'011	3.58	pF
'100	4.02	pF
'101	4.34	pF
'110	4.77	pF
'111	5.12	pF

Table 24. Feature Bit Address [221:219] ≥ INPUT_CAP_FBIN[2:0]

INPUT_CAP_FBIN[2:0]	Input Capacitance (Typical Value)	Unit
'000 (Default)	2.46	pF
'001	2.82	pF
'010	3.24	pF
'011	3.58	pF
'100	4.02	pF
'101	4.34	pF
'110	4.77	pF
'111	5.12	pF

Bypass Delay

The Intel specification calls for a fairly long delay of 2.5ns when the PLL is in bypass mode. The MDB1900ZB fully meets this specification in default mode. However, if the user wishes to have a much shorter bypass delay of 0.9ns this feature can be enabled.

Output Drive Levels

The Intel specification calls for very specific current drive levels on each of the HCSL outputs based on whether the part is driving 85Ω traces or 100Ω traces.

The specification calls for all enabled outputs to drive at the same current level. However, the MDB1900ZB allows the user to independently control the current drive to each output. This feature can be used to selectively save power on lightly loaded or short traces where V_{OH}, V_{OL} and edge rate can readily be met with reduced current without impacting other traces.

Table 25. Feature Bit Address [222] ≥ DELAY_BYPASS

Delay Bypass	Input-to-Output Delay – PLL Bypass Mode (Typical Value)	Unit
'0 (Default)	2.5	ns
'1	0.9	ns

Table 26. Feature Bit Address [215:140] ≥ Output Drive Level

Output	Feature Bit Address	Feature Bits
0	Address[143:140]	Out0trim[3:0]
1	Address[147:144]	Out1trim[3:0]
2	Address[151:148]	Out2trim[3:0]
3	Address[155:152]	Out3trim[3:0]
4	Address[159:156]	Out4trim[3:0]
5	Address[163:160]	Out5trim[3:0]
6	Address[167:164]	Out6trim[3:0]
7	Address[171:168]	Out7trim[3:0]
8	Address[175:172]	Out8trim[3:0]
9	Address[179:176]	Out9trim[3:0]
10	Address[183:180]	Out10trim[3:0]
11	Address[187:184]	Out11trim[3:0]
12	Address[191:188]	Out12trim[3:0]
13	Address[195:192]	Out13trim[3:0]
14	Address[199:196]	Out14trim[3:0]
15	Address[203:200]	Out15trim[3:0]
16	Address[207:204]	Out16trim[3:0]
17	Address[211:208]	Out17trim[3:0]
18	Address[215:212]	Out18trim[3:0]

Table 27. Output Drive Level, Output Trim Feature Bits Definition (also refer to Table 26)

Output Trim Feature Bits [3:0]	Output Drive Level (Relative to Default)	Output Current 100Ω Loads (mA)	Output Current 85Ω Loads (mA)
'0000 (Default)	100%	14.0	16.0
'0001	90%	12.6	14.4
'0011	80%	11.2	12.8
'0100	70%	9.8	11.2
'0110	60%	8.4	9.6
'0111	50%	7.0	8.0
'1010	40%	5.6	6.4
'1011	30%	4.2	4.8
'1100	20%	2.8	3.2
'1110	10%	1.4	1.6
'1111	0%	0.0	0.0

Example of Setting Output 1 to 60% Strength (change from default 100%)

Feature Bits: out1trim[3:0], address[147:144]

In order to set output1 to 60% strength, out1trim[3:0] needs to be '0110. Therefore, feature bits 145 and 146 need to be inverted:

1. Write '1011'1011 to Register 8 (to enable Register 9 and 10)
2. Write '1001'0001 to Register 9 (Feature Bit 145)
3. Write '1000'0010 to Register 10 (set Feature Bit 145 to 1)
4. Write '0000'0000 to Register 10
5. Write '1001'0010 to Register 9 (Feature Bit 146)
6. Write '1000'0010 to Register 10 (set Feature Bit 146 to 1)
7. Write '0000'0000 to Register 10

Package Information and Recommended Land Pattern[41]
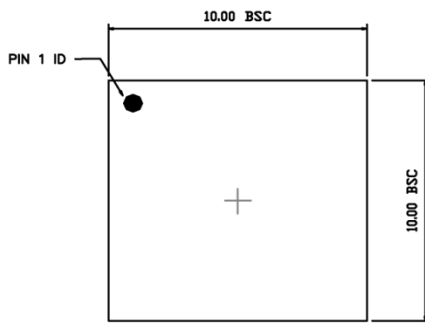
TOP VIEW
NOTE: 1, 2, 3
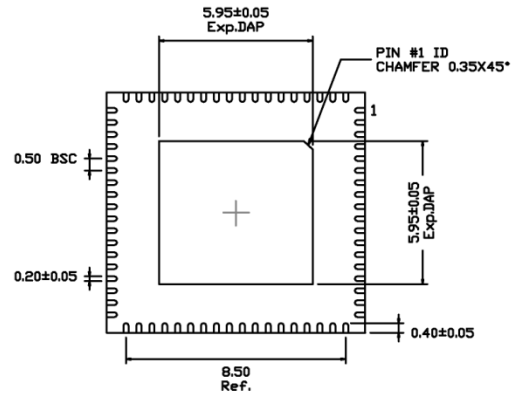
BOTTOM VIEW
NOTE: 1, 2, 3
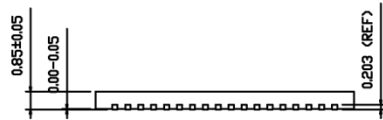
SIDE VIEW
NOTE: 1, 2, 3
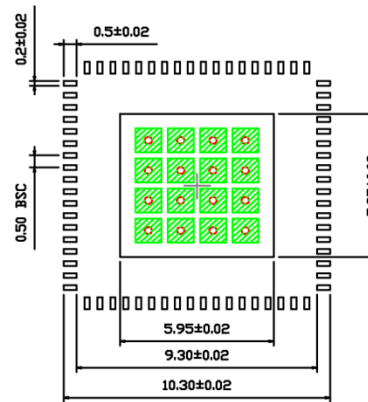
RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARK.
4. RED CIRCLES IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.3mm IN DIAMETER AND
SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.0MM PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA.
RECOMMENDED SIZE IS 1.0x1.0mm, SPACING IS 0.25mm.

Note: