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# Clocks for NXP QorIQ and Layerscape CPUs

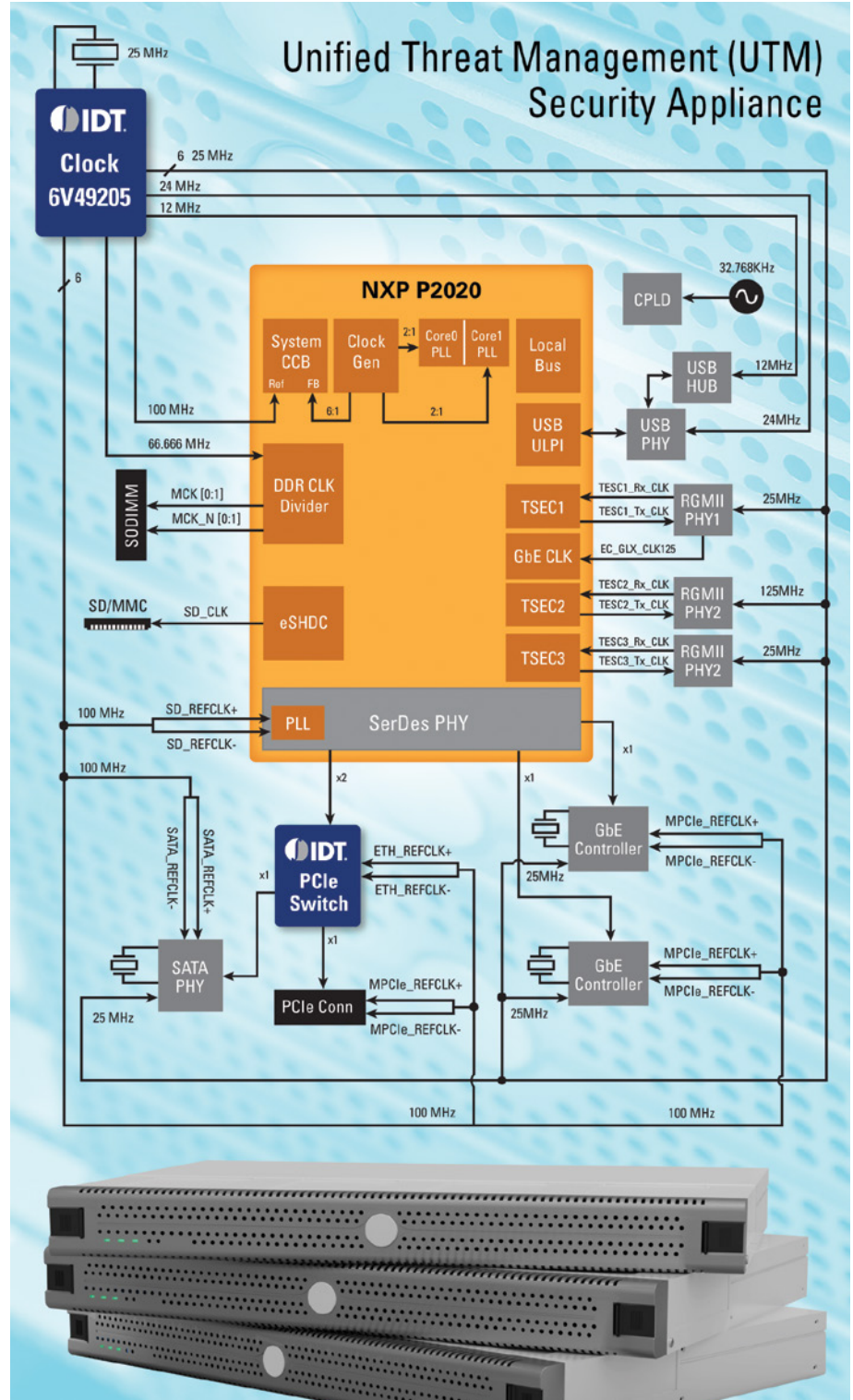
IDT has the industry's broadest portfolio of timing solutions for industrial, networking, consumer and embedded applications. With products uniquely complementing the NXP™ QorIQ™ and Layerscape™ processors, IDT provides the performance, flexibility, design expertise, reliability and manufacturing capabilities to ensure customer success.

### All-in-One Clock Solutions

- Spread-spectrum capable for EMI reduction
- Highly integrated single-chip solutions replace up to
  - 11 crystals
  - 2 oscillators
  - 3 clock synthesizers
- Low-power PCIe® outputs with integrated terminations
- PCIe Gen1/2/3 compliant PCIe outputs
- < 700fs RMS phase jitter
- Signal integrity tuning
- As little as 400mW power dissipation

### Building Block Clock Solutions

- Mix and match various clocks to support desired frequencies and data rates
- Clock generators
  - System and DDR clocks
  - SERDES clocks for PCIe Gen1-4 and 100GbE
- Clock distribution
  - Fanout buffers with < 50fs RMS additive phase jitter
  - PCIe fanout and zero delay buffers for PCIe Gen1-4
  - PCIe clock multiplexers for PCIe Gen1-4
  - Supports HCSL, HSTL, LVPECL, LVDS and LVCMOS signaling standards





# Clocks for NXP QorIQ and Layerscape CPUs

Selecting clocks for QorIQ designs is straightforward. Once the “Qor” clocking requirements of the NXP QorIQ processors are satisfied (SYS\_CCB clock, etc.), product selection proceeds to other required clocks, such as USB or 25M for Ethernet. Then the desired data rates, frequencies and number of SERDES links are factored into the clock selection. IDT offers both integrated and building block approaches to QorIQ timing solutions as shown in the product selector tables.

Clocking Solutions for NXP QorIQ and Layerscape Processors								
“All-in-One” Clock Solutions								
	NXP Clock Modes (only 1 at a time is used)			Other Clocks			SERDES Clock Pairs	
Part Number	SYS_CLK/ DDR_CLK	DIFSYS_CLK	PS_XI	GTX_CLK	USB_CLK (MHz)	Other LVCMOS Outputs (MHz)	Pairs (MHz)	App Jitter Compliance
6V49205	Yes	Yes	Yes (24M Only)	Yes	2 x 12/24	6 x 25 2 x 2.048	6 x 100/125	PCIe Gen1-2, SGMII, sRIO 1x-2x SATA/SATA3G
5P49V5907			Yes		4 x 50 - 167	PCIe Gen1-3, SGMII 1x-2.5x, sRIO 1x-2x SATA/SATA3G, XAUI, XAUI 10G		
5P49V5908			Yes		8 x 50 - 167			
“Building Block” Clock Generators								
Part Number	SYS_CLK/ DDR_CLK	DIFSYS_CLK	PS_XI	GTX_CLK	USB_CLK (MHz)	Other LVCMOS Outputs (MHz)	Pairs (MHz)	App Jitter Compliance
5P30521	Yes	Yes	Yes	Yes	Yes	1 x 32.768KHz	2 x 1 - 500	PCIe Gen1-3
5P30523						1 x REF	4 x 1 - 350	500fs RMS
5P49V69xx							-	-
840S07		No	No		-	-	-	-
MP9855					-	2x 25	-	-
840NT4	-	-	-	-	-	1 x 25 1 x 3.125 1 x 1.5625	-	-
840NT4-01	-	-	-	-	1 x 24	1 x 25 8 x 125	-	-
8T49N222	-	-	-	-	-	-	2 x 7.7 - 1200	300fs RMS
8T49N004	-	-	-	-	-	-	4 x 15.16 - 1250	212fs RMS
8T49N006	-	-	-	-	-	-	6 x 15.16 - 1250	
8T49N008	-	-	-	-	-	-	8 x 15.16 - 1250	
8T49N012	-	-	-	-	-	-	12 x 15.16 - 1250	
8T49NS0312	-	Yes	Yes	-	-	-	12 x 10.9 - 2500	89fs RMS



# Clocks for NXP QorIQ and Layerscape CPUs

"Building Block" Non-PLL Fanout Buffers and Multiplexers (< 50fs RMS additive phase jitter)									
Part Number	Inputs (#)	Input Type	Outputs (#)	Output Type	Output Freq (MHz)	Input Freq (MHz)	Core Supply (V)	Output Supply (V)	
5PB1104	1	LVCMOS	4	LVCMOS	0 - 200	0 - 200	1.8, 2.5, 3.3	1.8, 2.5, 3.3	
5PB1106			6						
5PB1108			8						
5PB1110			10						
8312I			12						
8P34S1102I		CML, LVDS, LVPECL	2	LVDS	0 - 1200	0 - 1200	1.8	1.8	
8P34S1106i			6						
8SLVP1102I			2	LVPECL	0 - 2000	0 - 2000	2.5, 3.3	2.5, 3.3	
8SLVP1104I			4						
8530-01		HCSL, HSTL, LVDS, LVPECL, SSTL	16	LVPECL	0 - 500	0 - 500	3.3	3.3	
8SLVP2102I	CML, LVDS, LVPECL	4	0 - 2000		0 - 2000	2.5, 3.3	2.5, 3.3		
8SLVP2104I		8							
8SLVP2106I	LVDS, LVPECL	12							
8SLVP2108I	LVPECL	16							
8T39S04A	3	Xtal, HCSL, HSTL, LVCMOS, LVDS, LVPECL						4	HCSL, LVDS, LVPECL
8T39S06A								6	
8T39S08A								8	

"Building Block" PCI Express Clock Generators (LP-HCSL outputs)								
Part Number	Input (MHz)	Spread Spectrum Support	Outputs (#)	Operating Frequency (MHz)	Lead Count (#)	Package Size (mm)	Supply Voltage (V)	App Jitter Compliance
9FGV0241	25	Yes	2	100	24	4 x 4	1.8	PCIe Gen1-4
9FGV0441			4		32	5 x 5		
9FGV0641			6		40	5 x 5		
9FGV0841			8		48	6 x 6		
9FGL0241			2		24	4 x 4	3.3	
9FGL0441			4		32	5 x 5		
9FGL0641			6		40	5 x 5		
9FGL0841			8		48	6 x 6		

"Building Block" non-PLL Fanout Buffers and Multiplexers (HCSL inputs and LP-HCSL outputs)								
Part Number	Inputs	Spread Spectrum Support	Outputs (#)	Operating Frequency (MHz)	Lead Count (#)	Package Size (mm)	Supply Voltage (V)	App Jitter Compliance
9DBV0541	1	Yes	5	1 - 200	32	5 x 5	1.8	PCIe Gen1-4
9DBV0741			7		40	5 x 5		
9DBV0941			9		48	6 x 6		
9DMV0141	2		1		16	3 x 3		
9DMV0441			4		24	4 x 4		
9DBL0741	1		7		40	5 x 5	3.3	
9DBL0941			9		48	6 x 6		
9DMV0441			2		4	24		



# Clocks for NXP QorIQ and Layerscape CPUs

"Building Block" PCI Express PLL Zero-Delay Buffers (HCSL inputs and LP-HCSL outputs)								
Part Number	Inputs	Spread Spectrum Support	Outputs (#)	Operating Frequency (MHz)	Lead Count (#)	Package Size (mm)	Supply Voltage (V)	App Jitter Compliance
9DBV0241	1	Yes	2	30 - 175	24	4 x 4	1.8	PCIe Gen1-4
9DBV0441			4		32	5 x 5		
9DBV0641			6		40	5 x 5		
9DBV0841			8		48	6 x 6		
9DBL0242			2		24	4 x 4	3.3	
9DBL0442			4		32	5 x 5		
9DBL0641			6		40	5 x 5		
9DBL0841			8		48	6 x 6		

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