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Differential-to-0.7V Differential PCI Express™ Jitter Attenuator

ICS871S1022

DATA SHEET

General Description

IDT's PLL-based clock generators offer sub-picosecond jitter, low-skew clock outputs, and edge rates that meet the ever-growing demands of today's networking solutions.

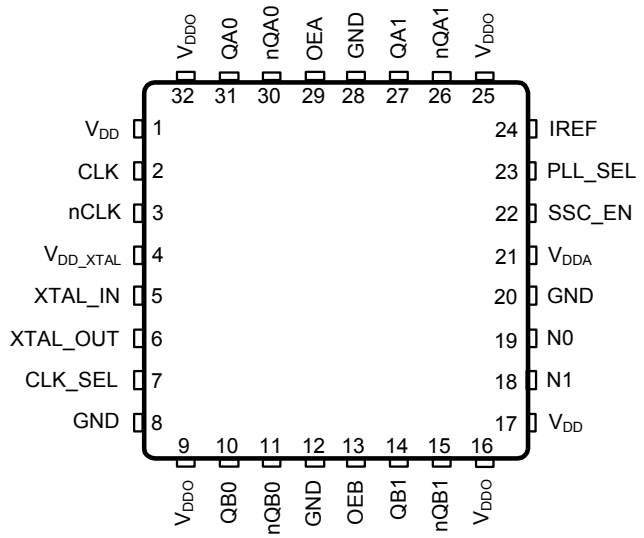
The ICS871S1022 is a PLL-based clock generator specifically designed for PCI Express Clock Generation applications. The device generates 100MHz, 125MHz, 250MHz or 500MHz from either a 25MHz fundamental mode crystal or a 100MHz recovered clock.

The ICS871S1022 has two modes of operation: (1) high frequency jitter attenuator and (2) high performance clock synthesizer mode. When in jitter attenuator mode, the ICS871S1022 is able to both suppress high frequency noise components and function as a frequency translator. Designed to receive a jittery and noisy clock from an external source, the ICS871S1022 uses FemtoClock® technology to clean up the incoming clock and translate the frequency to one of the four common PCI Express frequencies. When in synthesizer mode, the device is able to generate high performance SSC and non-SSC clocks from a low cost external, 25MHz, fundamental mode crystal. The ICS871S1022 uses FemtoClock® technology to generate low noise clock outputs capable of providing the seed frequencies for the common PCI Express link rates.

Features

- Four 0.7V differential output pairs
- One differential clock input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- RMS phase jitter @ 100MHz, using a 25MHz crystal (12kHz – 20MHz): 0.608ps (typical)
- High frequency jitter attenuator mode has high PLL bandwidth which allows for better input tracking
- Supports PCI Express Spread-Spectrum Clocking
- PCI Express Gen 1, 2 and 3 jitter compliant
- 3.3V operating supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Block Diagram

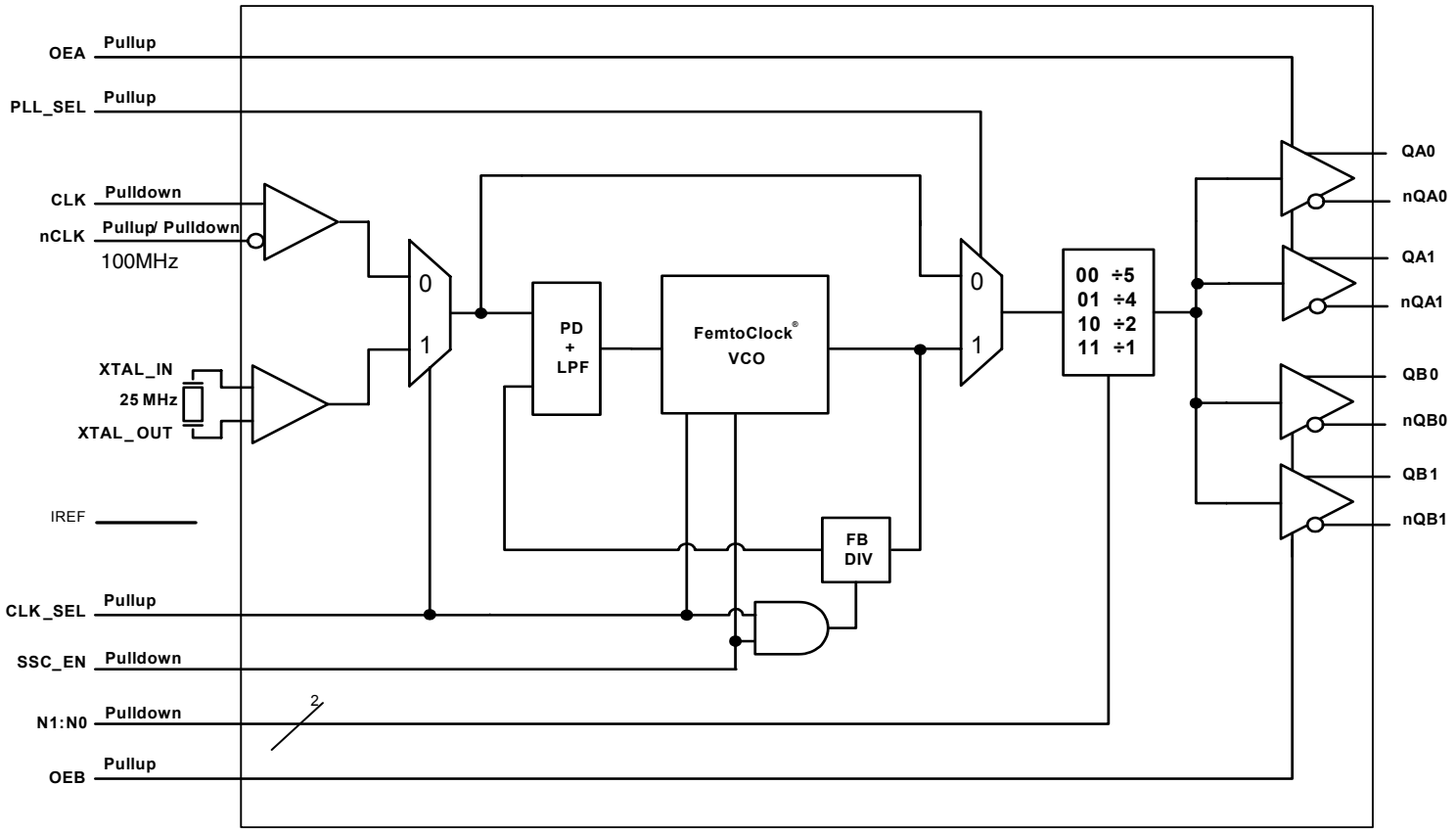


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 17	V_{DD}	Power		Core supply pins.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD}/2$.
4	V_{DD_XTAL}	Power		Crystal oscillator supply pin.
5, 6	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended or differential reference clock.
7	CLK_SEL	Input	Pullup	Input source control pin and device operation control pin. See Table 3C. LVCMOS/LVTTL interface levels.
8, 12, 20, 28	GND	Power		Power supply ground.
9, 16, 25, 32	V_{DDO}	Power		Output power supply pins.
10, 11	QB0, nQB0	Output		Differential output pair. HCSL interface levels.
13	OEB	Input	Pullup	Output enable pin for QB, nQB[0:1] pins. When HIGH, the outputs are active. When LOW, the outputs are in high-impedance state. See Table 3A. LVCMOS/LVTTL interface levels.
14,15	QB1, nQB1	Output		Differential output pair. HCSL interface levels.
18, 19	N1, N0	Input	Pulldown	Output divider control pins. See Table 3D for additional information. LVCMOS/LVTTL interface levels.
21	V_{DDA}	Power		Analog supply pin.
22	SSC_EN	Input	Pulldown	SSC enable pin. See Table 3B. LVCMOS/LVTTL interface levels.
23	PLL_SEL	Input	Pullup	PLL Bypass control pin. LVCMOS/LVTTL interface levels.
24	IREF	Output		HCSL current reference resistor output. An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
26, 27	nQA1, QA1	Output		Differential output pair. HCSL interface levels.
29	OEA	Input	Pullup	Output enable pin for QA, nQA[0:1] pins. When HIGH, the outputs are active. When LOW, the outputs are in a high-impedance state. See Table 3A. LVCMOS/LVTTL interface levels.
30, 31	nQA0, QA0	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			5		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Inputs	Outputs	
OEA, OEB	**QA[0:1], nQA[0:1]**	**QB[0:1], nQB[0:1]**
0	High-Impedance	High-Impedance
1	Enabled	Enabled

Table 3B. SSC Enable Function Table

Inputs	Outputs
SSC_EN	**Qx[0:1], nQx[0:1]**
0	SSC Disabled
1	-0.37% downspread

Table 3C. CLK_SEL Function Table

Input		
CLK_SEL	**Reference**	**Mode**
0	CLK, nCLK	High Frequency Jitter Attenuator
1	XTAL_IN, XTAL_OUT	Clock Synthesizer

Table 3D. Output Frequency Configuration Table

Inputs				Output Frequency (MHz)
CLK_SEL	**Input Frequency (MHz)**	**N1:N0**	**N Divider Value**	
0	100	00	5	100
0	100	01	4	125
0	100	10	2	250
0	100	11	1	500
1	25	00	5	100
1	25	01	4	125
1	25	10	2	250
1	25	11	1	500

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD_XTAL} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	39.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = V_{DD_XTAL} = V_{DDO} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DD_XTAL}	Crystal Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.18	3.3	V_{DD}	V
V_{DDO}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				100	mA
I_{DD_XTAL}	Crystal Supply Current				7	mA
I_{DDA}	Analog Supply Current				18	mA
I_{DDO}	Output Supply Current				27	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = V_{DD_XTAL} = V_{DDO} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SSC_EN, N0, N1	V_{DD} = V_{IN} = 3.465V			150	µA
		OEA, OEB, PLL_SEL, CLK_SEL	V_{DD} = V_{IN} = 3.465V			10	µA
I_{IL}	Input Low Current	SSC_EN, N0, N1	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		OEA, OEB, PLL_SEL, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DD\_XTAL} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-10			µA
		nCLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. PCI Express Jitter Specifications, $V_{DD} = V_{DD\_XTAL} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	f = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2), SSC_EN = 0		7.640	11.167	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2), SSC_EN = 0		0.619	1.094	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz, SSC_EN = 0		0.084	0.138	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	f = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2), SSC_EN = 0		0.120	0.241	0.8	ps

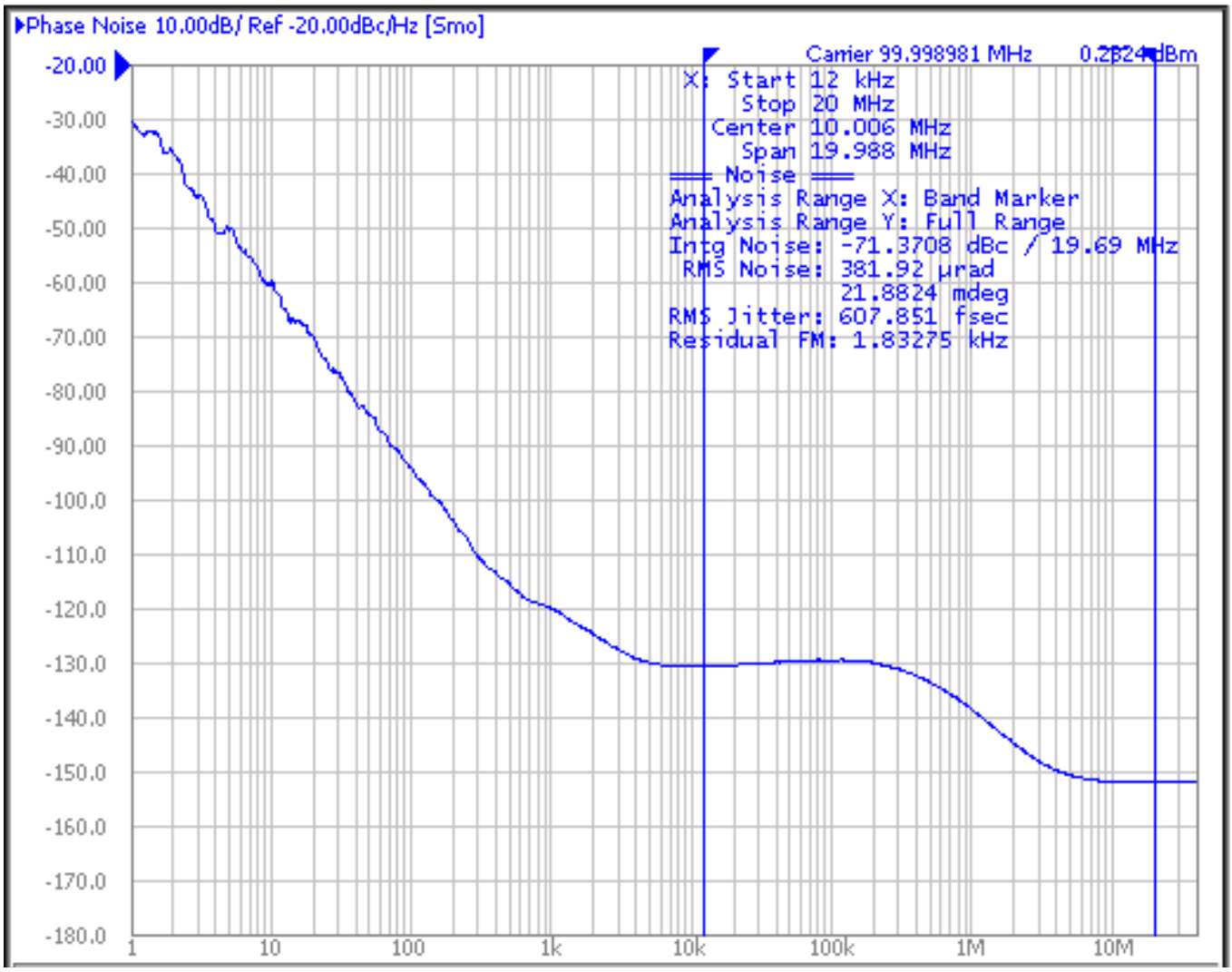
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 6B. AC Characteristics, $V_{DD} = V_{DD\_XTAL} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

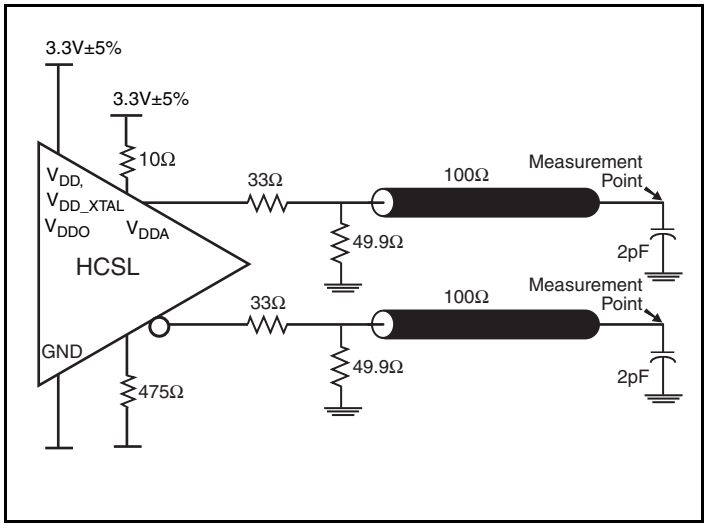
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		100		500	MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	CLK_SEL = 1 100MHz, Integration Range (12kHz to 20MHz)		0.608		ps
tsk(o)	Output Skew; NOTE 2, 3				85	ps
tsk(b)	Bank Skew; NOTE 2, 4				30	ps
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 2, 5	CLK_SEL = 1, SSC_EN = 0			20	ps
t_L	PLL Lock Time				100	ms
V_{MAX}	Absolute Max. Output Voltage; NOTE 6, 7				1150	mV
V_{MIN}	Absolute Min. Output Voltage; NOTE 6, 8		-300			mV
V_{RB}	Ringback Voltage; NOTE 9, 10		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; Note 9, 10		500			ps
V_{CROSS}	Absolute Crossing Voltage; NOTE 6, 11, 12		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 6, 11, 13				140	mV
	Rising Edge Rate; Note 9, 14		0.6		4	V/ns
	Falling Edge Rate; Note 9, 14		0.6		4	V/ns
odc	Output Duty Cycle; NOTE 9	$f_{OUT} \leq 250MHz$	48		52	%
		$f_{OUT} = 500MHz$	46		54	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1. Refer to Phase Noise Plot section.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4. Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 5. Jitter performance using XTAL inputs.
NOTE 6: Measurement taken from a single ended waveform.
NOTE 7: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 8: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section
NOTE 9: Measurement taken from a differential waveform.
NOTE 10:T_{STABLE} is the time the differential clock must maintain a minimum +- 150 mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 mV differential range.
NOTE 11: Measured at crossing point where the instantaneous voltage value of the rising edge of CLK+ equals the falling edge of CLK-.
NOTE 12: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 13: Defined as the total variation of all crossing voltages of rising CLK+ and falling CLK-, This is the maximum allowed variance in Vcross for any particular system. See Parameter Measurement Information Section
NOTE 14: Measured from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

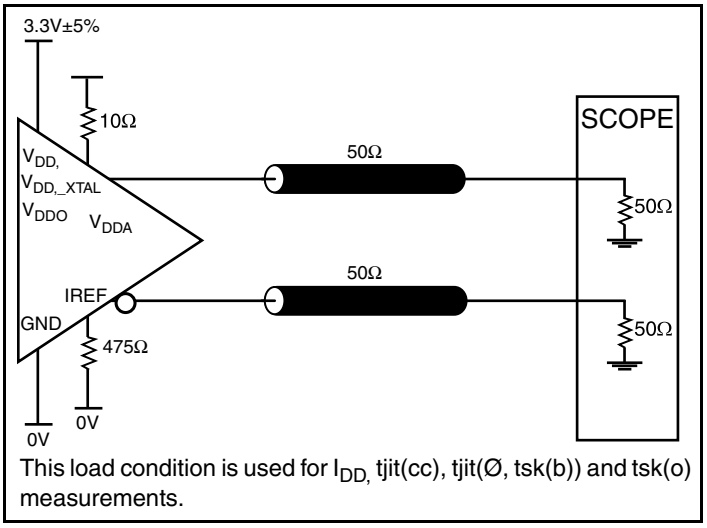
Typical Phase Noise at 100MHz



Parameter Measurement Information

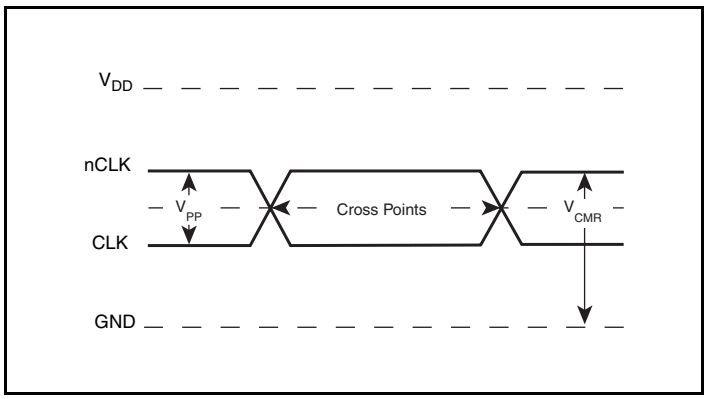


3.3V HCSL Output Load AC Test Circuit

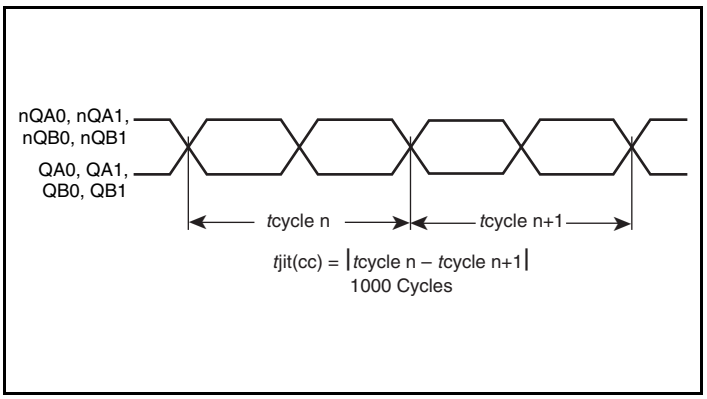


This load condition is used for I_{DD}, tjit(cc), tjit(Ø, tsk(b)) and tsk(o) measurements.

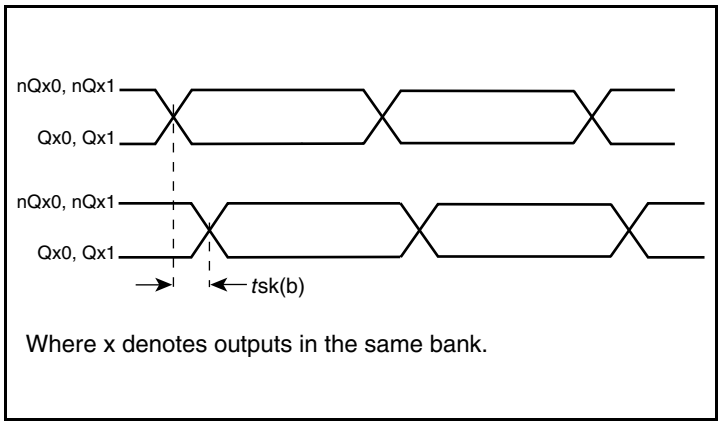
3.3V HCSL Output Load AC Test Circuit



Differential Input Level

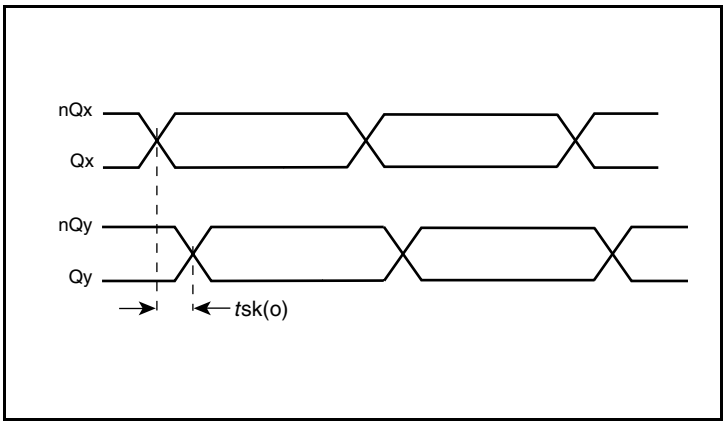


Cycle-to-Cycle Jitter



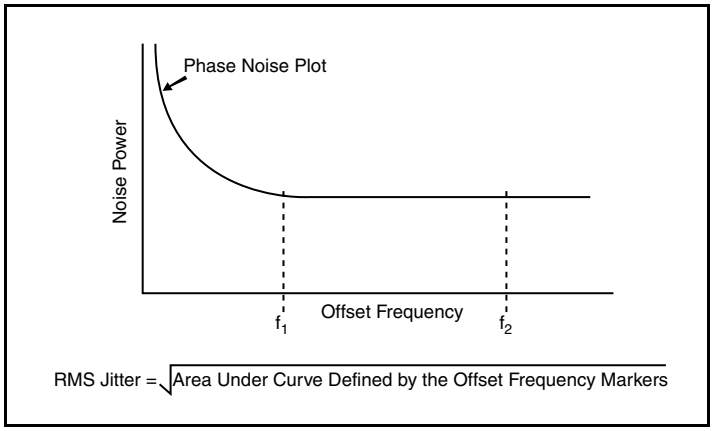
Where x denotes outputs in the same bank.

Bank Skew

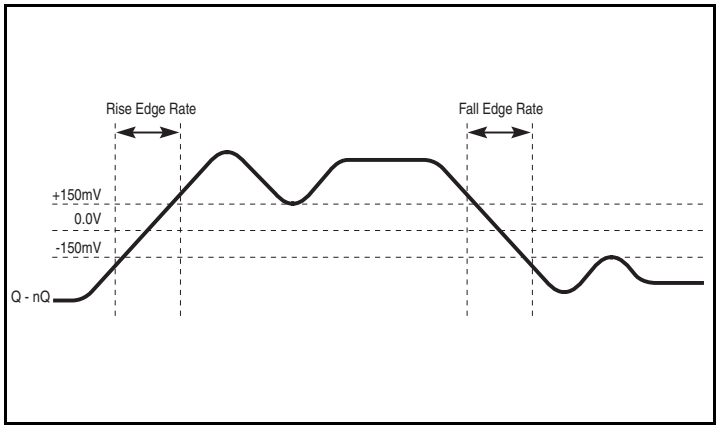


Output Skew

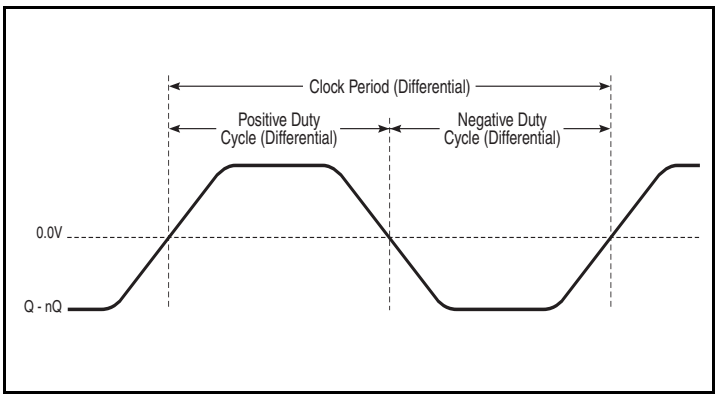
Parameter Measurement Information, continued



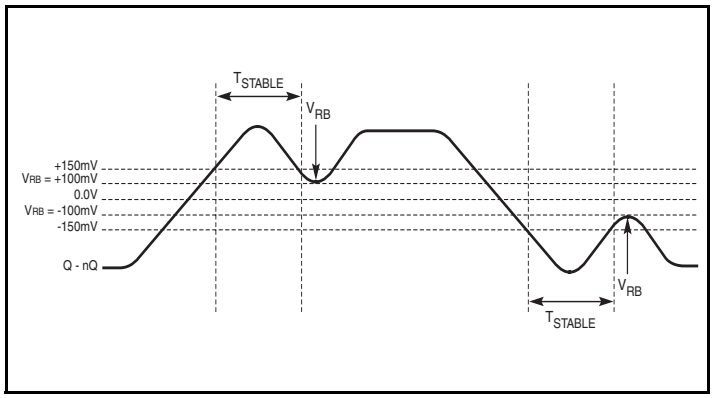
RMS Phase Jitter



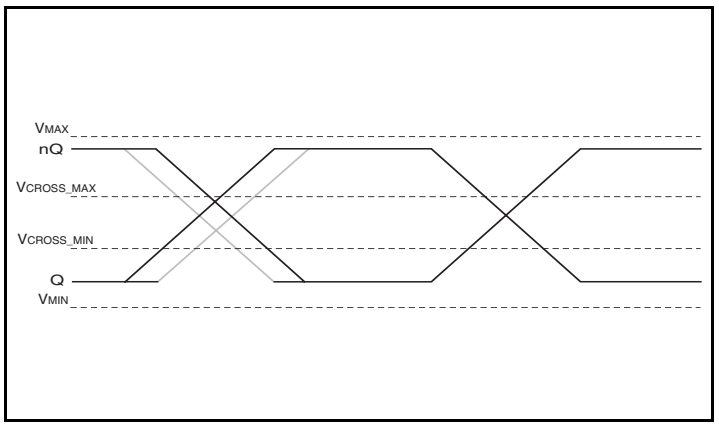
Differential Measurement Points for Rise/Fall Edge Rate



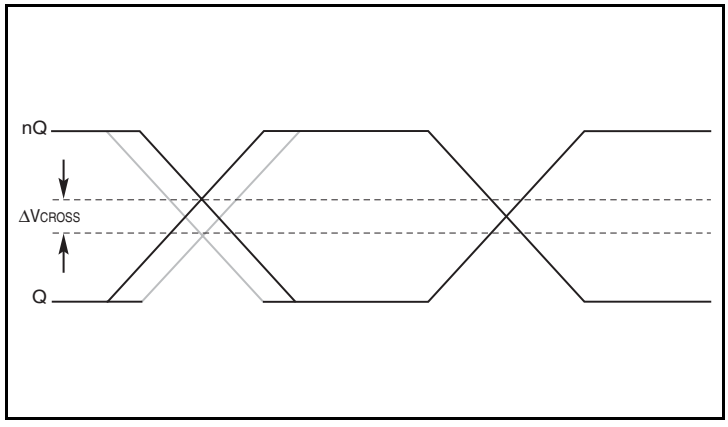
Differential Measurement Points for Duty Cycle/Period



Differential Measurement Points for Ringback

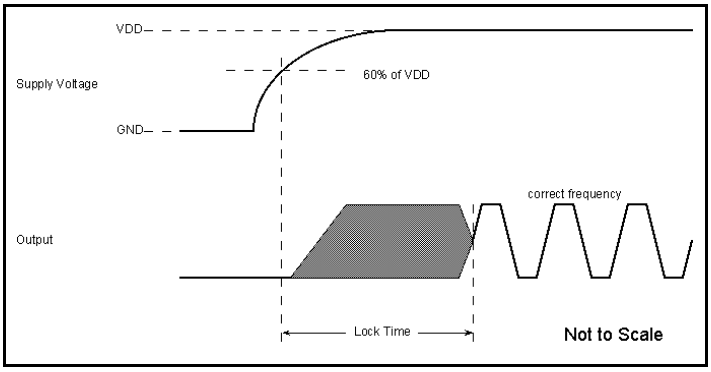


Single-ended Measurement Points for Absolute Cross Point and Swing



Single-ended Measurement Points for Delta Cross Point

Parameter Measurement Information, continued



PLL Lock Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

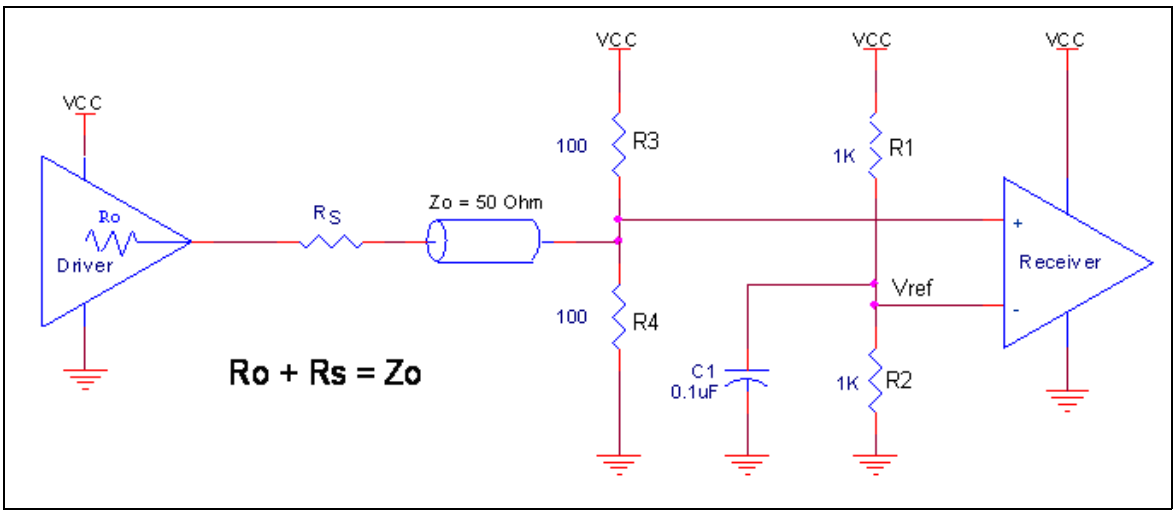


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

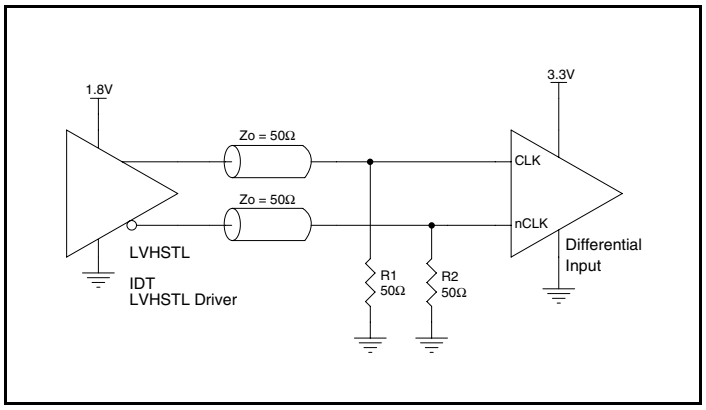


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

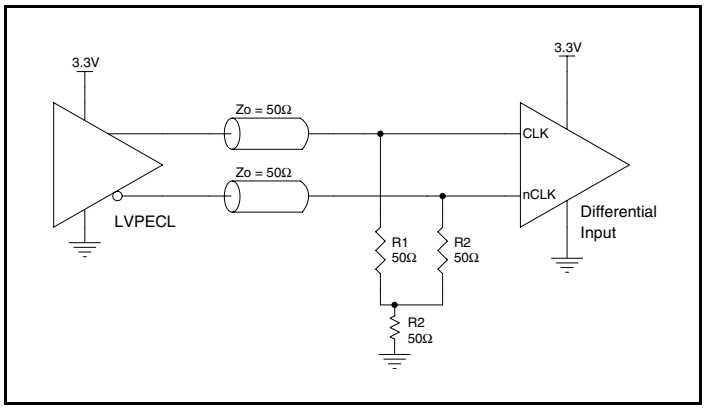


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

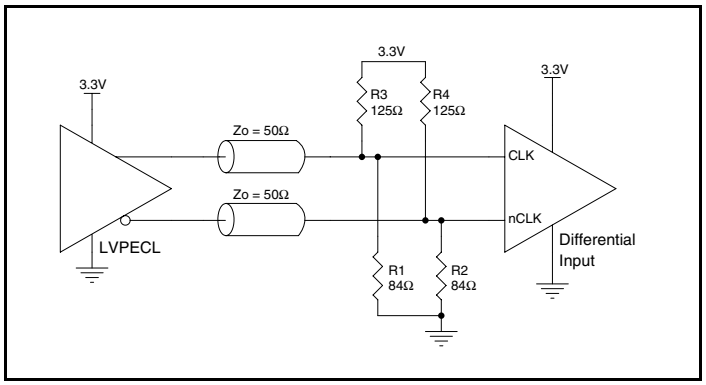


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

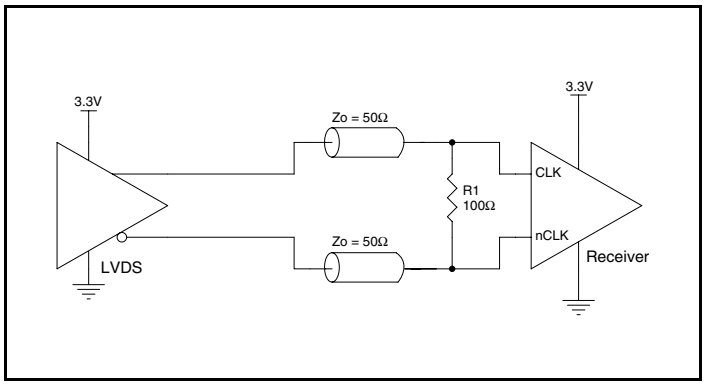


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

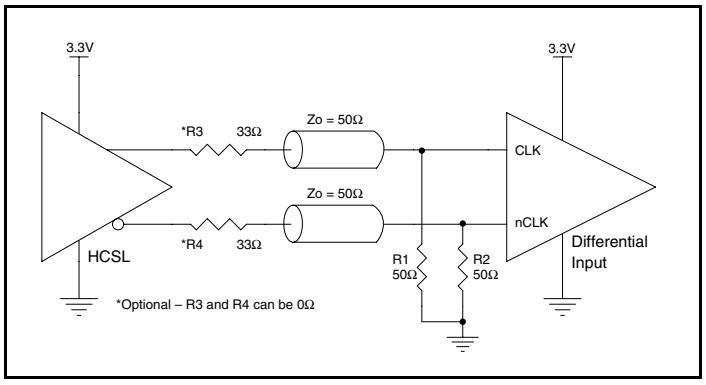


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

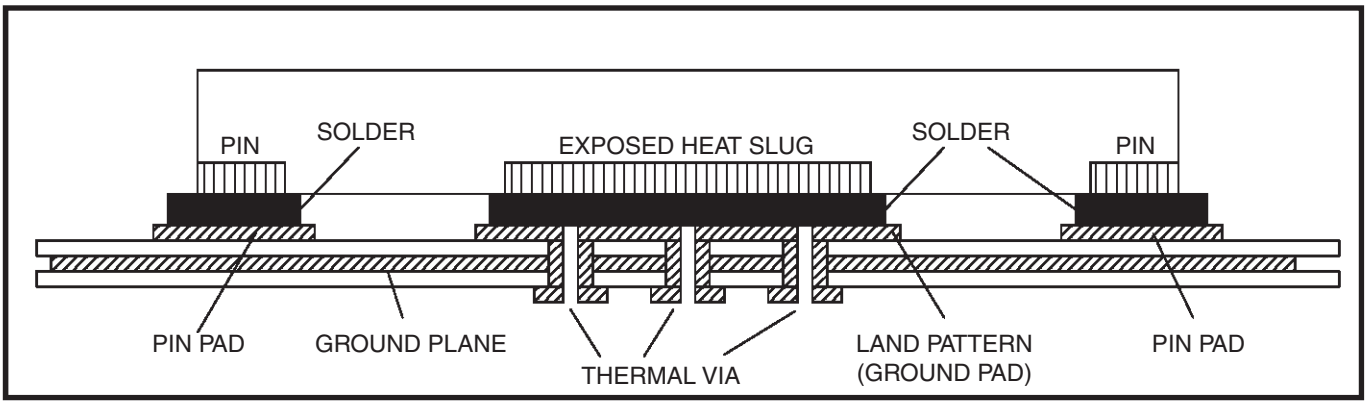


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

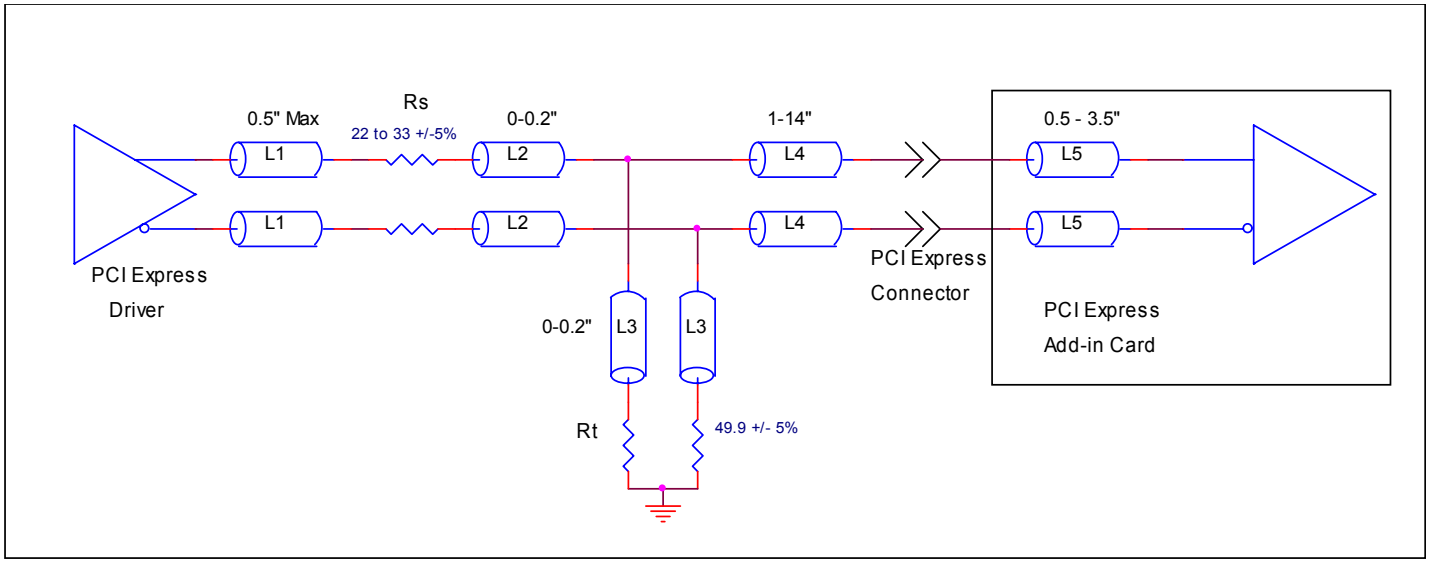


Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

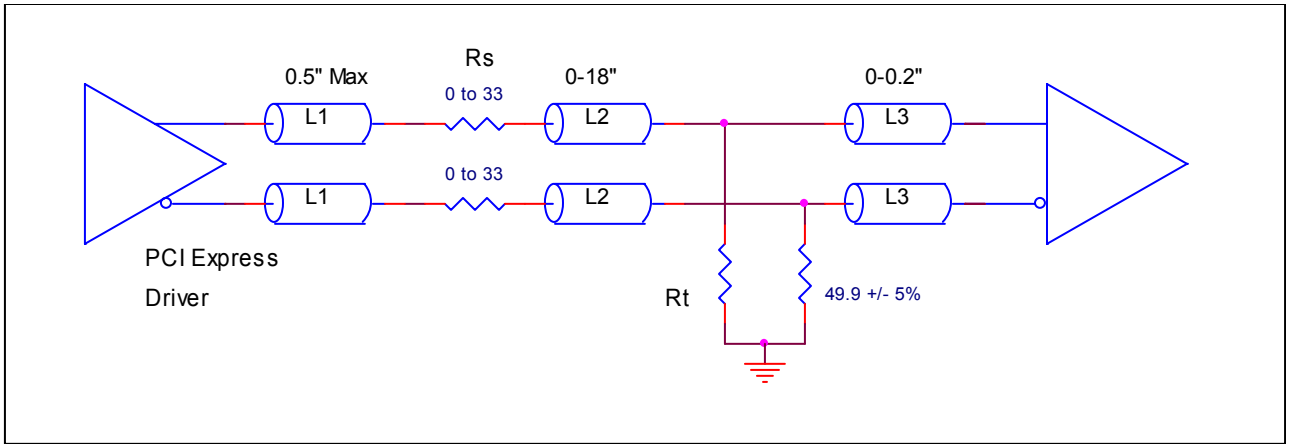


Figure 4B. Recommended Termination (where a point-to-point connection can be used)

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

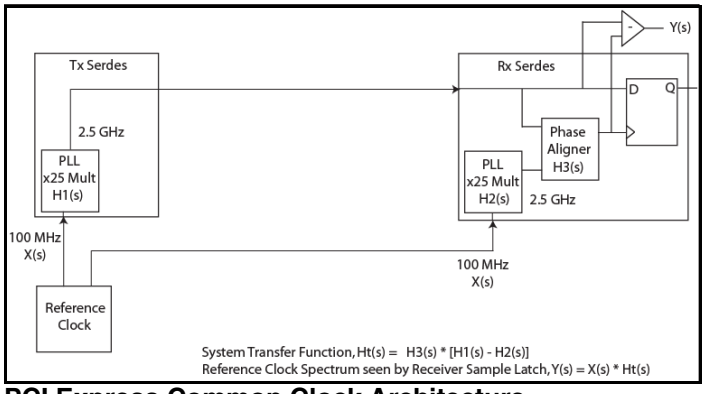
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

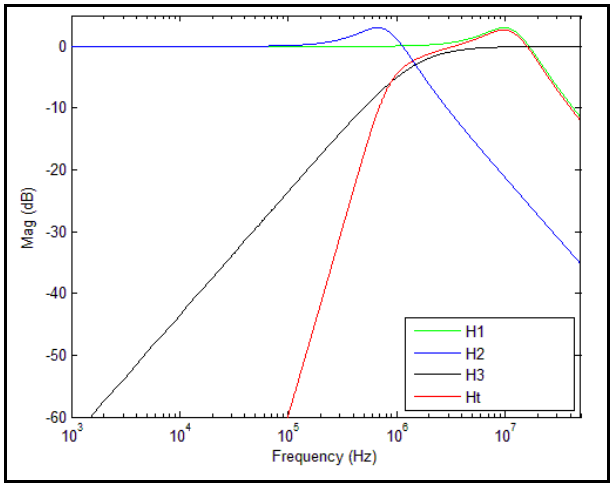
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



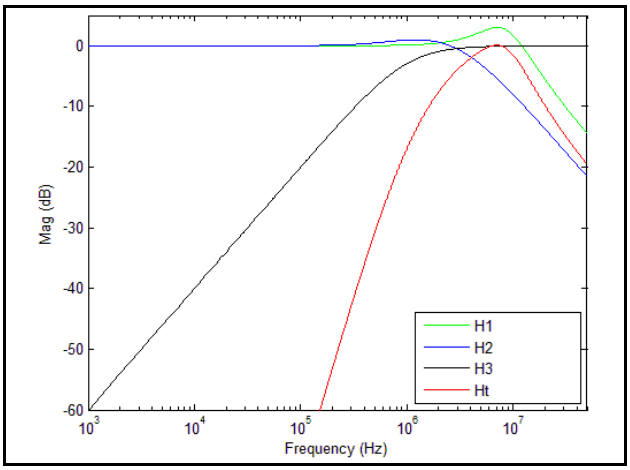
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

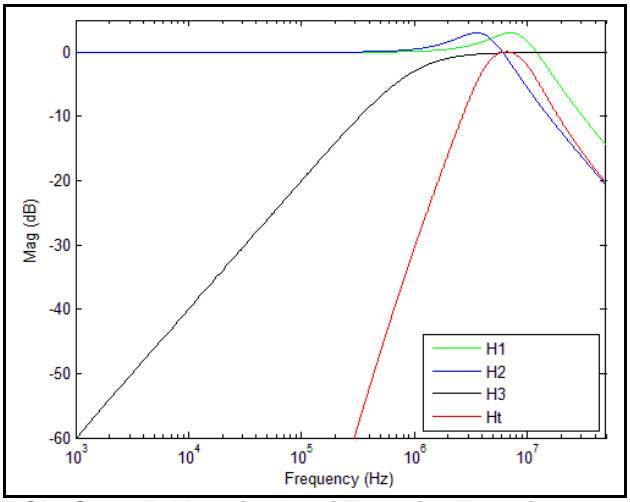


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

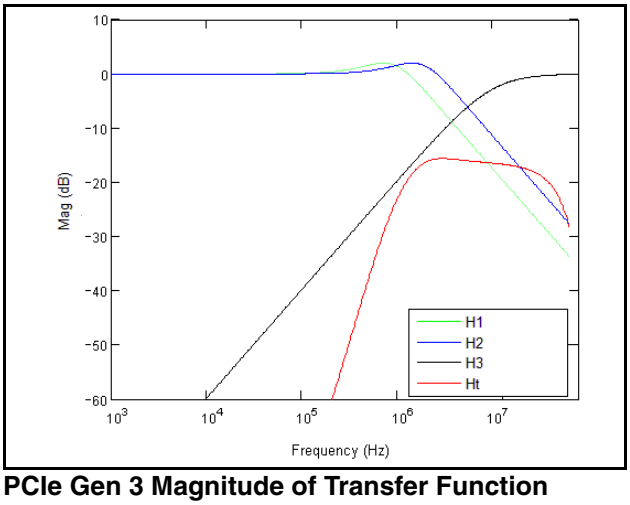


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Schematic Example

Figure 5 shows an example of ICS871S1022 application schematic. In this example, the device is operated V_{DD}= V_{DDO} = V_{DD_XTAL} = V_{DDA} = 3.3V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS871S1022 provides separate power supplies to isolate noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datashet to ensure the logic control inputs are properly set.

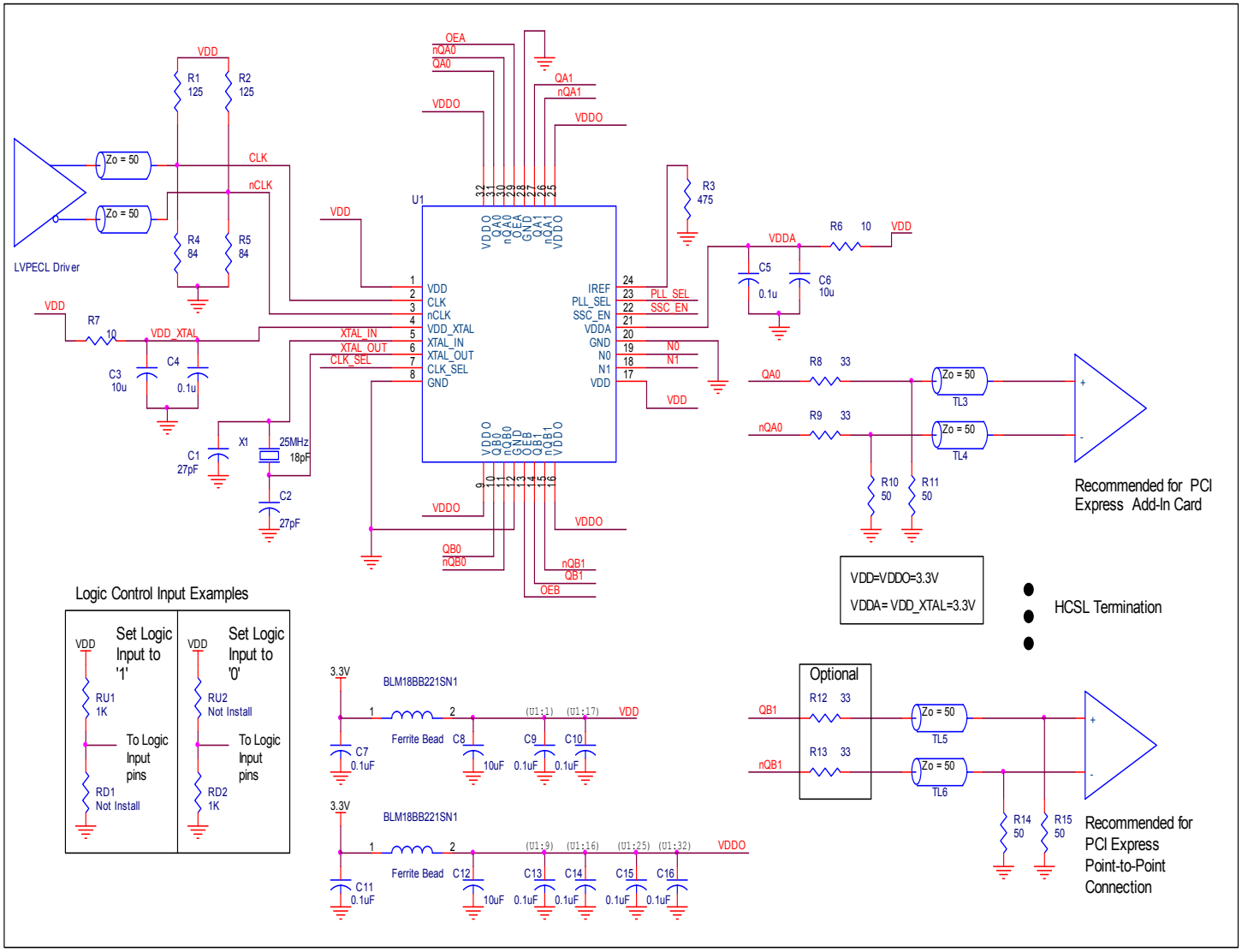


Figure 5. ICS871S1022 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS871S1022.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS871S1022 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 70°C is as follows:

I_{DD_MAX} = 87mA
$I_{DD\_XTAL\_MAX}$ = 7mA
I_{DDA_MAX} = 18mA
I_{DDO_MAX} = 27mA

Power (no-load)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DD_XTAL} + I_{DDA_MAX} + I_{DDO_MAX}) = 3.465V *(87mA + 7mA + 18mA + 27mA) = **481.635mW**

- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 44.5mW = **178mW**

Total Power$_{\_MAX}$ = 481.635mW + 178mW = **659.635mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.660W *39.5°C/W = 96.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

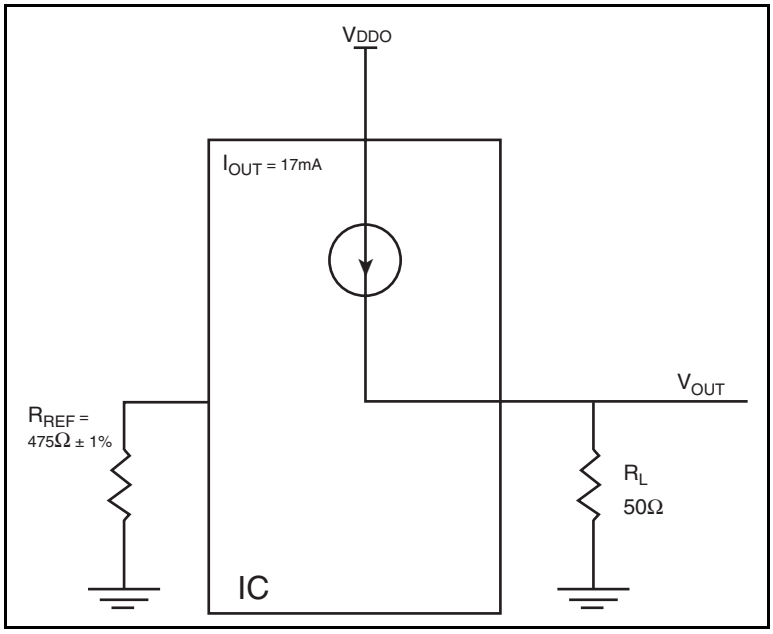


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DDO_MAX}.

Power = $(V_{DDO\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DDO\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

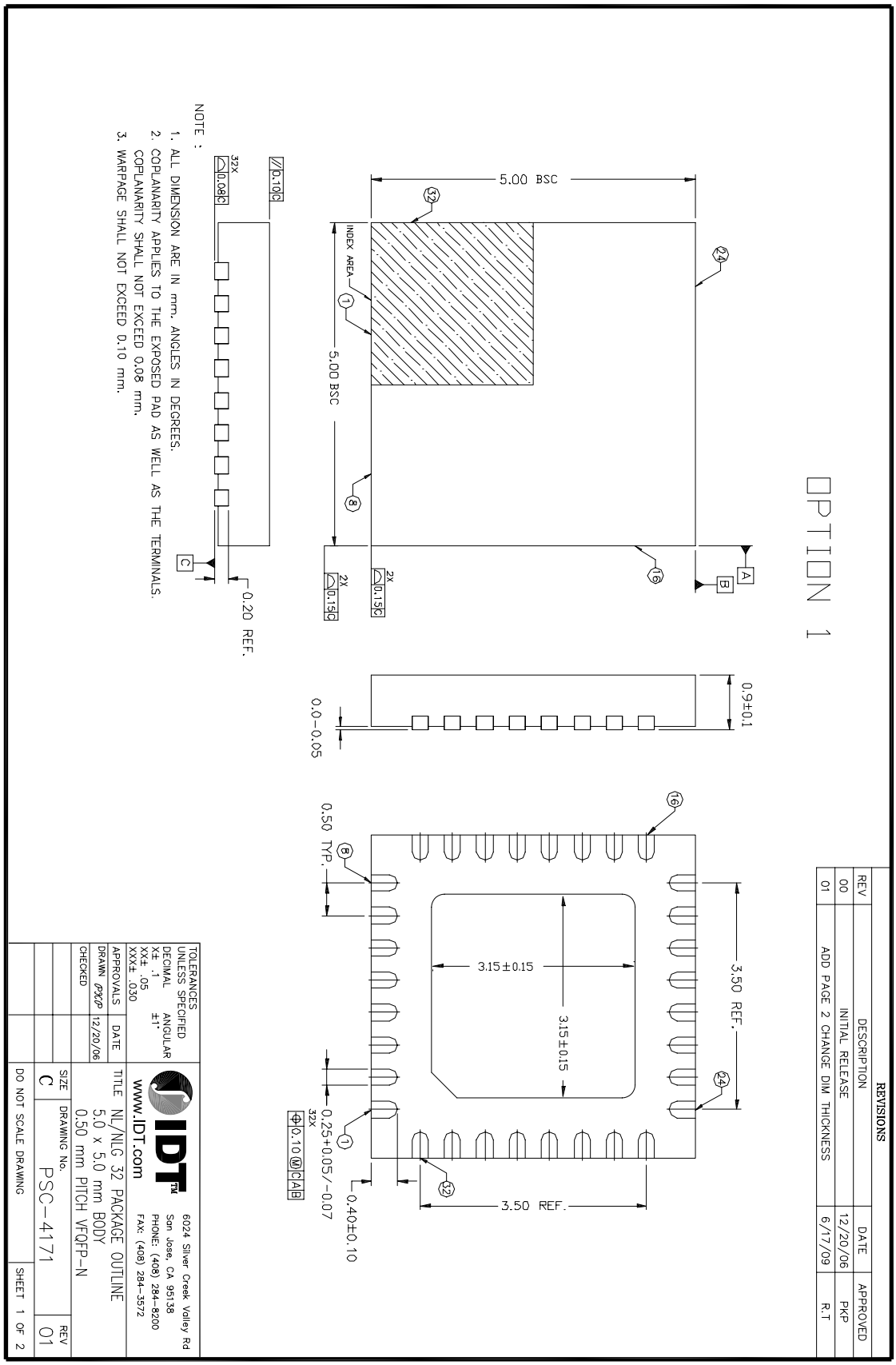
Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

Transistor Count

The transistor count for ICS871S1022 is: 11,517

32 Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
871S1022EKLF	ICS1S1022EL	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
871S1022EKLFT	ICS1S1022EL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4A	5 17	AC Characteristics Table - changed I_{DD} max from 87mA to 100mA (per Errata NEN-11-08. Power Considerations - added maximum current note.	8/24/11

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6024 Silver Creek Valley Road
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