阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

1.5V LOW-POWER WIDE-RANGE FREQUENCY CLOCK DRIVER

ICS98UAE877A

Description

The PLL clock buffer, ICS98UAE877A, is designed for a V_{DDQ} of 1.5V, an AV_{DD} of 1.5V and differential data input and output levels.

ICS98UAE877A is a zero delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock outputs (FB_OUTT, FBOUTC). The clock outputs are controlled by the input clocks (CLK_INT, CLK_INC), the feedback clocks (FB_INT, FB_INC), the LVCMOS program pins (OE, OS) and the Analog Power input (AVDD). When OE is low, the outputs (except FB_OUTT/FB_OUTC) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to GND or V_{DDQ}. When OS is high, OE will function as described above. When OS is low, OE has no effect on CLKT7/CLKC7 (they are free running in addition to FB_OUTT/FB_OUTC). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock signals (CLK_INT, CLK_INC) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL

will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INT, CLK_INC) within the specified stabilization time tSTAB.

The PLL in ICS98UAE877A clock driver uses the input clocks (CLK_INT, CLK_INC) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT[0:9], CLKC[0:9]). ICS98UAE877A is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

ICS98UAE877A is available in Commercial Temperature Range (0°C to 70°C) and Industrial Temperature Range (-40°C to +85°C). See Ordering Information for details

Features

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- Auto PD when input signal is at a certain logic state
- Available in 52-ball VFBGA and a 40-pin MLF

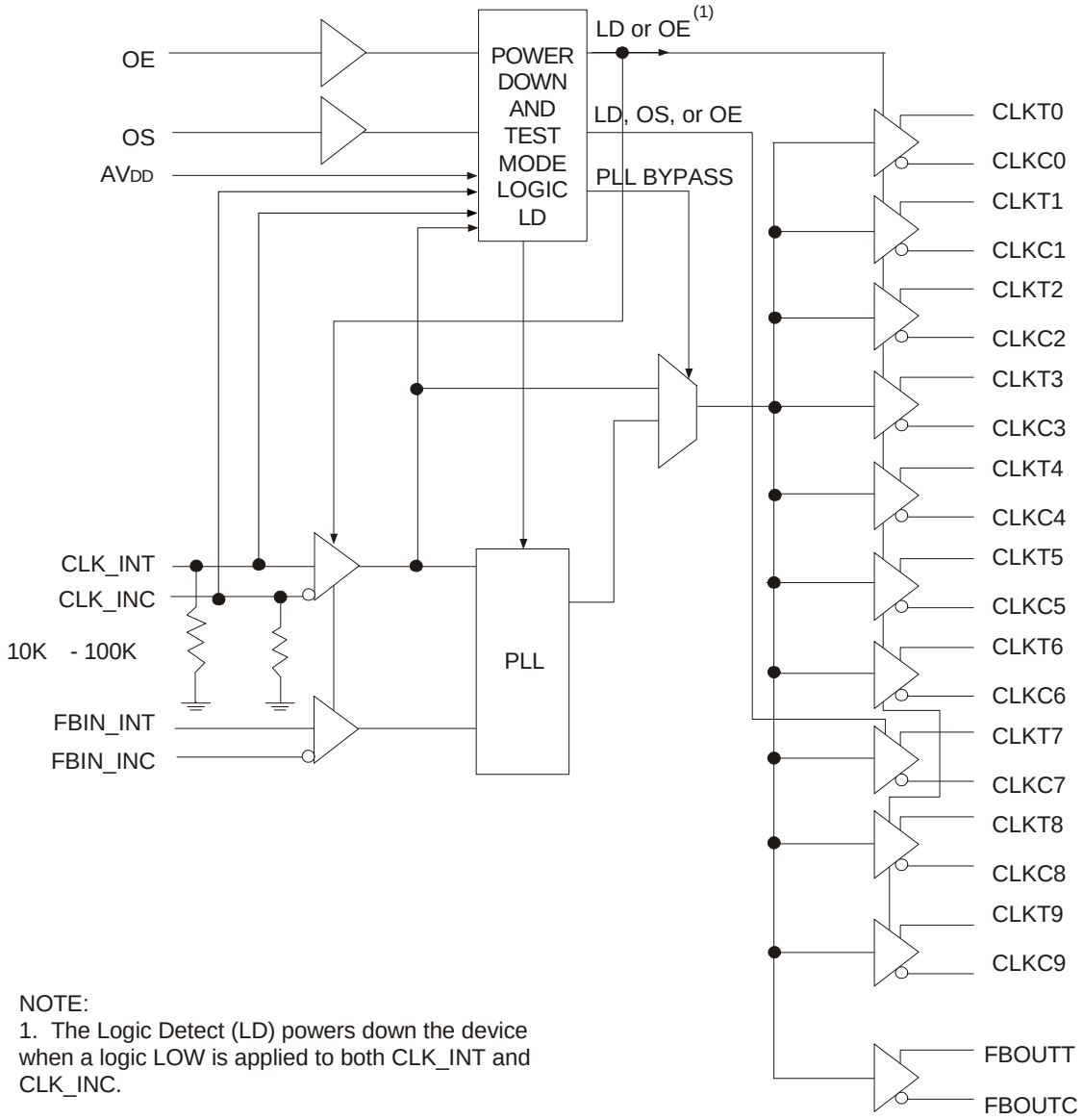
Applications

- DDR2 Memory Modules / Zero Delay Board Fan Out
- Provides complete DDR DIMM solution with IDT74SSTUAE32xxx family

Switching Characteristics

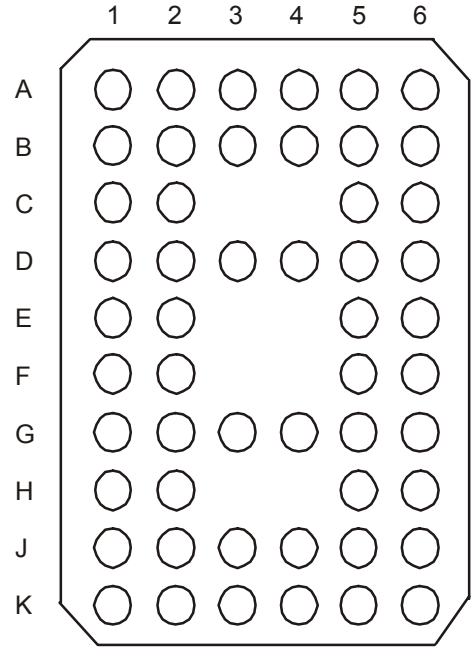
- Period jitter: 40ps (DDR2-400/533)
  30ps (DDR2-667)
- Half-period jitter: 60ps (DDR2-400/533)
  50ps (DDR2-667)
- Output-Output Skew 40ps (DDR2-400/533)
  30ps (DDR2-667)
- Cycle-Cycle Jitter 40ps

Block Diagram



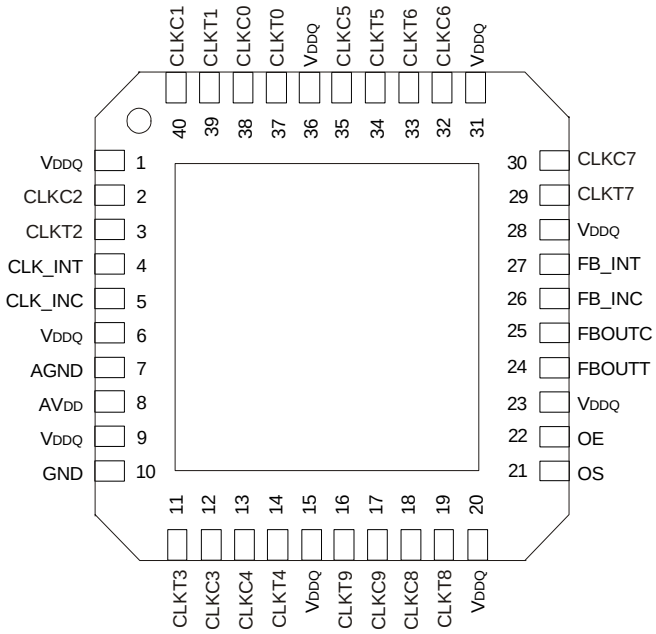
NOTE:
1. The Logic Detect (LD) powers down the device when a logic LOW is applied to both CLK_INT and CLK_INC.

Pin Configurations



	1	2	3	4	5	6
A	CLKT1	CLKT0	CLKC0	CLKC5	CLKT5	CLKT6
B	CLKC1	GND	GND	GND	GND	CLKC6
C	CLKC2	GND	NB	NB	GND	CLKC7
D	CLKT2	VDDQ	VDDQ	VDDQ	OS	CLKT7
E	CLK_INT	VDDQ	NB	NB	VDDQ	FB_INT
F	CLK_INC	VDDQ	NB	NB	OE	FB_INC
G	AGND	VDDQ	VDDQ	VDDQ	VDDQ	FB_OUTC
H	AVDD	GND	NB	NB	GND	FB_OUTT
J	CLKT3	GND	GND	GND	GND	CLKT8
K	CLKC3	CLKC4	CLKT4	CLKT9	CLKC9	CLKC8

176 BALL BGA
TOP VIEW



40-PIN MLF
TOP VIEW

Pin Descriptions

Terminal Name	Description	Electrical Characteristics
AGND	Analog Ground	Ground
AV_{DD}	Analog Power	1.5V Nominal
CLK_INT	Clock Input with a 10K-100K Ω pulldown resistor	Differential Input
CLK_INC	Complementary Clock Input with a 10K-100K Ω pulldown resistor	Differential Input
FB_INT	Feedback Clock Input	Differential Input
FB_INC	Complementary Feedback clock input	Differential Input
FB_OUTT	Feedback Clock Output	Differential Output
FB_OUTC	Complementary Feedback clock Output	Differential Output
OE	Output Enable (Asynchronous)	LVCMOS Input
OS	Output Select (tied to GND or V_{DDQ})	LVCMOS Input
GND	Ground	Ground
V_{DDQ}	Logic and Output Power	1.5V Nominal
CLKT[0:9]	Clock Outputs	Differential Outputs
CLKC[0:9]	Complementary Clock Outputs	Differential Outputs
NB	No Ball	

Function Table

Inputs					Outputs				PLL
AVDD	**OE**	**OS**	**CLK_ INT**	**CLK_ INC**	**CLKT**	**CLKC**	**FB_ OUTT**	**FB_ OUTC**	
GND	H	X	L	H	L	H	L	H	Bypassed/Off
GND	H	X	H	L	H	L	H	L	Bypassed/Off
GND	L	H	L	H	L(Z)[1]	L(Z)[1]			Bypassed/Off
GND	L	L	H	L	L(Z), CLKT7 active[1]	L(Z), CLKC7 active[1]	H	L	Bypassed/Off
1.5V (nom)	L	H	L	H	L(Z)[1]	L(Z)[1]	L	H	On
1.5V (nom)	L	L	H	L	L(Z), CLKT7 active[1]	L(Z), CLKC7 active[1]	H	L	On
1.5V (nom)	H	X	L	H	L	H	L	H	On
1.5V (nom)	H	X	H	L	H	L	H	L	On
1.5V (nom)	X	X	L	L	L(Z)[1]	L(Z)[1]	L(Z)[1]	L(Z)[1]	Off
1.5V (nom)	X	X	H	H	Reserved				

1 Outputs are disabled to a LOW state meeting the I_{ODL} limit.

Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Item	Rating
Supply Voltage, (AV_{DD} and V_{DDQ})	-0.5V to 2.5V
Logic Inputs	GND - 0.5V to V_{DDQ} + 0.5V
Ambient Operating Temperature	-40° C to +85° C
Storage Temperature	-65 to +150° C

DC Electrical Characteristics Over Operating Range

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C; Supply Voltage AV_{DD}/V_{DDQ} = 1.5V ± 0.075V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = -100µA	V_{DDQ} - 2			V
		I_{OH} = -6mA	1.1	1.45		
V_{OL}	Output LOW Voltage	I_{OL} = 100µA		0.25	0.1	V
		I_{OL} = 6mA			0.6	
V_{IK}	Input Clamp Voltage	I_{IN} = -18mA			-1.2	V
I_{IH}	Input HIGH Current	CLK_INT, CLK_INC; V_I = V_{DD} or GND			±250	µA
I_{IL}	Input LOW Current	OS, FB_INT, FB_INC; V_I = V_{DD} or GND			±10	µA
I_{ODL}	Output Disabled LOW Current	OE = L, V_{ODL} = 100mV	100			µA
$I_{DD}1.5$	Operating Supply Current	C_L = 0pF @ 410MHz			300	mA
I_{DDLD}		C_L = 0pF			500	µA
C_{IN}[1]	Input Capacitance	V_I = V_{DDQ} or GND	2		3	pF
C_{OUT}[1]	Output Capacitance	V_{OUT} = V_{DDQ} or GND	2		3	

1 Guaranteed by design, not 100% tested in production.

Recommended Operating Conditions

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C; Supply Voltage AV_{DD}/V_{DDQ} = 1.5V ± 0.075V.

Symbol	Parameter[1]	Conditions	Min.	Typ.	Max.	Units
AV_{DD}, V_{DDQ}	Supply Voltage		1.425	1.5	1.575	V
V_{IL}	LOW - Level Input Voltage	CLK_INT, CLK_INC, FB_INT, FB_INC			0.35 x V_{DDQ}	V
		OE, OS				
V_{IH}	HIGH -Level Input Voltage	CLK_INT, CLK_INC, FB_INT, FB_INC	0.65 x V_{DDQ}			V
		OE, OS				
V_{IN}	DC Input Signal Voltage[2]		-0.3		V_{DDQ} + 0.3	V
V_{ID}	Differential Input Signal Voltage[3]	DC - CLK_INT, CLK_INC, FB_INT, FB_INC	0.35		V_{DDQ} + 0.4	V
		AC - CLK_INT, CLK_INC, FB_INT, FB_INC	0.6			
V_{OX}	Output Differential Cross-Voltage[4]		V_{DDQ}/2 - 0.1		V_{DDQ}/2 +0.1	V
V_{IX}	Input Differential Cross-Voltage[4]		V_{DDQ}/2 - 0.15	V_{DDQ}/2	V_{DDQ}/2 + 0.15	
I_{OH}	HIGH-Level Output Current				-6	mA
I_{OL}	LOW-Level Output Current				6	
T_A	Operating Free-Air Temperature		-40		+85	°C

1 Unused inputs must be held HIGH or LOW to prevent them from floating.

2 DC input signal voltage specifies the allowable DC execution of differential input.

3 Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.

4 Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signal must be crossing.

Timing Requirements Over Recommended Operating Free-Air Temperature Range

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C; Supply Voltage AV_{DD}/V_{DDQ} = 1.5V ± 0.075V.

Symbol	Parameter[1]	Conditions	Min.	Max.	Units
$freq_{OP}$	Max Clock Frequency[2]	1.5V ± 0.075V @ 25° C	95	410	MHz
$freq_{APP}$	Application Frequency Range[3]	1.5V ± 0.075V @ 25° C	160	410	MHz
d_{TIN}	Input Clock Duty Cycle		40	60	%
T_{STAB}	CLK Stabilization[4]			9	µs

1 The PLL must be able to handle spread spectrum induced skew.

2 Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)

3 Application clock frequency indicates a range over which the PLL must meet all timing parameters.

4 Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal, within the value specificied by the Static Phase Offset ($t\varnothing$), after power-up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CLK and $\overline{CLK}$ go to a logic low state, enter the power-down mode and later return to active operation. CLK and $\overline{CLK}$ may be left floating after they have been driven low for one complete clock cycle.

Switching Characteristics Over Recommended Free Air Operating Range

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C; Supply Voltage AV_{DD}/V_{DDQ} = 1.5V ± 0.075V

Symbol	Parameter[1]	Conditions	(MHz)	Min.	Typ.	Max.	Units
t_{EN}	Output Enable Time	OE to any output	160 - 410		4.73	8	ns
t_{DIS}	Output Disable Time	OE to any output			5.82	8	ns
$t_{JIT(PER)}$	Period Jitter		160 - 270	-40		40	ps
			271 - 410	-30		30	
$t_{JIT(HPER)}$	Half-Period Jitter		160 - 270	-60		60	ps
			271 - 410	-50		50	
$SL_{r1(i)}$	Input Slew Rate	Input Clock	160 - 410	1	2.5	4	v/ns
		Output Enable (OE, OS)		0.5			
$SL_{r1(o)}$	Output Clock Slew Rate			0.8		2	v/ns
$t_{JIT(CC+)}$	Cycle-to-Cycle Period Jitter			0		40	ps
$t_{JIT(CC-)}$				0		-40	
$t_{(\varnothing)\,DYN}$	Dynamic Phase Offset		160 - 270	-50		50	ps
			271 - 410	-20		20	
t_{SPO}[2]	Static Phase Offset		271 - 410	-60	0	60	ps
$\sum(su)$	$t_{JIT(PER)} + t_{(\varnothing)\,DYN} + t_{SKEW(O)}$					80	ps
$\sum(h)$	$t_{(\varnothing)\,DYN} + t_{SKEW(O)}$					60	ps
t_{SKEW}	Output-to-Output Skew		160 - 270			60	ps
			271 - 410			30	
	SSC Modulation Frequency			30		33	KHz
	SSC Clock Input Frequency Deviation			0		-0.5	%
	PLL Loop Bandwidth (-3dB from unity gain)			2			MHz

1 Guaranteed for application frequency range.
2 Static phase offset shifted by design.

Parameter Measurement Information

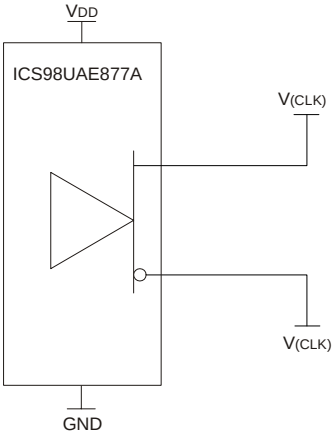


Figure 1: IBIS Model Output Load

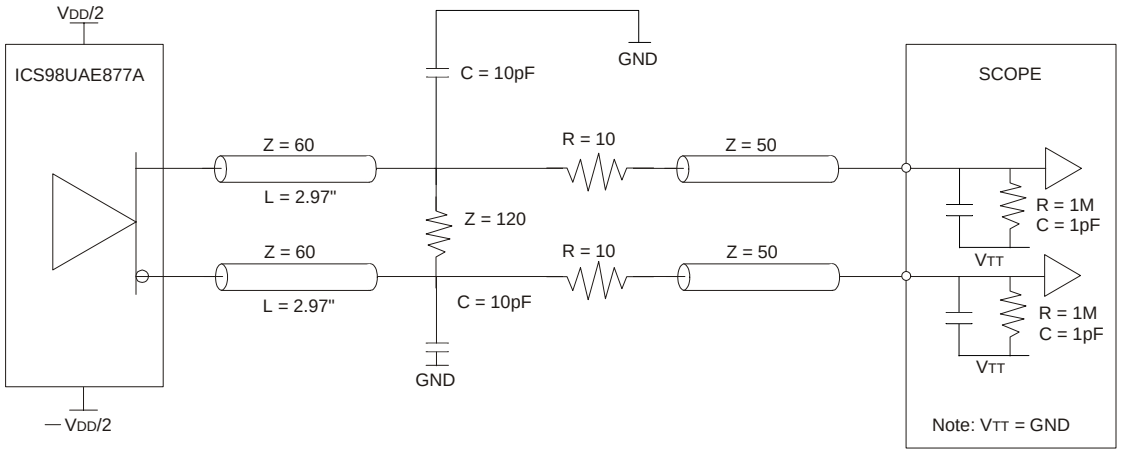


Figure 2: Output Load Test Circuit

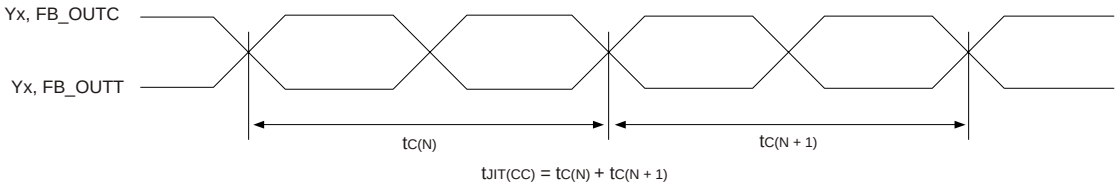
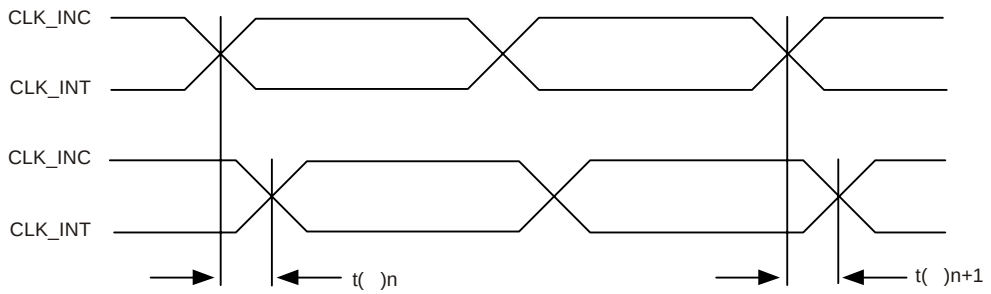


Figure 3: Cycle-to-Cycle Jitter



$$t(\ ) = \frac{\sum_{1}^{n=N} t(\ )n}{N}$$

Figure 4: Static Phase Offset

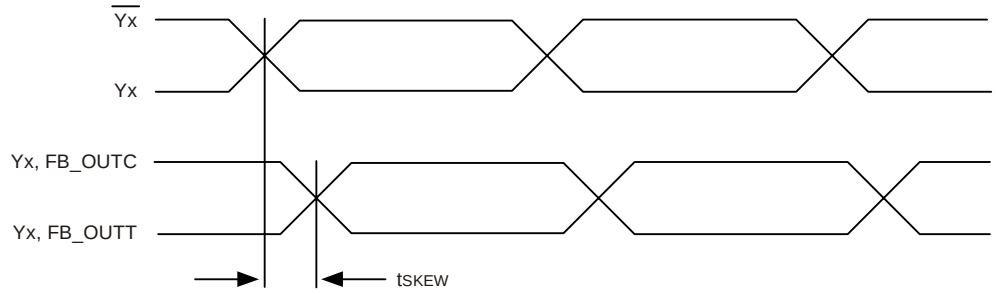
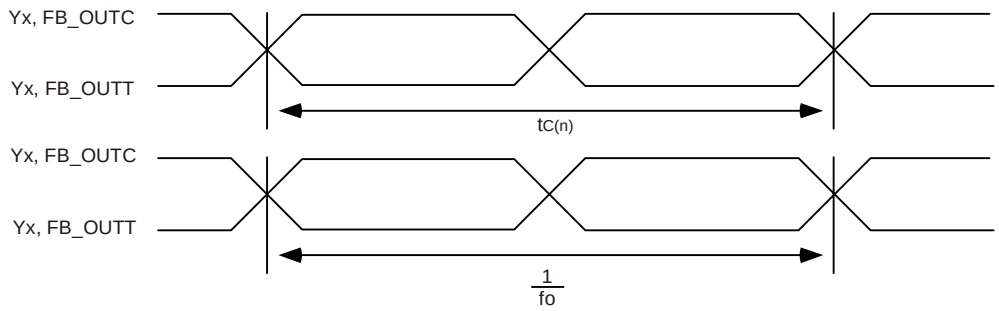
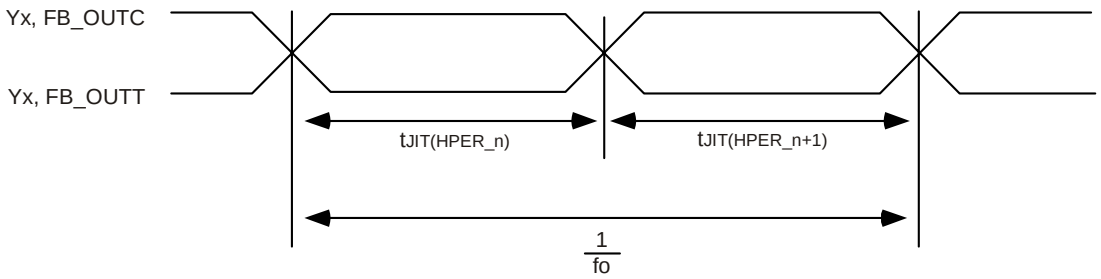


Figure 5: Output Skew



$$t_{(JIT\_PER)} = t_{C(n)} - \frac{1}{fo}$$

Figure 6: Period Jitter



$$t_{JIT(HPER)} = t_{JIT(HPER\_n)} - \frac{1}{2xfo}$$

Figure 7: Half-Period Jitter

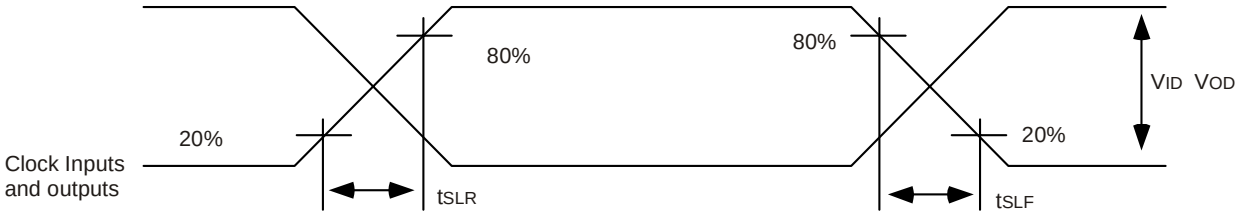


Figure 8: Input and Output Slew Rates

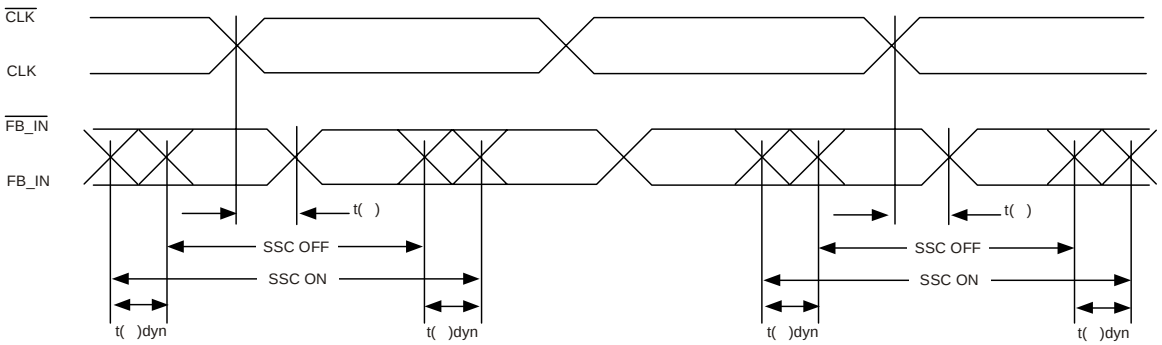


Figure 9: Dynamic Phase Offset

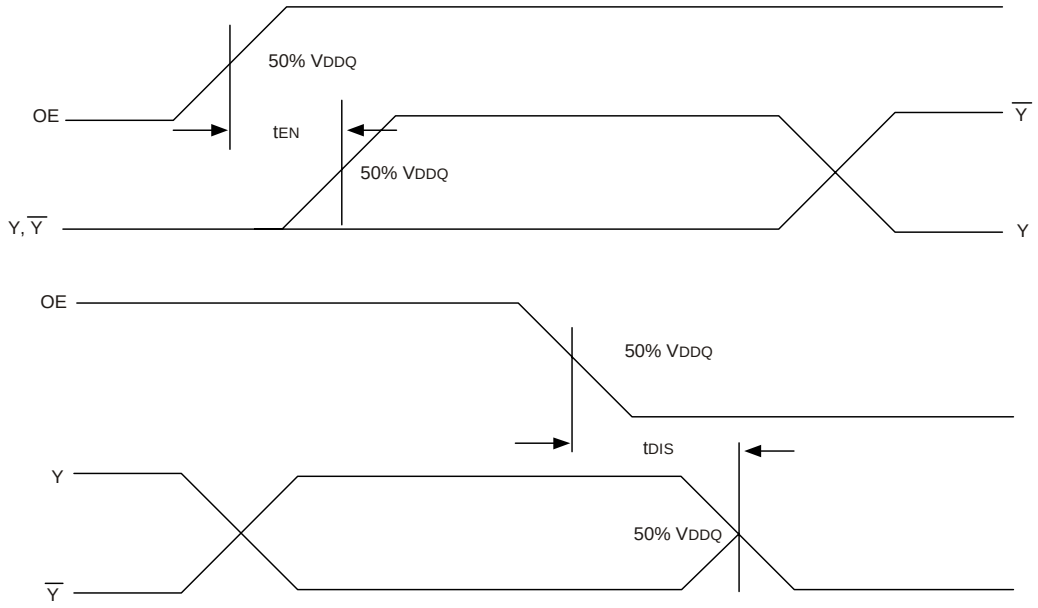


Figure 10: Time Delay Between OE and Clock Output (Y, $\overline{Y}$)

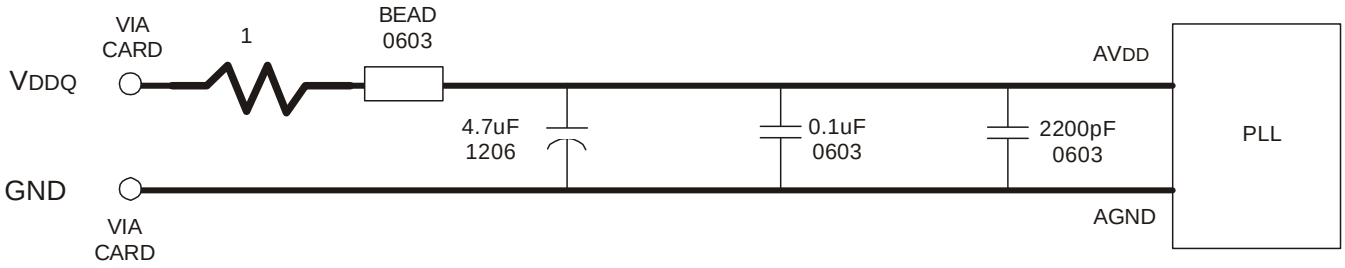
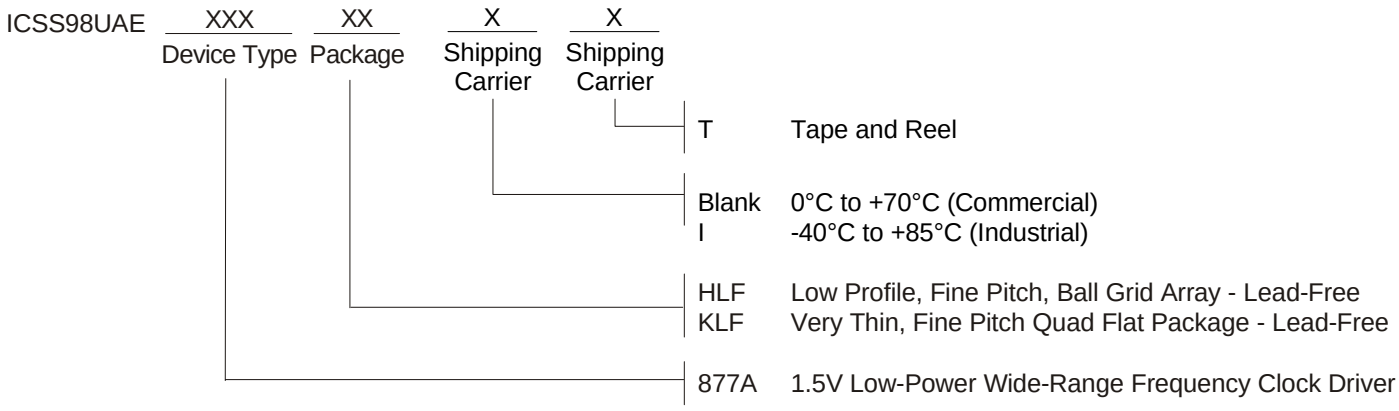


Figure 11. AVDD Filtering

*Place the 2200pF capacitors close to the PLL.
*Use wide traces for PLL Analog power and GND. Connect PLL and caps to AGND trace and connect trace to one GND via (farthest from PLL).
*Recommended bead: Fair-rite P/N 2506036017Y0 or equivalent (0.8 DC max., 600 at 100MHz).

Ordering Information



Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com