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1.8V Low-Power Wide-Range Frequency Clock Driver

Recommended Application:

- DDR2 Memory Modules / Zero Delay Board Fan Out
- Provides complete DDR2 DIMM logic solution

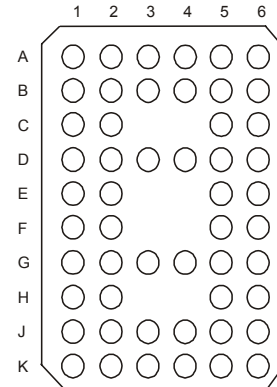
Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_18)
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- Auto PD when input signal is at a certain logic state

Switching Characteristics:

- Period jitter: 40ps (DDR2-400/533)
30ps (DDR2-667/800)
- Half-period jitter: 60ps (DDR2-400/533)
50ps (DDR2-667/800)
- OUTPUT - OUTPUT skew: 40ps (DDR2-400/533)
30ps (DDR2-667/800)
- CYCLE - CYCLE jitter 40ps

Pin Configuration

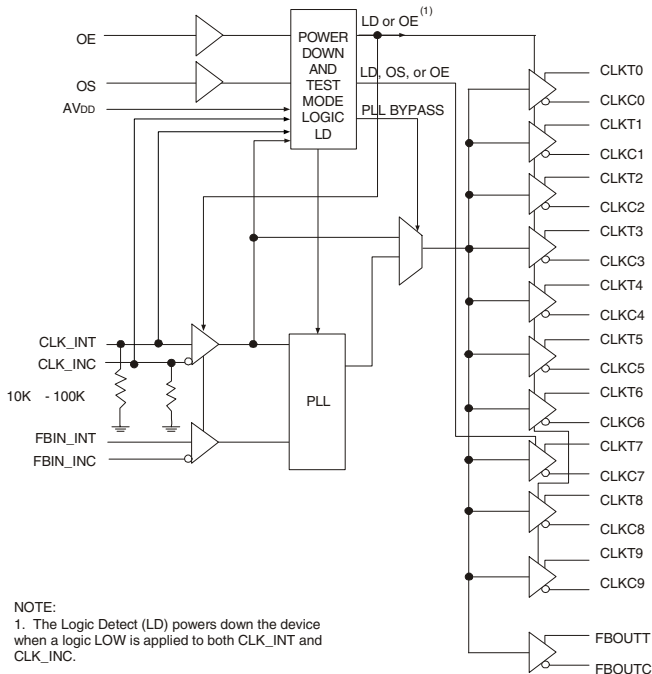


52-Ball BGA

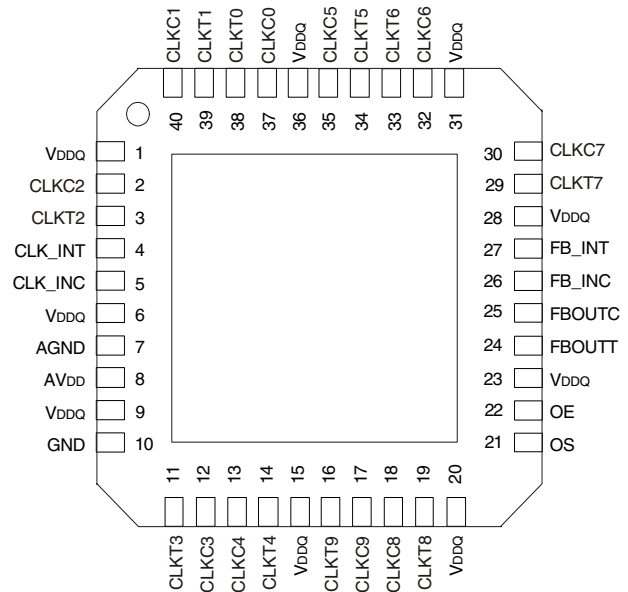
Top View

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---------|-------|-------|-------|-------|---------|
| A | CLKT1 | CLKT0 | CLKC0 | CLKC5 | CLKT5 | CLKT6 |
| B | CLKC1 | GND | GND | GND | GND | CLKC6 |
| C | CLKC2 | GND | NB | NB | GND | CLKC7 |
| D | CLKT2 | VDDQ | VDDQ | VDDQ | OS | CLKT7 |
| E | CLK_INT | VDDQ | NB | NB | VDDQ | FB_INT |
| F | CLK_INC | VDDQ | NB | NB | OE | FB_INC |
| G | AGND | VDDQ | VDDQ | VDDQ | VDDQ | FB_OUTC |
| H | AVDD | GND | NB | NB | GND | FB_OUTT |
| J | CLKT3 | GND | GND | GND | GND | CLKT8 |
| K | CLKC3 | CLKC4 | CLKT4 | CLKT9 | CLKC9 | CLKC8 |

Block Diagram



NOTE:
1. The Logic Detect (LD) powers down the device when a logic LOW is applied to both CLK_INT and CLK_INC.



40-Pin MLF



Pin Descriptions

| Terminal Name | Description | Electrical Characteristics |
|------------------|---|----------------------------|
| AGND | Analog Ground | Ground |
| AV _{DD} | Analog power | 1.8 V nominal |
| CLK_INT | Clock input with a (10K-100K Ohm) pulldown resistor | Differential input |
| CLK_INC | Complementary clock input with a (10K-100K Ohm) pulldown resistor | Differential input |
| FB_INT | Feedback clock input | Differential input |
| FB_INC | Complementary feedback clock input | Differential input |
| FB_OUTT | Feedback clock output | Differential output |
| FB_OUTC | Complementary feedback clock output | Differential output |
| OE | Output Enable (Asynchronous) | LVC MOS input |
| OS | Output Select (tied to GND or V _{DDQ}) | LVC MOS input |
| GND | Ground | Ground |
| V _{DDQ} | Logic and output power | 1.8V nominal |
| CLKT[0:9] | Clock outputs | Differential outputs |
| CLKC[0:9] | Complementary clock outputs | Differential outputs |
| NB | No ball | |

The PLL clock buffer, **ICS98ULPA877A**, is designed for a V_{DDQ} of 1.8 V, a AV_{DD} of 1.8 V and differential data input and output levels. Package options include a plastic 52-ball VFBGA and a 40-pin MLF.

ICS98ULPA877A is a zero delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock outputs (FB_OUTT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INT, CLK_INC), the feedback clocks (FB_INT, FB_INC), the LVC MOS program pins (OE, OS) and the Analog Power input (AV_{DD}). When OE is low, the outputs (except FB_OUTT/FB_OUTC) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to GND or V_{DDQ}. When OS is high, OE will function as described above. When OS is low, OE has no effect on CLKT7/CLKC7 (they are free running in addition to FB_OUTT/FB_OUTC). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock signals (CLK_INT, CLK_INC) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INT, CLK_INC) within the specified stabilization time t_{STAB}.

The PLL in **ICS98ULPA877A** clock driver uses the input clocks (CLK_INT, CLK_INC) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT[0:9], CLKC[0:9]). **ICS98ULPA877A** is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.



ICS98ULPA877A is available in Commercial Temperature Range (0°C to 70°C) and Industrial Temperature Range (-40°C to +85°C). See Ordering Information for details

Function Table

| Inputs | | | | | Outputs | | | | PLL |
|-----------|----|----|---------|---------|---------------------------|---------------------------|---------|---------|--------------|
| AVDD | OE | OS | CLK_INT | CLK_INC | CLKT | CLKC | FB_OUTT | FB_OUTC | |
| GND | H | X | L | H | L | H | L | H | Bypassed/Off |
| GND | H | X | H | L | H | L | H | L | Bypassed/Off |
| GND | L | H | L | H | *L(Z) | *L(Z) | L | H | Bypassed/Off |
| GND | L | L | H | L | *L(Z), CLKT7 active | *L(Z), CLKC7 active | H | L | Bypassed/Off |
| 1.8V(nom) | L | H | L | H | *L(Z) | *L(Z) | L | H | On |
| 1.8V(nom) | L | L | H | L | *L(Z), CLKT7 active | *L(Z), CLKC7 active | H | L | On |
| 1.8V(nom) | H | X | L | H | L | H | L | H | On |
| 1.8V(nom) | H | X | H | L | H | L | H | L | On |
| 1.8V(nom) | X | X | L | L | *L(Z) | *L(Z) | *L(Z) | *L(Z) | Off |
| 1.8V(nom) | X | X | H | H | Reserved | | | | |

*L(Z) means the outputs are disabled to a low stated meeting the I_{ODL} limit.



Absolute Maximum Ratings

| | |
|-------------------------------|---------------------------------------|
| Supply Voltage (VDDQ & AVDD) | -0.5V to 2.5V |
| Logic Inputs | GND - 0.5V to V _{DDQ} + 0.5V |
| Ambient Operating Temperature | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;
 Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|---|------------------------|------|------|-------|
| Input High Current (CLK_INT, CLK_INC) | I _{IH} | V _I = V _{DDQ} or GND | | | ±250 | μA |
| Input Low Current (OE, OS, FB_INT, FB_INC) | I _{IL} | V _I = V _{DDQ} or GND | | | ±10 | μA |
| Output Disabled Low Current | I _{ODL} | OE = L, V _{ODL} = 100mV | 100 | | | μA |
| Operating Supply Current | I _{DD1.8} | C _L = 0pf @ 410MHz | | | 300 | mA |
| | I _{DDL} | C _L = 0pf | | | 500 | μA |
| Input Clamp Voltage | V _{IK} | V _{DDQ} = 1.7V I _{in} = -18mA | | | -1.2 | V |
| High-level output voltage | V _{OH} | I _{OH} = -100 μA | V _{DDQ} - 0.2 | | | V |
| | | I _{OH} = -9 mA | 1.1 | 1.45 | | V |
| Low-level output voltage | V _{OL} | I _{OL} = 100 μA | | 0.25 | 0.10 | V |
| | | I _{OL} = 9 mA | | | 0.6 | V |
| Input Capacitance ¹ | C _{IN} | V _I = GND or V _{DDQ} | 2 | | 3 | pF |
| Output Capacitance ¹ | C _{OUT} | V _{OUT} = GND or V _{DDQ} | 2 | | 3 | pF |

¹Guaranteed by design, not 100% tested in production.



Recommended Operating Condition (see note1)

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;

Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------------------------|---------------------------------------|----------------------------|--------------------|----------------------------|-------|
| Supply Voltage | V _{DDQ} , A _{VDD} | | 1.7 | 1.8 | 1.9 | V |
| Low level input voltage | V _{IL} | CLK_INT, CLK_INC, FB_INC, FB_INT | | | 0.35 x V _{DDQ} | V |
| | | OE, OS | | | 0.35 x V _{DDQ} | V |
| High level input voltage | V _{IH} | CLK_INT, CLK_INC, FB_INC, FB_INT | 0.65 x V _{DDQ} | | | V |
| | | OE, OS | 0.65 x V _{DDQ} | | | V |
| DC input signal voltage (note 2) | V _{IN} | | -0.3 | | V _{DDQ} + 0.3 | V |
| Differential input signal voltage (note 3) | V _{ID} | DC - CLK_INT, CLK_INC, FB_INC, FB_INT | 0.3 | | V _{DDQ} + 0.4 | V |
| | | AC - CLK_INT, CLK_INC, FB_INC, FB_INT | 0.6 | | V _{DDQ} + 0.4 | V |
| Output differential cross-voltage (note 4) | V _{OX} | | V _{DDQ} /2 - 0.10 | | V _{DDQ} /2 + 0.10 | V |
| Input differential cross-voltage (note 4) | V _{IX} | | V _{DDQ} /2 - 0.15 | V _{DD} /2 | V _{DDQ} /2 + 0.15 | V |
| High level output current | I _{OH} | | | | -9 | mA |
| Low level output current | I _{OL} | | | | 9 | mA |
| Operating free-air temperature | T _A | | -40 | | 85 | °C |

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signal must be crossing.



Timing Requirements

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;

Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|-----------------------------|---------------------|------------------|-----|-----|-------|
| Max clock frequency | freq _{op} | 1.8V±0.1V @ 25°C | 95 | 410 | MHz |
| Application Frequency Range | freq _{App} | 1.8V±0.1V @ 25°C | 160 | 410 | MHz |
| Input clock duty cycle | d _{tin} | | 40 | 60 | % |
| CLK stabilization | T _{STAB} | | | 15 | µs |

NOTE: The PLL must be able to handle spread spectrum induced skew.

NOTE: Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)

NOTE: Application clock frequency indicates a range over which the PLL must meet all timing parameters.

NOTE: Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal, within the value specified by the Static Phase Offset (t_{ϕ}), after power-up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and CK# go to a logic low state, enter the power-down mode and later return to active operation. CK and CK# may be left floating after they have been driven low for one complete clock cycle.



Switching Characteristics¹

Commercial: TA = 0°C - 70°C; Industrial: TA = -40°C - +85°C;
 Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITION | (MHz) | MIN | TYP | MAX | UNITS | |
|---|----------------------|--------------------------|------------|------------|------|-------|-------|----|
| Output enable time | t_{en} | OE to any output | 160 to 410 | | 4.73 | 8 | ns | |
| Output disable time | t_{dis} | OE to any output | | | 5.82 | 8 | ns | |
| Period jitter | $t_{jit(per)}$ | | 160 to 270 | -40 | | 40 | ps | |
| | | | 271 to 410 | -30 | | 30 | ps | |
| Half-period jitter | $t_{jit(hper)}$ | | 160 to 270 | -60 | | 60 | ps | |
| | | | 271 to 410 | -50 | | 50 | ps | |
| Input slew rate | SLr1(i) | Input Clock | 160 to 410 | 1 | 2.5 | 4 | v/ns | |
| | | Output Enable (OE), (OS) | | 0.5 | | | v/ns | |
| Output clock slew rate | SLr1(o) | 1.5 | | 2.5 | 3 | v/ns | | |
| Cycle-to-cycle period jitter | $t_{jit(cc+)}$ | | | 0 | | 40 | ps | |
| | $t_{jit(cc-)}$ | | | 0 | | -40 | ps | |
| Dynamic Phase Offset | $t_{(\emptyset)dyn}$ | | | 160 to 270 | -50 | | 50 | ps |
| | | | | 271 to 410 | -20 | | 20 | ps |
| Static Phase Offset | t_{SPO}^2 | | | 271 to 410 | -50 | 0 | 50 | ps |
| $t_{jit(per)} + t_{(\emptyset)dyn} + t_{skew(o)}$ | $\sum_{(su)}$ | | | | | | 80 | ps |
| $t_{(\emptyset)dyn} + t_{skew(o)}$ | $\sum_{(h)}$ | | | | | | 60 | ps |
| Output to Output Skew | t_{skew} | | 160 to 270 | | | 40 | ps | |
| | | | 271 to 410 | | | 30 | ps | |
| SSC modulation frequency | | | | 30.00 | | 33 | kHz | |
| SSC clock input frequency deviation | | | | 0.00 | | -0.50 | % | |
| PLL Loop bandwidth (-3 dB from unity gain) | | | | 2.0 | | | MHz | |

Notes:

1. Switching characteristics guaranteed for application frequency range.
2. Static phase offset shifted by design.



Parameter Measurement Information

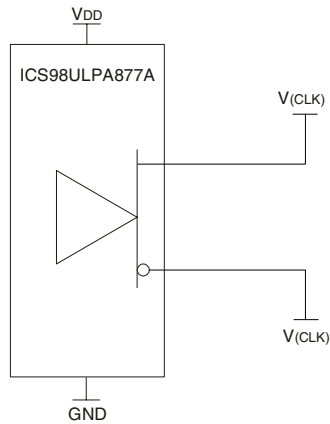


Figure 1: IBIS Model Output Load

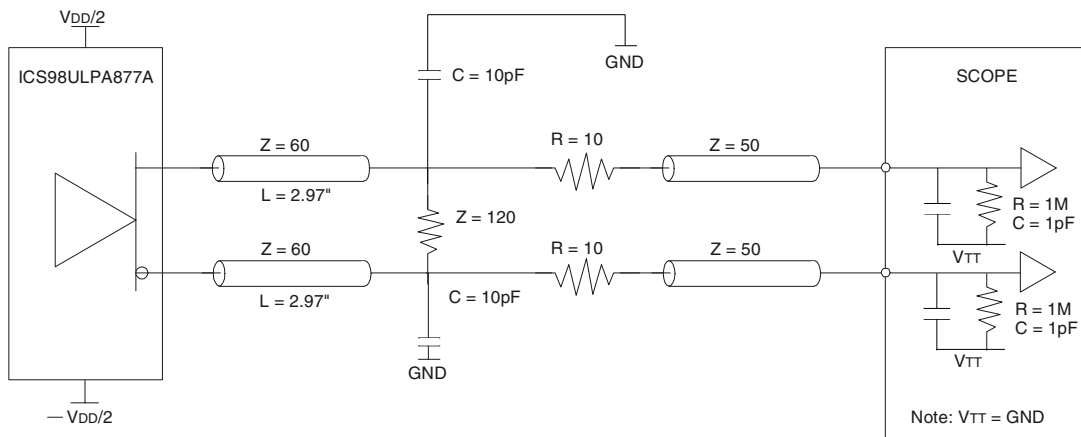


Figure 2: Output Load Test Circuit

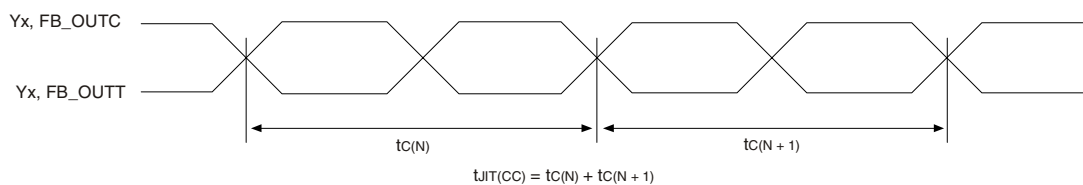


Figure 3: Cycle-to-Cycle Jitter



Parameter Measurement Information

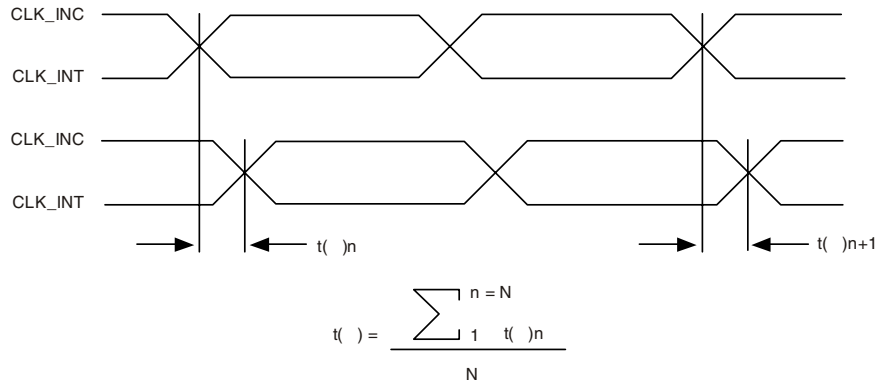


Figure 4: Static Phase Offset

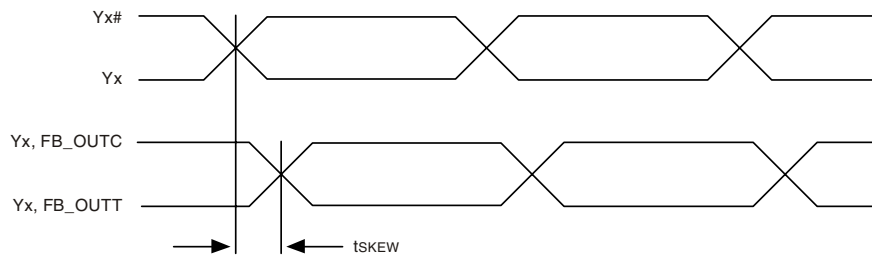
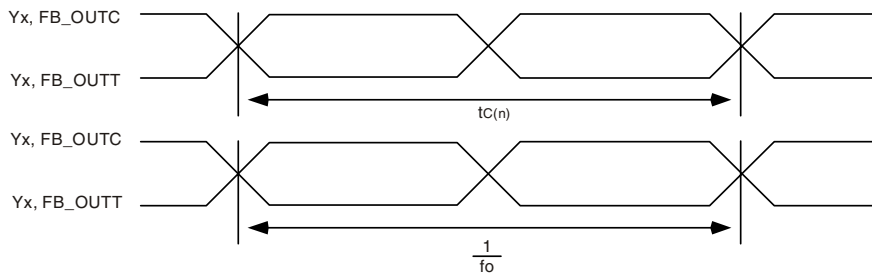


Figure 5: Output Skew

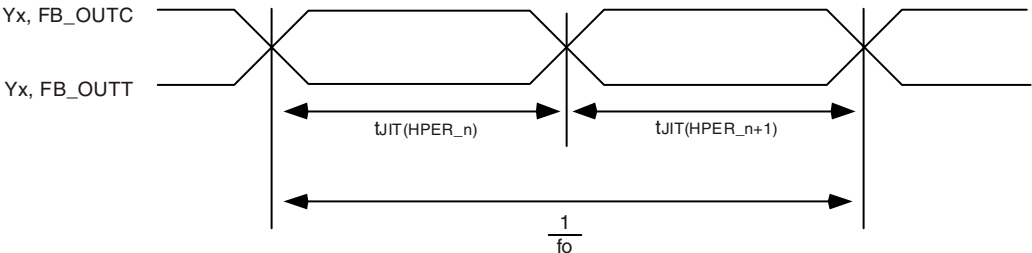


$$t(JIT_PER) = tC(n) - \frac{1}{f_o}$$

Figure 6: Period Jitter



Parameter Measurement Information



$$tJIT(HPER) = tJIT(HPER_n) - \frac{1}{2xfo}$$

Figure 7: Half-Period Jitter

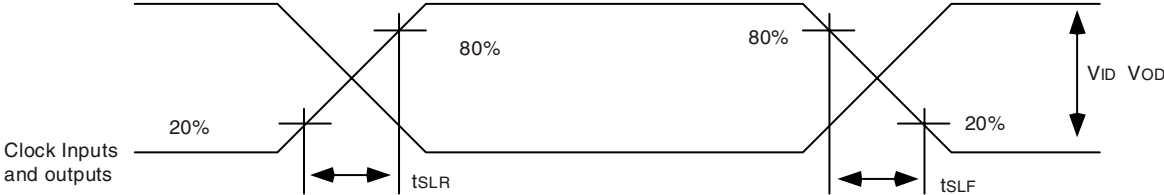


Figure 8: Input and Output Slew Rates

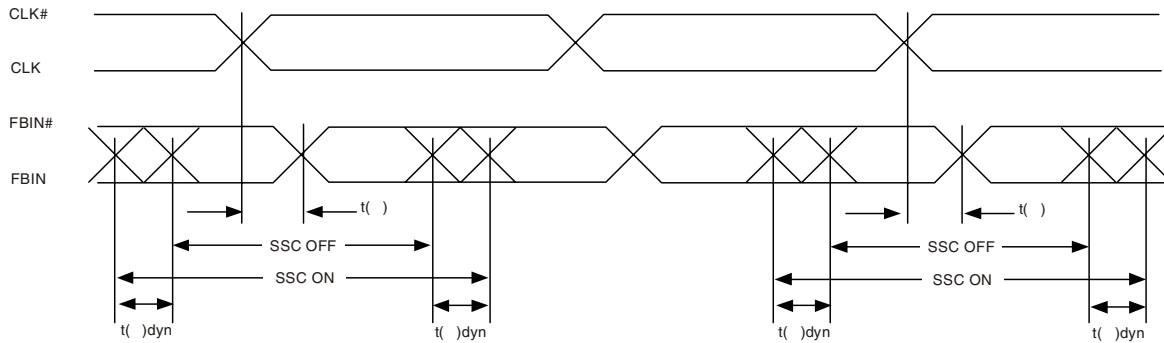


Figure 9: Dynamic Phase Offset

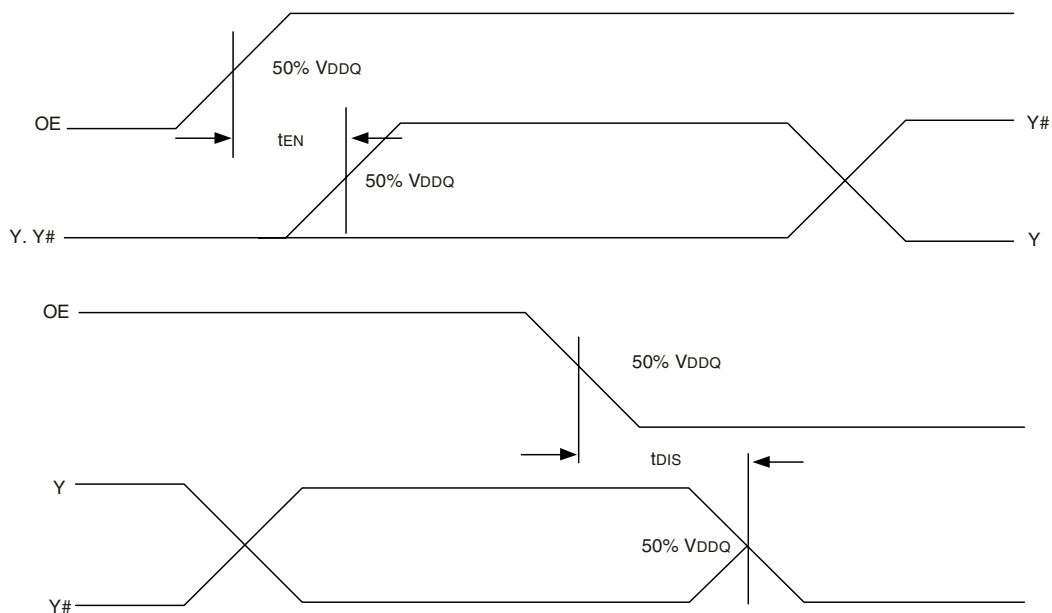


Figure 10: Time Delay Between OE and Clock Output (Y, Y#)

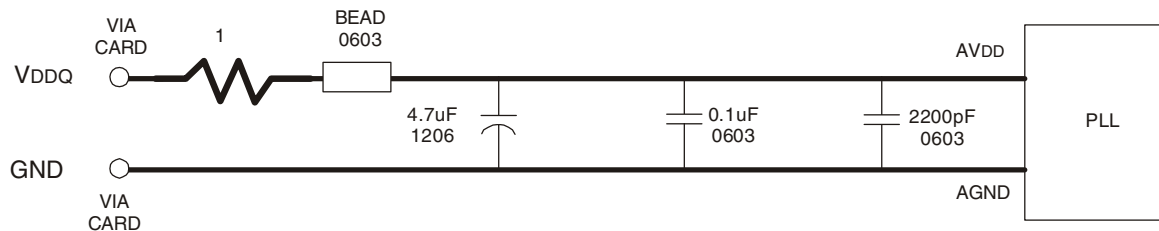
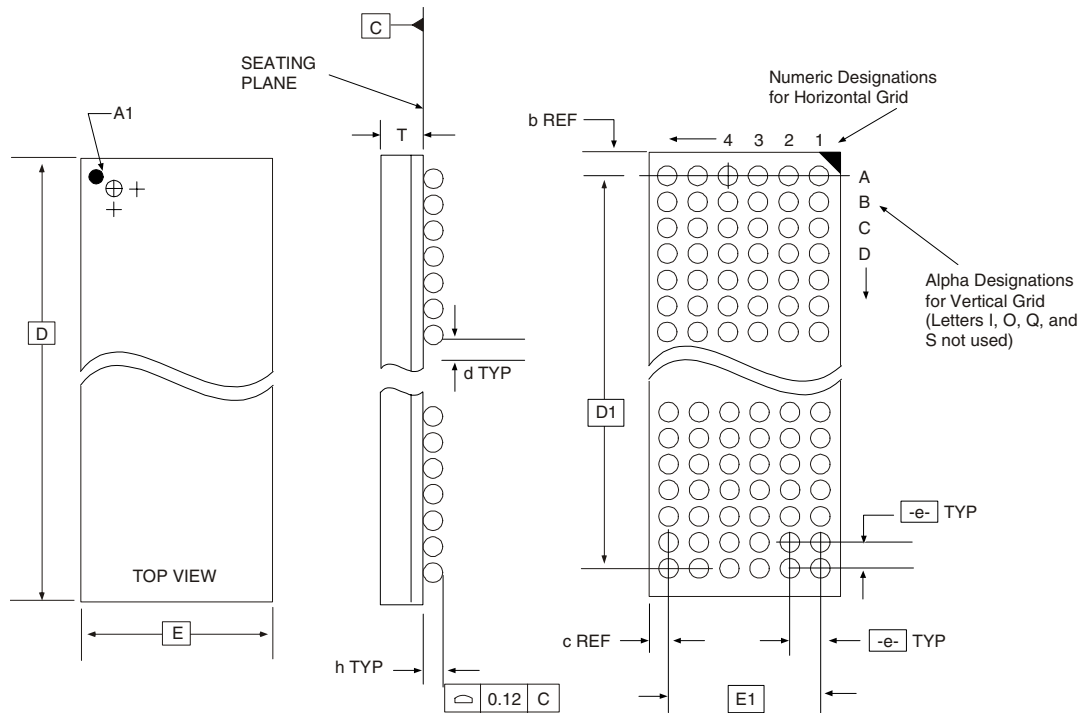


Figure 11. AVDD Filtering

- *Place the 2200pF capacitors close to the PLL.
- *Use wide traces for PLL Analog power and GND. Connect PLL and caps to AGND trace and connect trace to one GND via (farthest from PLL).
- *Recommended bead: Fair-rite P/N 2506036017Y0 or equivalent (0.8 DC max., 600 at 100MHz).



ALL DIMENSIONS IN MILLIMETERS

| D | E | T Min/Max | e | BALL GRID | | Max. TOTAL | d Min/Max | h Min/Max | D1 | E1 | REF. DIMENSIONS | |
|----------|----------|--------------|----------|-----------|------|---------------|--------------|--------------|----------|----------|-----------------|-------|
| | | | | HORIZ | VERT | | | | | | b | c |
| 7.00 Bsc | 4.50 Bsc | 0.86/1.00 | 0.65 Bsc | 6 | 10 | 60 | 0.25/0.45 | 0.15/0.31 | 5.85 Bsc | 3.25 Bsc | 0.575 | 0.625 |

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205*, MO-225**

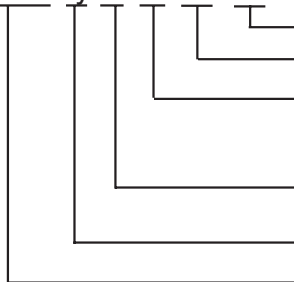
10-0055

Ordering Information

98ULPA877AHLFT

Example:

XXXX y H z LF T



Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

Temperature Grade

Blank = 0°C to +70°C (Commercial)

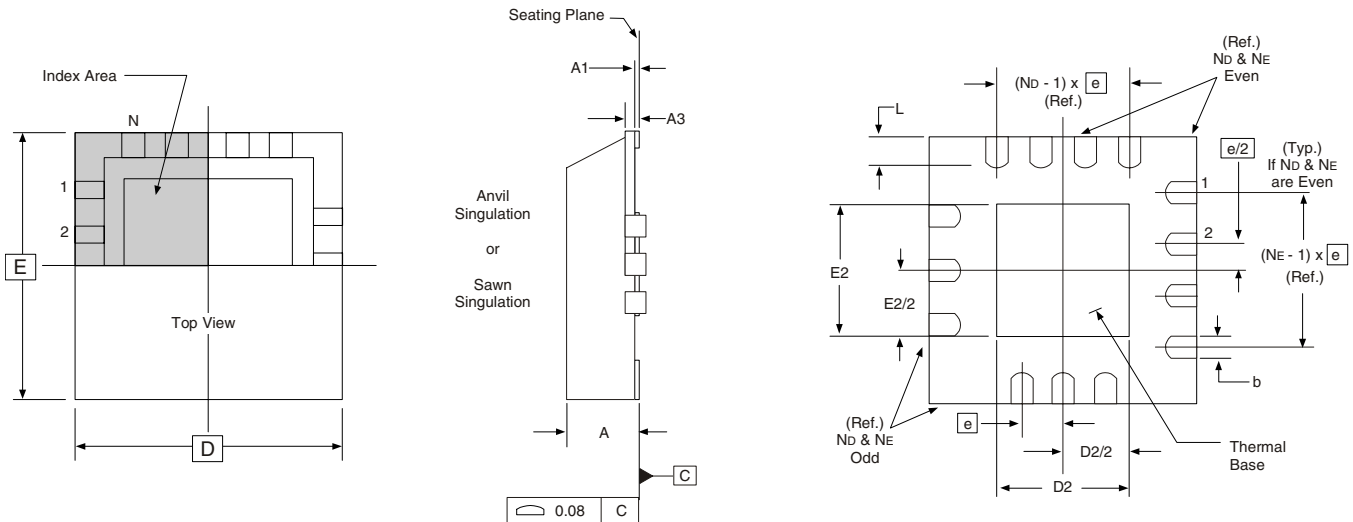
I = -40°C to +85°C (Industrial)

Package Type

H = BGA

Revision Designator (will not correlate with datasheet revision)

Device Type



THERMALLY ENHANCED, VERY THIN, FINE PITCH QUAD FLAT / NO LEAD PLASTIC PACKAGE

ALL DIMENSIONS IN MILLIMETERS

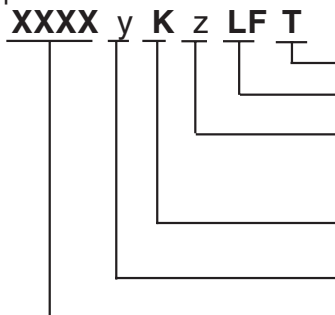
| | | SYMBOL | MIN. | MAX. |
|----------------|-------------|--------|----------------|------|
| N | 40 | | | |
| N _D | 10 | A | 0.80 | 1.00 |
| N _E | 10 | A1 | 0 | 0.05 |
| D x E BASIC | 6.00 x 6.00 | A3 | 0.25 Reference | |
| D2 MIN. / MAX. | 2.75 / 3.05 | b | 0.18 | 0.30 |
| E2 MIN. / MAX. | 2.75 / 3.05 | e | 0.50 BASIC | |
| L MIN. / MAX. | 0.30 / 0.50 | | | |

Source Reference: MLF2™ †
10-0053

Ordering Information

98ULPA877AKLFT

Example:



Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

Temperature Grade

Blank = 0°C to +70°C (Commercial)

I = -40°C to +85°C (Industrial)

Package Type

K = MLF

Revision Designator (will not correlate with datasheet revision)

Device Type