

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



1.8V PHASE LOCKED LOOP DIFFERENTIAL 1:10 SDRAM CLOCK DRIVER

IDTCSPU877D

FEATURES:

- 1 to 10 differential clock distribution
- Optimized for clock distribution in DDR2 (Double Data Rate) SDRAM applications
- Operating frequency: 125MHz to 340MHz
- Very low skew: $\leq 40\text{ps}$
- Very low jitter: $\leq 40\text{ps}$
- 1.8V AVDD and 1.8V VDDO
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Available in 52-Ball VFBGA and 40-pin MLF packages

APPLICATIONS:

- Meets or exceeds JEDEC standard 82.8 for registered DDR2 clock driver
- Along with SSTU32864/65/66, DDR2 register, provides complete solution for DDR2 DIMMs

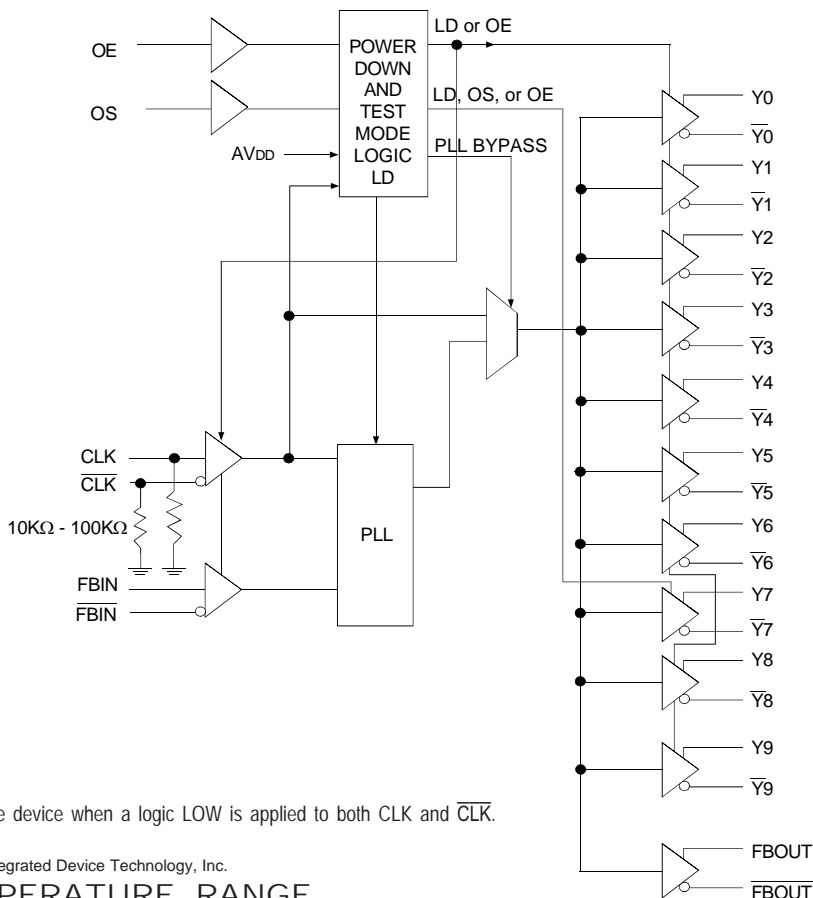
DESCRIPTION:

The CSPU877D is a PLL based clock driver that acts as a zero delay buffer to distribute one differential clock input pair (CLK, $\overline{\text{CLK}}$) to 10 differential output pairs ($\overline{\text{Y}}[0:9]$, Y [0:9]) and one differential pair of feedback clock output (FBOUT, $\overline{\text{FBOUT}}$). External feedback pins (FBIN, $\overline{\text{FBIN}}$) for synchronization of the outputs to the input reference is provided. OE, OS, and AVDD control the power-down and test mode logic. When AVDD is grounded, the PLL is turned off and bypassed for test mode purposes. When the differential clock inputs (CLK, $\overline{\text{CLK}}$) are both at logic low, this device will enter a low power-down mode. In this mode, the receivers are disabled, the PLL is turned off, and the output clock drivers are disabled, resulting in a current consumption device of less than 500 μA .

The CSPU877D requires no external components and has been optimized for very low phase error, skew, and jitter, while maintaining frequency and duty cycle over the operating voltage and temperature range. The CSPU877D, designed for use in both module assemblies and system motherboard based solutions, provides an optimum high-performance clock source.

The CSPU877D is available in Commercial Temperature Range (0°C to +70°C). See Ordering Information for details.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

The Logic Detect (LD) powers down the device when a logic LOW is applied to both CLK and $\overline{\text{CLK}}$.

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

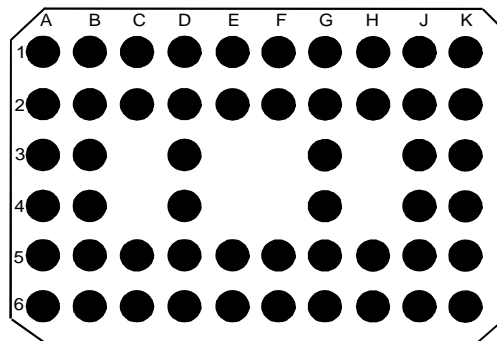
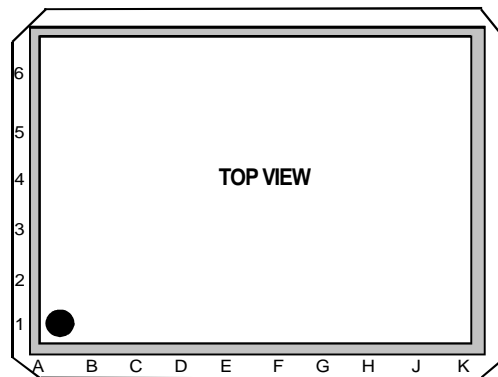
AUGUST 2004

PIN CONFIGURATION

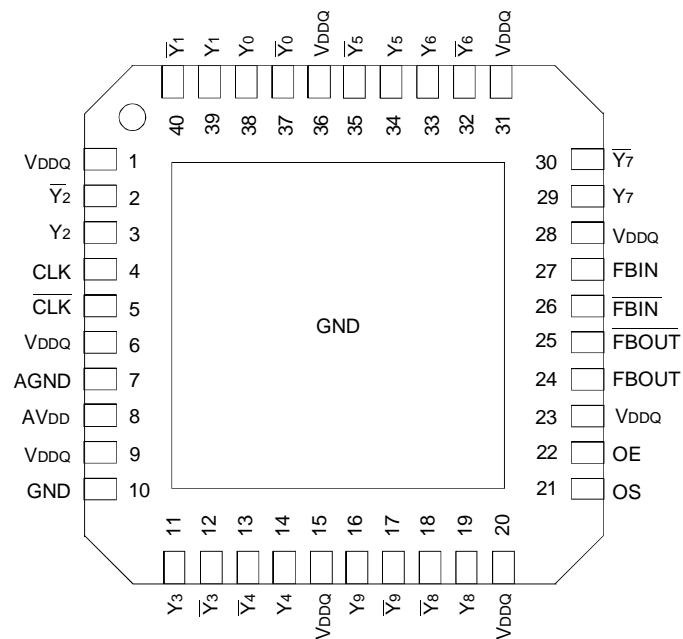
6	Y6	$\overline{Y6}$	$\overline{Y7}$	Y7	FBIN	\overline{FBIN}	$\overline{FBOU7}$	FBOU7	Y8	$\overline{Y8}$
5	Y5	GND	GND	OS	VDDQ	OE	VDDQ	GND	GND	$\overline{Y9}$
4	$\overline{Y5}$	GND	NB	VDDQ	NB	NB	VDDQ	NB	GND	Y9
3	$\overline{Y0}$	GND	NB	VDDQ	NB	NB	VDDQ	NB	GND	Y4
2	Y0	GND	GND	VDDQ	VDDQ	VDDQ	VDDQ	GND	GND	$\overline{Y4}$
1	Y1	$\overline{Y1}$	$\overline{Y2}$	Y2	CLK	\overline{CLK}	AGND	AVDD	Y3	$\overline{Y3}$
	A	B	C	D	E	F	G	H	J	K

VFBGA
TOP VIEW

52 BALL VFBGA PACKAGE LAYOUT



PIN CONFIGURATION



MLF
TOP VIEW

ABSOLUTE MAXIMUM RATINGS^(1,2)

Symbol	Rating	Max	Unit
V _{DDQ} , AV _{DD}	Supply Voltage Range	-0.5 to +2.5	V
V _I ⁽³⁾	Input Voltage Range	-0.5 to V _{DDQ} + 0.5	V
V _O ⁽³⁾	Voltage range applied to any output in the high or low state	-0.5 to V _{DDQ} + 0.5	V
I _{IK} (V _I < 0)	Input clamp current	±50	mA
I _{OK} (V _O < 0 or V _O > V _{DDQ})	Output Clamp Current	±50	mA
I _O (V _O = 0 to V _{DDQ})	Continuous Output Current	±50	mA
V _{DDQ} or GND	Continuous Current	±100	mA
TSTG	Storage Temperature Range	- 65 to +150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 2.5V max.

CAPACITANCE⁽¹⁾

Parameter	Description	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance V _I = V _{DDQ} or GND	2	—	3	pF
C _{IΔ}	Delta Input Capacitance CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$			0.25	pF
C _L	Load Capacitance	—	10	—	pF

NOTE:

- Unused inputs must be held high or low to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV _{DD} ⁽¹⁾	Supply Voltage		V _{DDQ}		V
V _{DDQ}	I/O Supply Voltage	1.7	1.8	1.9	V
T _A	Operating Free-Air Temperature	0	—	+70	°C

- NOTE:**
- The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are guaranteed.

PIN DESCRIPTION (VFBGA)

Pin Name	Pin Number	Description
AGND	G1	Ground for 1.8V analog supply
AV _{DD}	H1	1.8V analog supply
CLK, $\overline{\text{CLK}}$	E1, F1	Differential clock input with a 10K Ω to 100K Ω pulldown resistor
FBIN, $\overline{\text{FBIN}}$	E6, F6	Feedback differential clock input
$\overline{\text{FBOU}}$, FBOU	G6, H6	Feedback differential clock output
GND	B2 - B5, C2, C5, H2, H5, J2 - J5	Ground
V _{DDQ}	D2 - D4, E2, E5, F2, G2 - G5	1.8V supply
OE	F5	Output Enable
OS	D5	Output Select (tied to GND or V _{DDQ})
$\overline{\text{Y}}_{[0:9]}$	A3, A4, B1, B6, C1, C6, K1, K2, K5, K6	Buffered output of input clock, $\overline{\text{CLK}}$
Y _[0:9]	A1, A2, A5, A6, D1, D6, J1, J6, K3, K4	Buffered output of input clock, CLK
NB		No Ball

PIN DESCRIPTION (MLF)

Pin Name	Pin Number	Description
AGND	7	Ground for 1.8V analog supply
AV _{DD}	8	1.8V analog supply
CLK, $\overline{\text{CLK}}$	4, 5	Differential clock input with a 10K Ω to 100K Ω pulldown resistor
FBIN, $\overline{\text{FBIN}}$	26, 27	Feedback differential clock input
$\overline{\text{FBOU}}$, FBOU	24, 25	Feedback differential clock output
GND	10	Ground
V _{DDQ}	1, 6, 9, 15, 20, 23, 28, 31, 36	1.8V supply
OE	22	Output Enable
OS	21	Output Select (tied to GND or V _{DDQ})
Y _[0:9]	3, 11, 14, 16, 19, 29, 33, 34, 38, 39	Buffered output of input clock, CLK
$\overline{\text{Y}}_{[0:9]}$	2, 12, 13, 17, 18, 30, 32, 35, 37, 40	Buffered output of input clock, $\overline{\text{CLK}}$
NB		No Ball

FUNCTION TABLE(1,2)

INPUTS					OUTPUTS				PLL
AVDD	OE	OS	CLK	$\overline{\text{CLK}}$	Y	$\overline{\text{Y}}$	FBOU $\overline{\text{T}}$	$\overline{\text{FBOU}}$	
GND	H	X	L	H	L	H	L	H	OFF
GND	H	X	H	L	H	L	H	L	OFF
GND	L	H	L	H	L(z)	L(z)	L	H	OFF
GND	L	L	H	L	L(z) Y7 Active	L(z) $\overline{\text{Y7}}$ Active	H	L	OFF
1.8V (nom)	L	H	L	H	L(z)	L(z)	L	H	ON
1.8V (nom)	L	L	H	L	L(z) Y7 Active	L(z) $\overline{\text{Y7}}$ Active	H	L	ON
1.8V (nom)	H	X	L	H	L	H	L	H	ON
1.8V (nom)	H	X	H	L	H	L	H	L	ON
1.8V (nom)	X	X	L ⁽³⁾	L ⁽³⁾	L(z)	L(z)	L(z)	L(z)	OFF
X	X	X	H	H	Reserved				

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
- L(z) means the outputs are disabled to a LOW state, meeting the I_{ODL} limit in DC Electrical Characteristics table.
- The device will enter a low power-down mode when CLK and $\overline{\text{CLK}}$ are both at logic LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{IK}	Input Clamp Voltage (All Inputs)	V _{DDQ} = 1.7V, I _I = -18mA	—	—	-1.2	V
V _{IL} ⁽²⁾	Input LOW Voltage (OE, OS, CLK, $\overline{\text{CLK}}$)		—	—	0.35V _{DDQ}	V
V _{IH} ⁽²⁾	Input HIGH Voltage (OE, OS, CLK, $\overline{\text{CLK}}$)		0.65V _{DDQ}	—	—	
V _{IN} ⁽¹⁾	Input Signal Voltage		-0.3	—	V _{DDQ} + 0.3	V
V _{ID} (DC) ⁽²⁾	DC Input Differential Voltage		0.3	—	V _{DDQ} + 0.4	V
V _{OD} ⁽³⁾	Output Differential Voltage	AVDD/VDDQ = 1.7V	0.5	—	—	V
V _{OH}	Output HIGH Voltage	I _{OH} = -100μA, V _{DDQ} = 1.7V to 1.9V	V _{DDQ} - 0.2	—	—	V
		I _{OH} = -9mA, V _{DDQ} = 1.7V	1.1	—	—	
V _{OL}	Output LOW Voltage	I _{OL} = 100μA, V _{DDQ} = 1.7V to 1.9V	—	—	0.1	V
		I _{OL} = 9mA, V _{DDQ} = 1.7V	—	—	0.6	
I _{ODL}	Output Disabled LOW Current	OE = L, V _{ODL} = 100mV, AVDD/VDDQ = 1.7V	100	—	—	μA
I _{IN}	Input Current	CLK, $\overline{\text{CLK}}$			±250	μA
		OE, OS, FBIN, $\overline{\text{FBIN}}$			±10	
I _{DDL}	Static Supply Current (I _{DDQ} and I _{ADD})	AVDD/VDDQ = Max., CLK and $\overline{\text{CLK}}$ = GND			500	μA
I _{DD}	Dynamic Power Supply Current (I _{DDQ} and I _{ADD}) ^(4,5)	AVDD/VDDQ = Max., CLK = 270MHz			300	mA

NOTES:

- V_{IN} specifies the allowable DC excursion of each different output.
- V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{\text{CLK}}$. The CLK and $\overline{\text{CLK}}$ V_{IH} and V_{IL} limits are used to define the DC LOW and HIGH levels for the power down mode.
- V_{OD} is the magnitude of the difference between the true output level and the complementary level.
- All Outputs are left open (unconnected to PCB).
- Total I_{DD} = I_{DDQ} + I_{ADD} = F_{CK} * C_{PD} * V_{DDQ}, for C_{PD} = (I_{DDQ} + I_{ADD}) / (F_{CK} * V_{DDQ}) where F_{CK} is the input frequency, V_{DDQ} is the power supply, and C_{PD} is the Power Dissipation Capacitance.

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
f _{CLK}	Operating Clock Frequency ^(1,2,3)	125	340	MHz
	Application Clock Frequency ^(1,3,4)	160	340	MHz
t _{DC}	Input Clock Duty Cycle	40	60	%
t _L	Stabilization Time ⁽⁵⁾	—	15	μs

NOTES:

- The PLL will track a spread spectrum clock input.
- Operating clock frequency is the range over which the PLL will lock, but may not meet all timing specifications. To be used only for low speed system debug.
- Will lock to input frequency as low as 30MHz at room temperature and nominal or higher supply voltage (1.8V - 1.9V).
- Application clock frequency is the range over which timing specifications apply.
- Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the PLL circuit to obtain phase lock of its feedback signal to its reference signal when CLK and $\overline{\text{CLK}}$ go to a logic LOW state, enters the power-down mode, and later return to active operation. CLK and $\overline{\text{CLK}}$ may be left floating after they have been driven LOW for one complete clock cycle.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

Symbol	Description	Test Conditions	Min.	Typ. ⁽²⁾	Max.	Unit
t _{PLH} ⁽²⁾	LOW to HIGH Level Propagation Delay Time	AVDD = GND, OE = H, OS = L, CLK to any output		TBD		ns
t _{PHL} ⁽²⁾	HIGH to LOW Level Propagation Delay Time	AVDD = GND, OE = H, OS = L, CLK to any output		TBD		ns
t _{JIT(CC+)}	Jitter (cycle-to-cycle)	166/200/266MHz	0		40	ps
t _{JIT(CC-)}			0		-40	
t _{JIT(PER)} ⁽³⁾	Jitter (period)	166/200/266MHz	-40		40	ps
t _{JIT(HPER)} ⁽³⁾	Half-Period Jitter	166/200/266MHz	-60		60	ps
t _{SLR(O)} ^(1,4)	Output Clock Slew Rate (single-ended)	166/200/266MHz (20% to 80%)	1.5	2.5	3	V/ns
t _{SLR(I)} ^(1,4)	Output Enable (OE)		0.5	—	—	V/ns
	Input Clock Slew Rate		1	2.5	4	
t _(∅) ⁽⁵⁾	Static Phase Offset	166/200/266MHz	-50		50	ps
t _{(∅)DYN}	Dynamic Phase Offset	166/200/266MHz	-50		50	ps
t _{SK(O)}	Output Skew				40	ps
t _{EN}	Output Enable to any Y or $\overline{\text{Y}}$				8	ns
t _{DIS}	Output Disable to any Y or $\overline{\text{Y}}$				8	ns
V _{OX} ⁽⁶⁾	AC Differential Output Crosspoint Voltage	Differential outputs terminated with 120Ω	(V _{DDQ} /2)-0.1		(V _{DDQ} /2)+0.1	V
V _{ID(AC)}	AC Differential Input Voltage		0.6		V _{DDQ} +0.4	V
V _{IX}	AC Differential Input Crosspoint Voltage		(V _{DDQ} /2)-0.15		(V _{DDQ} /2)+0.15	V
The PLL on the CSPU877D will meet all the above test parameters while supporting SSC synthesizers with the following parameters:						
SSC	Modulation Frequency		30	—	33	KHz
SSC	Clock Input Frequency Deviation		0	—	-0.5	%
f _{3dB}	PLL Loop Bandwidth		2			MHz

NOTES:

- There are two different terminations that are used with the above AC tests. The output load shown in figure 1 is used to measure the input and output differential pair cross-voltage only. The output load shown in figure 2 is used to measure all other tests, including input and output slew rates. For consistency, use 50Ω equal length cables with SMA connectors on the test board.
- Refers to transition of non-inverting output.
- Period jitter and half-period jitter specifications are separate specifications that must be met independently of each other.
- To eliminate the impact of input slew rates on static phase offset, the input slew rates of reference clock input (CLK, $\overline{\text{CLK}}$) and feedback clock input (FBIN, $\overline{\text{FBIN}}$) are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these nominal values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- Static phase offset does not include jitter.
- V_{ox} is specified at the DDR DRAM clock input or test load.

TEST CIRCUIT AND SWITCHING WAVEFORMS

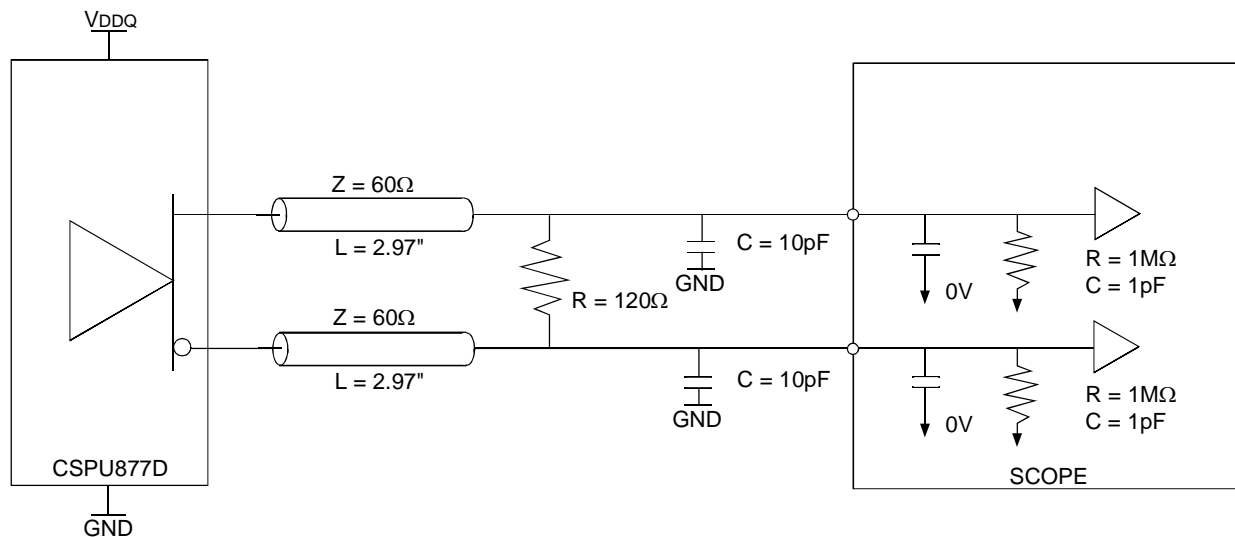


Figure 1: Output Load Test Circuit 1

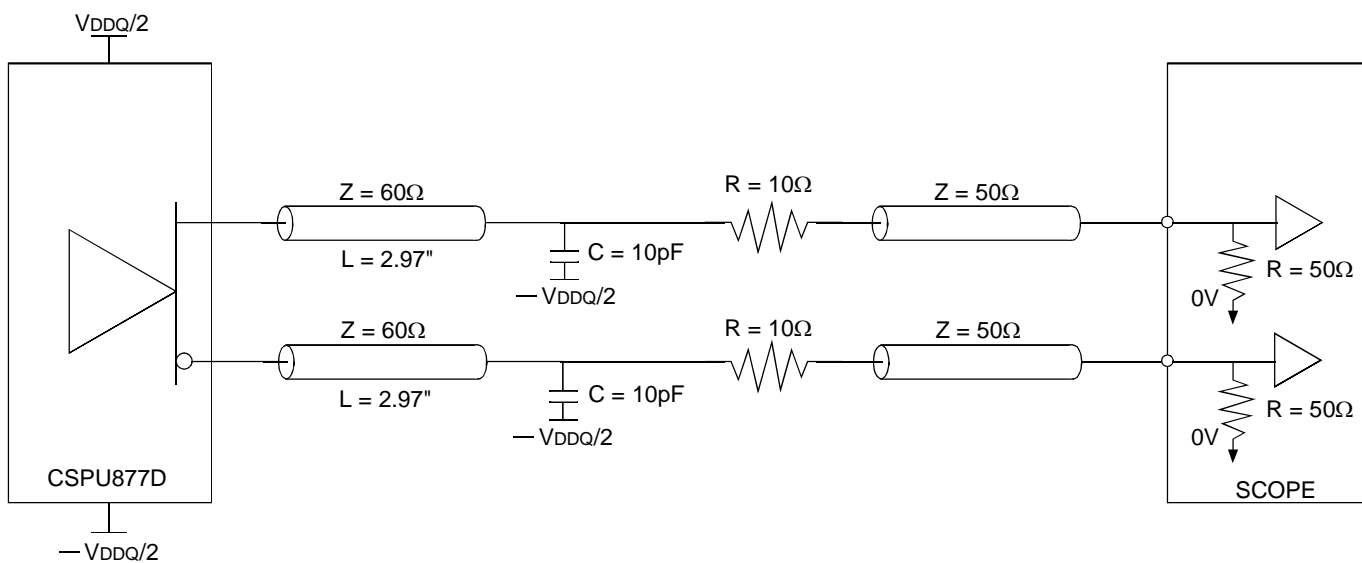
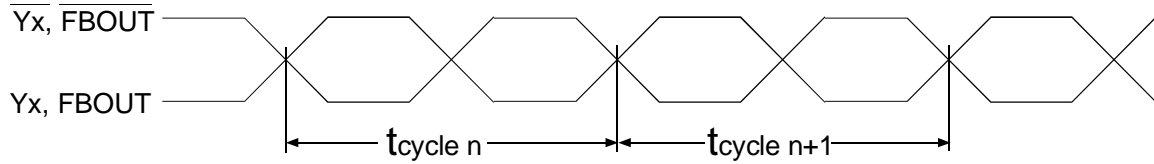


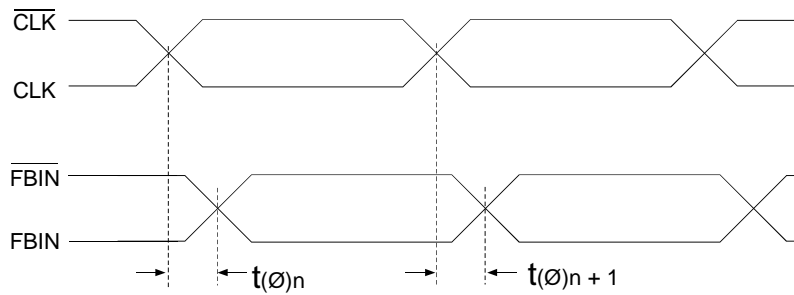
Figure 2: Output Load Test Circuit 2

TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

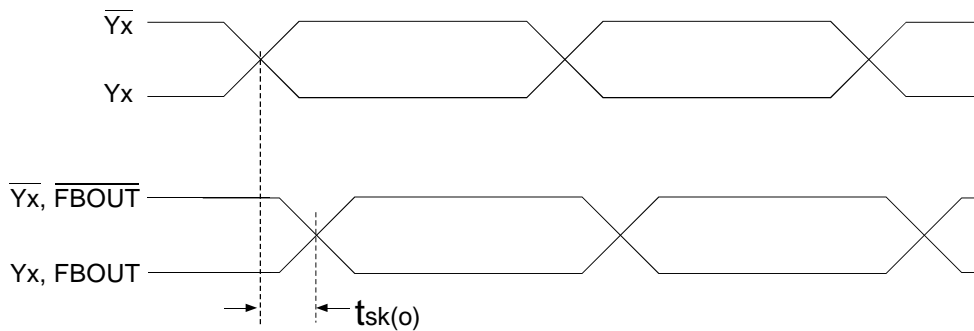
Cycle-to-Cycle jitter



$$t(\varnothing) = \frac{\sum_{n=1}^{n=N} t(\varnothing)_n}{N}$$

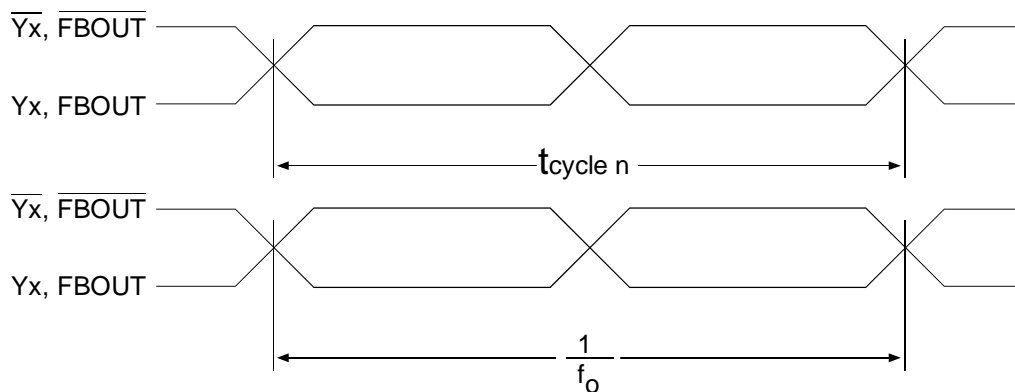
(N is a large number of samples)

Static Phase Offset



Output Skew

TEST CIRCUIT AND SWITCHING WAVEFORMS

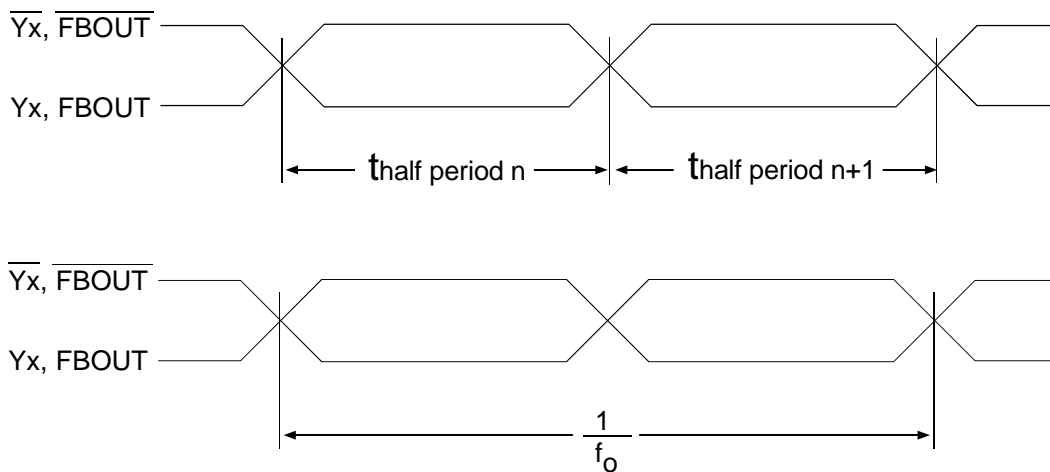


$$t_{\text{jit(per)}} = t_{\text{cycle } n} - \frac{1}{f_0}$$

NOTE:

f_0 = Average input frequency measured at CLK / $\overline{\text{CLK}}$

Period jitter



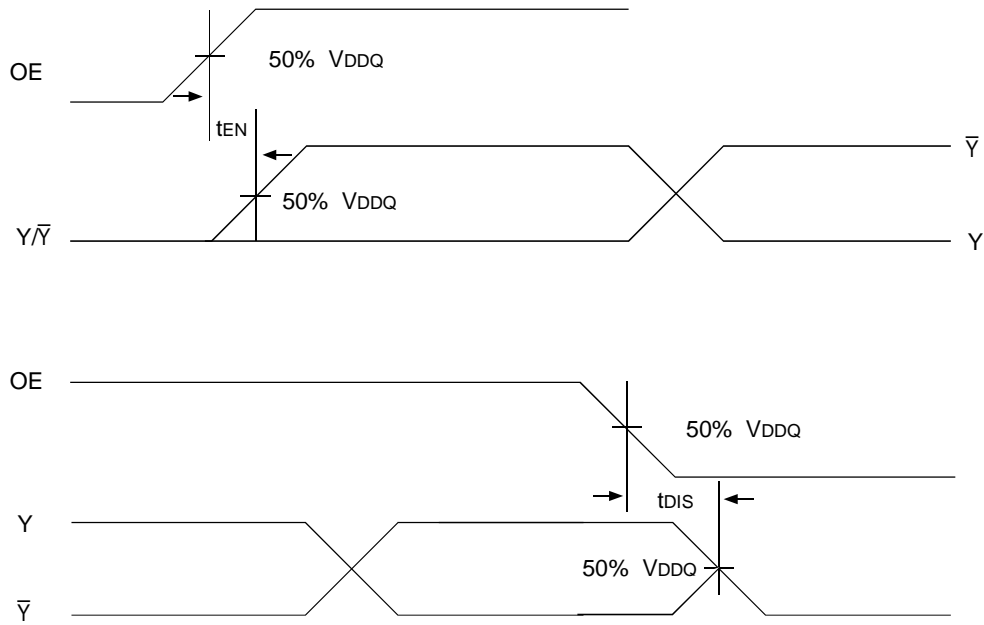
$$t_{\text{jit(hper)}} = t_{\text{half period } n} - \frac{1}{2 \cdot f_0}$$

NOTE:

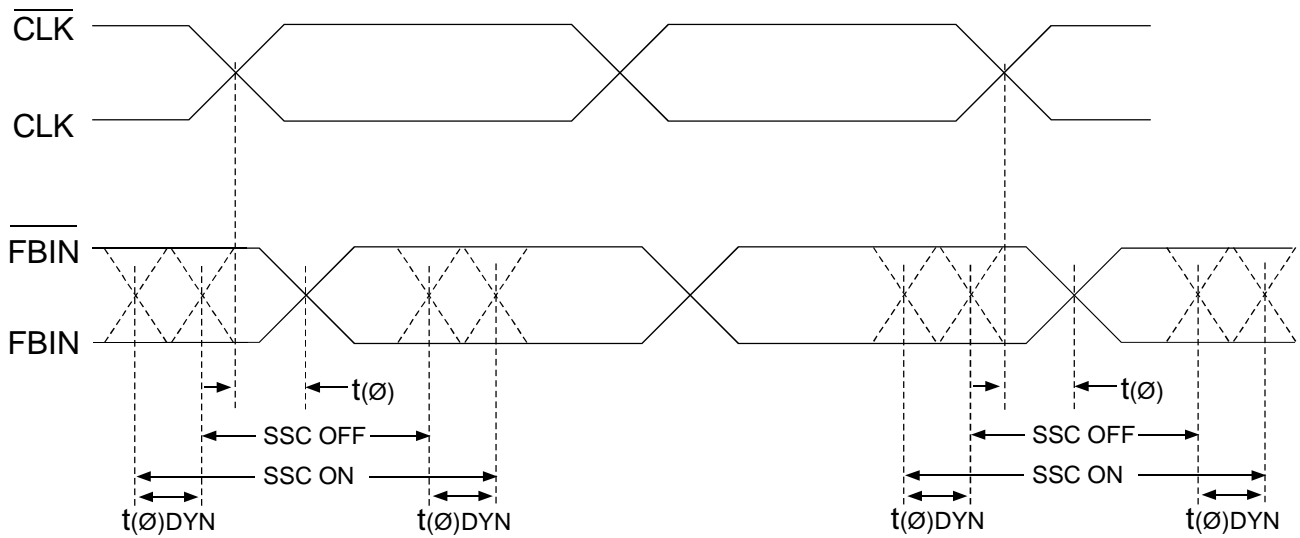
f_0 = Average input frequency measured at CLK / $\overline{\text{CLK}}$

Half-Period jitter

TEST CIRCUIT AND SWITCHING WAVEFORMS

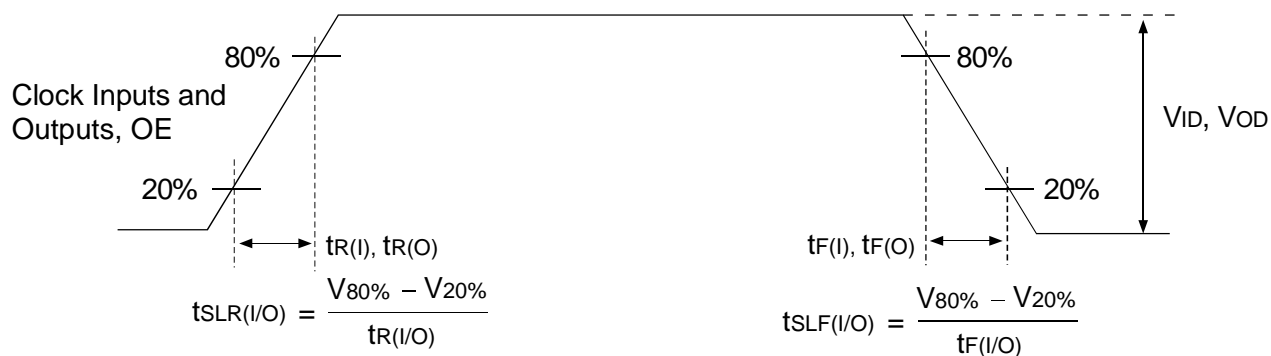


Time Delay Between Output Enable (OE) and Clock Output (Y, \bar{Y})

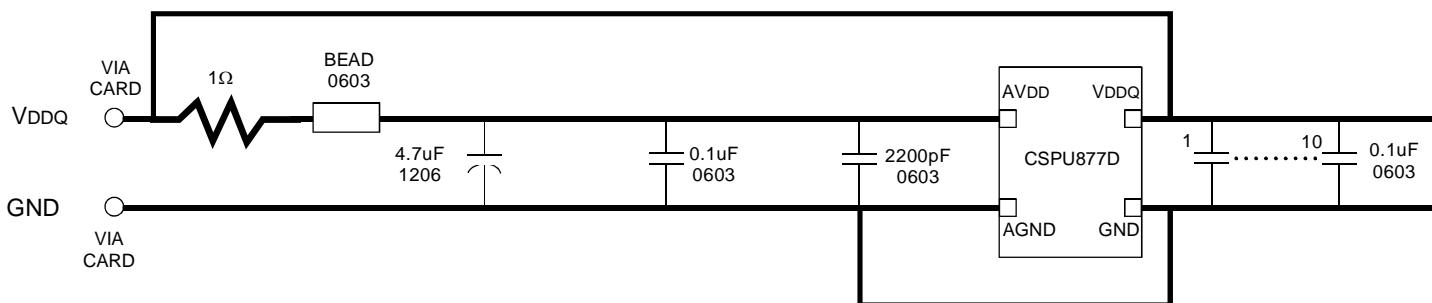


Dynamic Phase Offset

TEST CIRCUIT AND SWITCHING WAVEFORMS



Input and Output Slew Rates



NOTES:

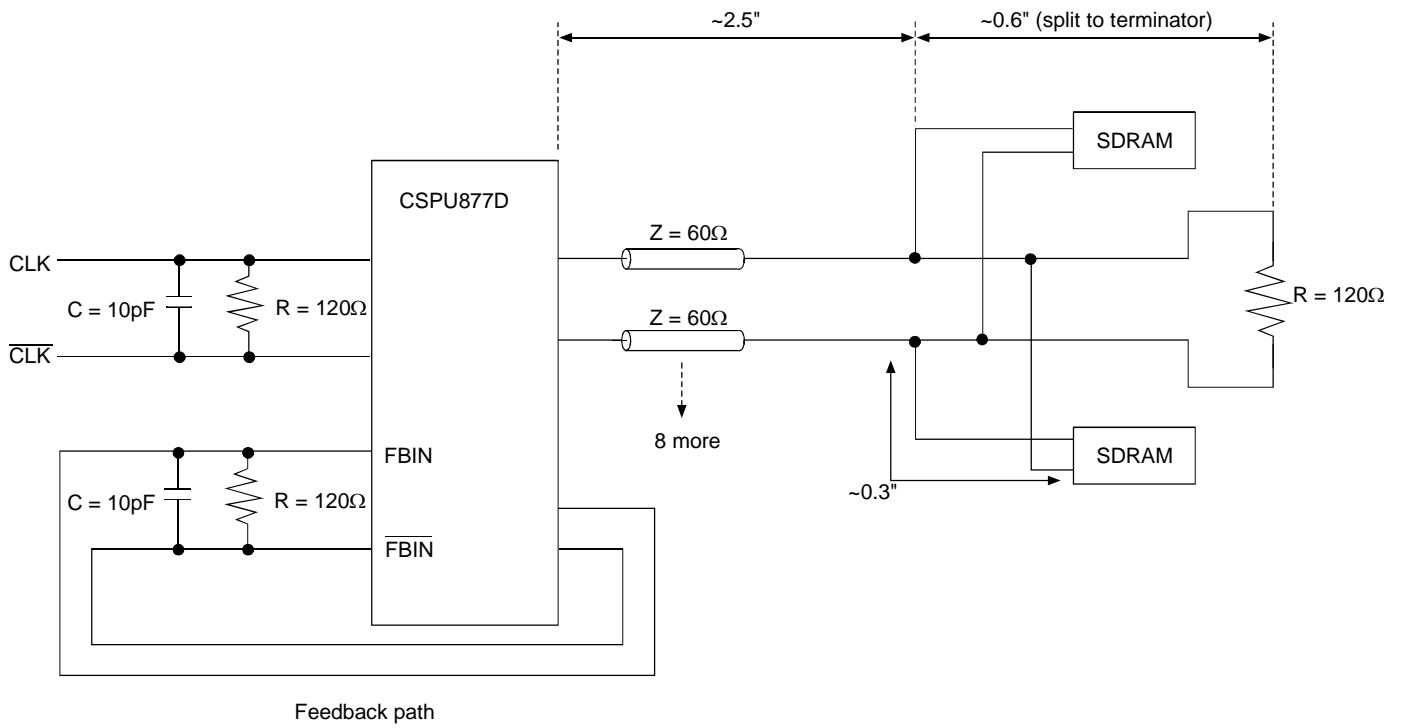
- Place all decoupling capacitors as close to the CSPU877D pins as possible.
- Use wide traces for AVDD and AGND.
- Recommended bead: Fair-rite P/N 2506036017Y0 or equivalent (0.8Ω DC max., 600Ω at 100MHz).

Recommended Filtering for the Analog and Digital Power Supplies (AVDD and VDDQ)

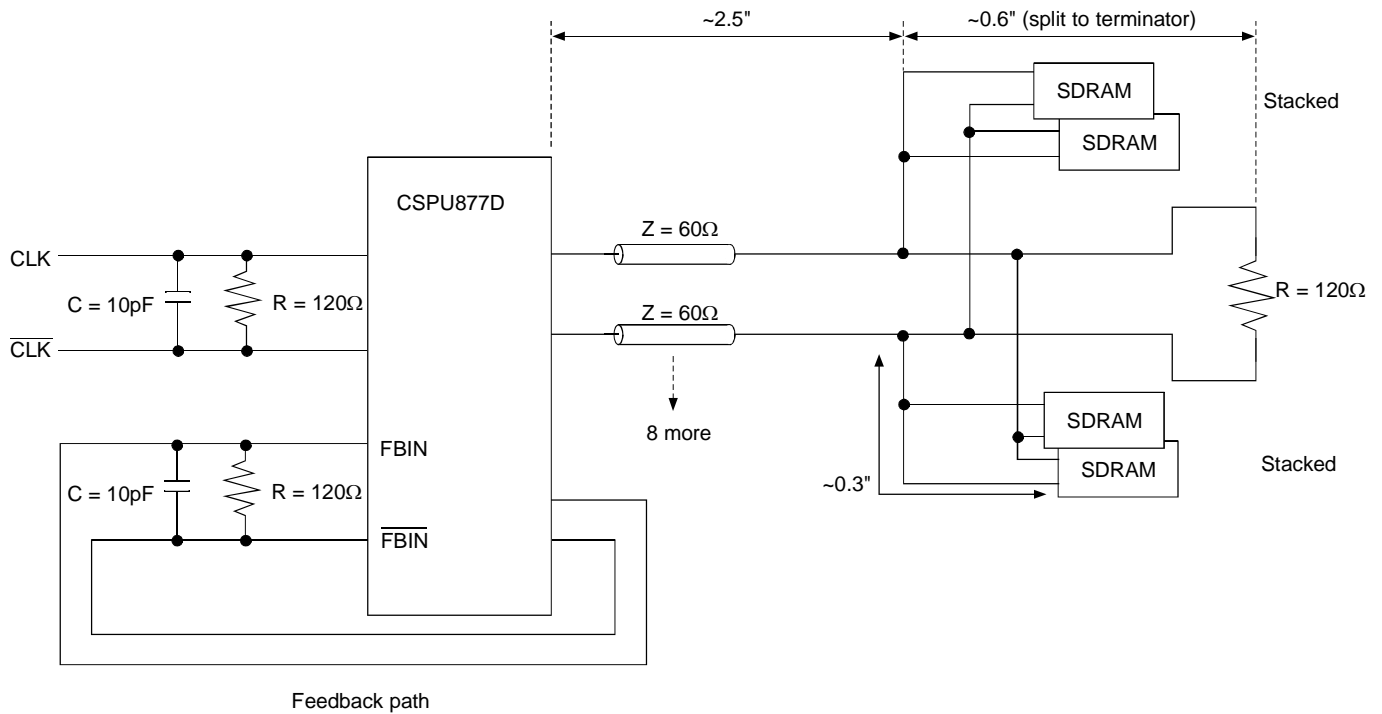
APPLICATION INFORMATION

Clock Structure	# of SDRAM Loads per Clock	Clock Loading on the PLL outputs (pF)	
		Min.	Max.
#1	2	3	5
#2	4	6	10

APPLICATION INFORMATION



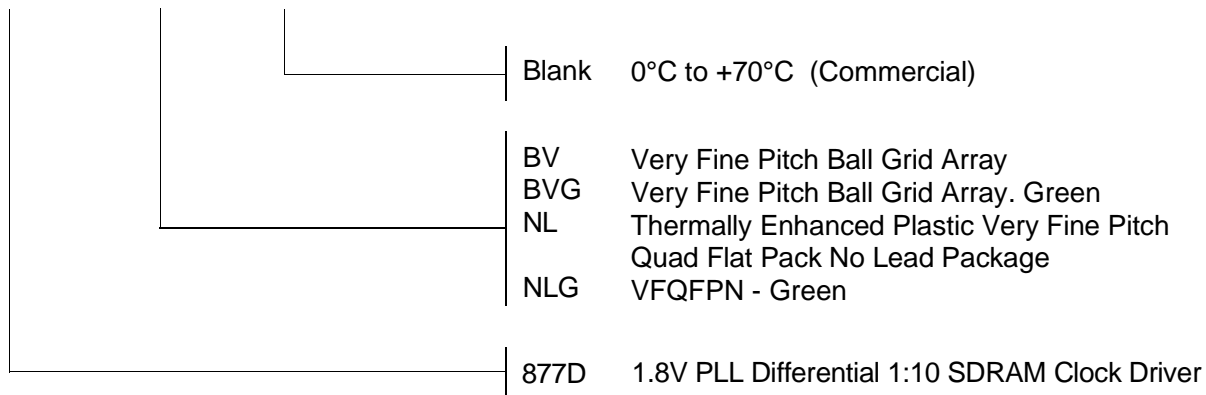
Clock Structure 1



Clock Structure 2

ORDERING INFORMATION

IDTCSPU XXXXX XX X
 Device Type Package Process



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
 (408) 654-6459