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**8-OUTPUT SMALL FORM FACTOR PCIE GEN1-2-3 BUFFER**
**IDT6P61033**
**Description**

The IDT6P61033 is an 8-output very low power buffer for 100MHz PCIe Gen1, Gen2 and Gen3 applications with integrated output terminations providing  $Z_o=100\Omega$ . The device has 8 output enables for clock management, and 3 selectable SMBus addresses.

**Recommended Application**

PCIe Gen1-2-3 Buffer for Freescale designs

**Output Features**

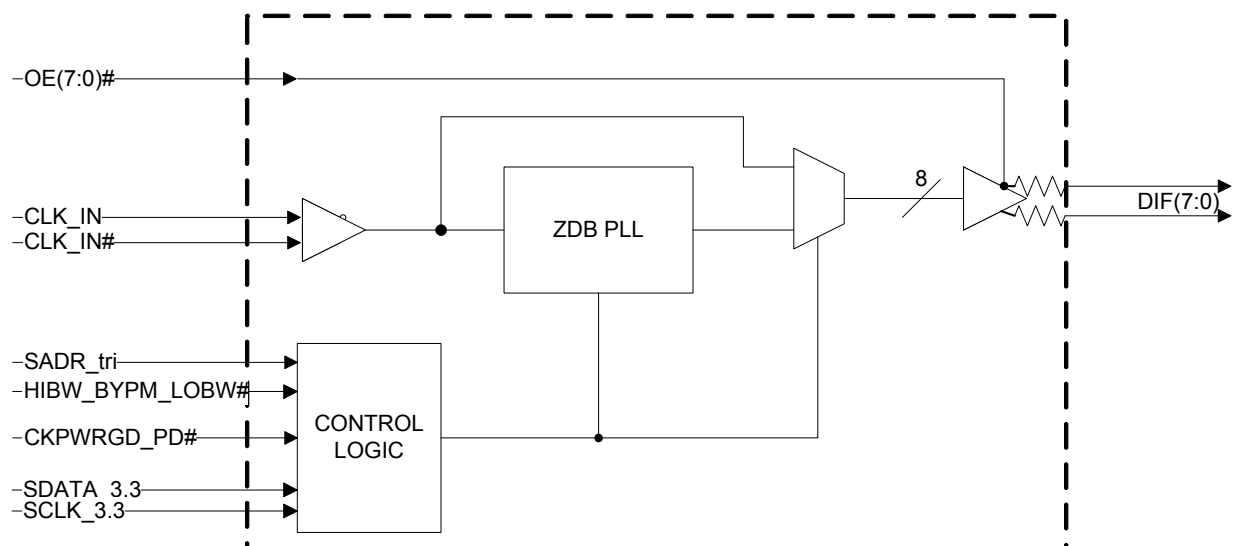
- 8 - 0.7V low-power HCSL-compatible (LP-HCSL) DIF pairs w/ $Z_o=100\Omega$

**Key Specifications**

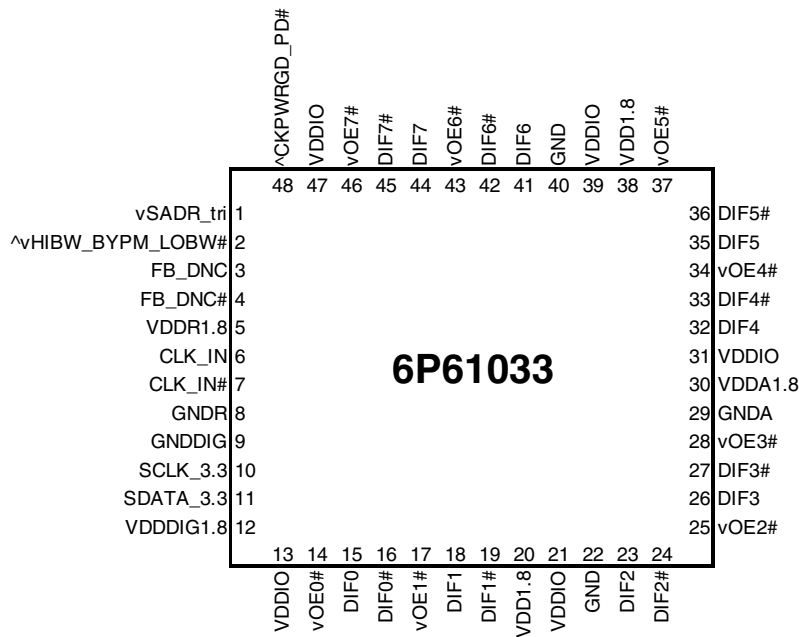
- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- Very low additive phase jitter in bypass mode

**Features/Benefits**

- Integrated terminations provide  $100\Omega$  differential  $Z_o$ ; reduced component count and board space
- 1.8V operation; minimal power consumption
- Outputs can optionally be supplied from any voltage between 1.05 and 1.8V; maximum power savings
- OE# pins; support DIF power management
- HCSL compatible differential input; can be driven by common clock sources
- LP-HCSL differential clock outputs; reduced power and board space
- Programmable Slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- Pin/software selectable PLL bandwidth and PLL Bypass; minimize phase jitter for each application
- Outputs blocked until PLL is locked; clean system start-up
- Software selectable 50MHz or 125MHz PLL operation; useful for Ethernet applications
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 48-pin 6x6mm VFQFPN; minimal board space
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment

**Block Diagram**


## Pin Configuration



### 48-pin VFQFPN, 6x6 mm, 0.4mm pitch

^v prefix indicates internal 120KOhm pull up *AND* pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

^ prefix indicates internal 120KOhm pull up resistor

## SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

## Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On <sup>1</sup>
1	Running	1	0	Running	Running	On <sup>1</sup>
1	Running	1	1	Low	Low	On <sup>1</sup>

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

## Power Connections

Pin Number			Description
VDD	VDDIO	GND	
5		8	Input receiver analog
12		9	Digital Power
20, 31, 38	13, 21, 31, 39, 47	22, 29, 40	DIF outputs
30		29	PLL Analog

## Frequency Select Table

FSEL Byte3 [4:3]	CLK_IN (MHz)	DIFx (MHz)
00 (Default)	100.00	CLK_IN
01	50.00	CLK_IN
10	125.00	CLK_IN
11	Reserved	Reserved

## PLL Operating Mode

HiBW BypM LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11

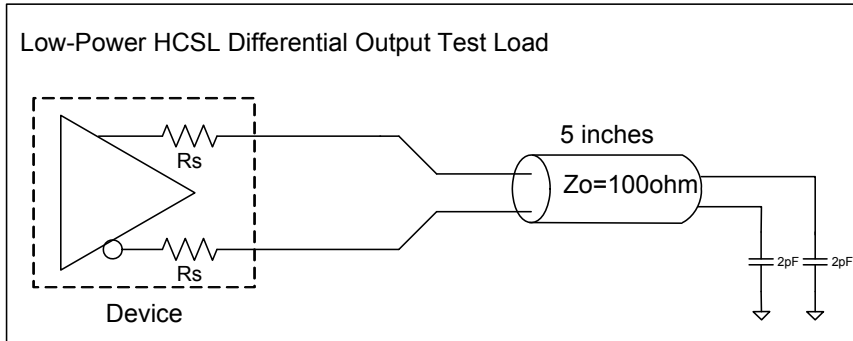
## Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	vSADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. See SMBus Address Selection Table.
2	^vHIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
3	FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
4	FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
5	VDDR1.8	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
6	CLK_IN	IN	True Input for differential reference clock.
7	CLK_IN#	IN	Complementary Input for differential reference clock.
8	GNDR	GND	Analog Ground pin for the differential input (receiver)
9	GNDDIG	GND	Ground pin for digital circuitry
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	VDDDIG1.8	PWR	1.8V digital power (dirty power)
13	VDDIO	PWR	Power supply for differential outputs
14	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
15	DIF0	OUT	Differential true clock output
16	DIF0#	OUT	Differential Complementary clock output
17	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	VDD1.8	PWR	Power supply, nominal 1.8V
21	VDDIO	PWR	Power supply for differential outputs
22	GND	GND	Ground pin.
23	DIF2	OUT	Differential true clock output
24	DIF2#	OUT	Differential Complementary clock output
25	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
26	DIF3	OUT	Differential true clock output
27	DIF3#	OUT	Differential Complementary clock output
28	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
29	GNDA	GND	Ground pin for the PLL core.
30	VDDA1.8	PWR	1.8V power for the PLL core.
31	VDDIO	PWR	Power supply for differential outputs
32	DIF4	OUT	Differential true clock output
33	DIF4#	OUT	Differential Complementary clock output
34	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
35	DIF5	OUT	Differential true clock output
36	DIF5#	OUT	Differential Complementary clock output
37	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
38	VDD1.8	PWR	Power supply, nominal 1.8V

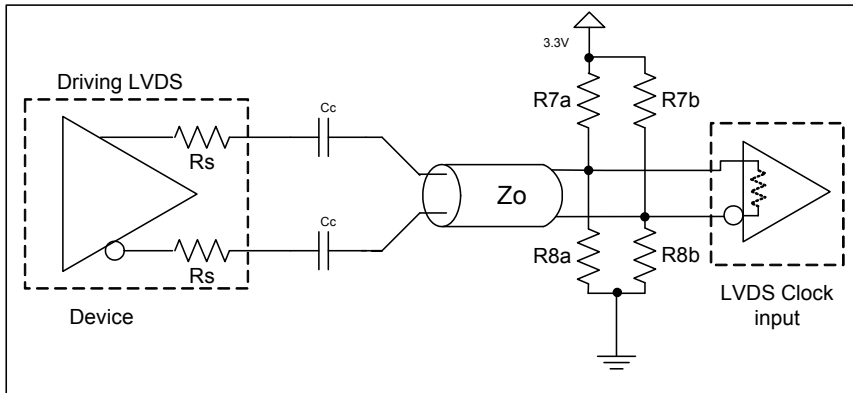
**Pin Descriptions (cont.)**

39	VDDIO	PWR	Power supply for differential outputs
40	GND	GND	Ground pin.
41	DIF6	OUT	Differential true clock output
42	DIF6#	OUT	Differential Complementary clock output
43	vOE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
44	DIF7	OUT	Differential true clock output
45	DIF7#	OUT	Differential Complementary clock output
46	vOE7#	IN	Active low input for enabling DIF pair 7. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
47	VDDIO	PWR	Power supply for differential outputs
48	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.

## Test Loads



## Driving LVDS



### Driving LVDS inputs

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
$C_c$	0.1 uF	0.1 uF	
$V_{cm}$	1.2 volts	1.2 volts	

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT6P61033. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
1.8V Supply Voltage	VDDxx	Applies to VDD, VDDA and VDDIO	-0.5		2.5	V	1,2
Input Voltage	V <sub>IN</sub>		-0.5		V <sub>DD</sub> +0.5V	V	1, 3
Input High Voltage, SMBus	V <sub>IHSMB</sub>	SMBus clock and data pins			3.6V	V	1
Storage Temperature	T <sub>s</sub>		-65		150	°C	1
Junction Temperature	T <sub>j</sub>				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup>Not to exceed 2.5V.

## Electrical Characteristics–Clock Input Parameters

T<sub>A</sub> = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V <sub>IHDIF</sub>	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V <sub>ILDIF</sub>	Differential inputs (single-ended measurement)	V <sub>SS</sub> - 300	0	300	mV	1,3
Input Common Mode Voltage - DIF_IN	V <sub>COM</sub>	Common Mode Input Voltage	300		725	mV	1
Input Amplitude - DIF_IN	V <sub>SWING</sub>	Peak to Peak value (V <sub>IHDIF</sub> - V <sub>ILDIF</sub> )	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4			V/ns	1,2
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-5	0.01	5	uA	1
Input Duty Cycle	d <sub>tin</sub>	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J <sub>DIFin</sub>	Differential Measurement	0		150	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through +/-75mV window centered around differential zero

<sup>3</sup>The device can be driven from a single ended clock by driving the true clock and biasing the complement clock input to the V<sub>BIAS</sub>, where V<sub>BIAS</sub> is (V<sub>IHIGH</sub> - V<sub>ILOW</sub>)/2

## Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
1.8V Supply Voltage	VDD	Supply voltage for core, analog and LVCMOS outputs	1.7	1.8	1.9	V	1
IO Supply Voltage	VDDIO	Supply voltage for differential Low Power Outputs	0.9975	1.05	1.9	V	1
Ambient Operating Temperature	T <sub>COM</sub>	Commercial range	0	25	70	°C	1
	T <sub>IND</sub>	Industrial range	-40	25	85	°C	1
Input High Voltage	V <sub>IH</sub>	Single-ended inputs, except SMBus	0.75 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	1
Input Mid Voltage	V <sub>IM</sub>	Single-ended tri-level inputs ('_tri' suffix)	0.4 V <sub>DD</sub>		0.6 V <sub>DD</sub>	V	1
Input Low Voltage	V <sub>IL</sub>	Single-ended inputs, except SMBus	-0.3		0.25 V <sub>DD</sub>	V	1
Schmitt Trigger Positive Going Threshold Voltage	V <sub>T+</sub>	Single-ended inputs, where indicated	0.4 V <sub>DD</sub>		0.7 V <sub>DD</sub>	V	1
Schmitt Trigger Negative Going Threshold Voltage	V <sub>T-</sub>	Single-ended inputs, where indicated	0.1 V <sub>DD</sub>		0.4 V <sub>DD</sub>	V	1
Hysteresis Voltage	V <sub>H</sub>	V <sub>T+</sub> - V <sub>T-</sub>	0.1 V <sub>DD</sub>		0.4 V <sub>DD</sub>	V	1
Output High Voltage	V <sub>IH</sub>	Single-ended outputs, except SMBus. I <sub>OH</sub> = -2mA	V <sub>DD</sub> -0.45			V	1
Output Low Voltage	V <sub>IL</sub>	Single-ended outputs, except SMBus. I <sub>OL</sub> = -2mA			0.45	V	1
Input Current	I <sub>IN</sub>	Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD	-5		5	uA	1
	I <sub>INP</sub>	Single-ended inputs V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F <sub>ibyp</sub>	Bypass mode	1		200	MHz	2
	F <sub>ipll100</sub>	100MHz PLL mode	60	100.00	110	MHz	2
	F <sub>ipll125</sub>	125MHz PLL mode	75	125.00	137.5	MHz	2
	F <sub>ipll156</sub>	156.25MHz PLL mode	93.75	156.25	171.875	MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
Capacitance	C <sub>IN</sub>	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C <sub>INDIF_IN</sub>	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
Clk Stabilization	T <sub>STAB</sub>	From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.600	1	ms	1,2
Input SS Modulation Frequency	f <sub>MODIN</sub>	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz	1
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t <sub>DRVPD</sub>	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t <sub>F</sub>	Fall time of single-ended control inputs			5	ns	1,2
Trise	t <sub>R</sub>	Rise time of single-ended control inputs			5	ns	1,2
SMBus Input Low Voltage	V <sub>ILSMB</sub>				0.8	V	1
SMBus Input High Voltage	V <sub>IHSMB</sub>		2.1		3.6	V	1
SMBus Output Low Voltage	V <sub>OLSMB</sub>	@ I <sub>PULLUP</sub>			0.4	V	1
SMBus Sink Current	I <sub>PULLUP</sub>	@ V <sub>OL</sub>	4			mA	1
Nominal Bus Voltage	V <sub>DDSMB</sub>	3.3V bus voltage	2.7		3.6	V	1
SCLK/SDATA Rise Time	t <sub>RSMB</sub>	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t <sub>FSMB</sub>	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f <sub>MAXSMB</sub>	Maximum SMBus operating frequency			400	kHz	1,5

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active



## Electrical Characteristics–DIF 0.7V Low Power HCSL Outputs

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on 3.0V/ns setting	1.1	2	3	V/ns	1, 2, 3
		Scope averaging on 2.0V/ns setting	1.9	3	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		7	20	%	1, 2, 4
Voltage High	V <sub>HIGH</sub>	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	774	850	mV	1, 7
Voltage Low	V <sub>LOW</sub>		-150	18	150		1, 7
Max Voltage	V <sub>max</sub>	Measurement on single ended signal using absolute value. (Scope averaging off)		821	1150	mV	1
Min Voltage	V <sub>min</sub>		-300	-15			1
Vswing	Vswing	Scope averaging off	300	1536		mV	1,2,7
Crossing Voltage (abs)	V <sub>cross_abs</sub>	Scope averaging off	250	414	550	mV	1,5,7
Crossing Voltage (var)	Δ-V <sub>cross</sub>	Scope averaging off		13	140	mV	1, 6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup> V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting Δ-V<sub>cross</sub> to be smaller than V<sub>cross</sub> absolute.

<sup>7</sup> At default SMBus settings.

## Electrical Characteristics–Current Consumption

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I <sub>DDAOP</sub>	VDDA+VDDR, PLL Mode, @100MHz		11	15	mA	1
	I <sub>DDOP</sub>	VDD1.8, All outputs active @100MHz		8	10	mA	1
	I <sub>DDIOOP</sub>	VDDIO, All outputs active @100MHz		28	35	mA	1
Powerdown Current	I <sub>DDAPD</sub>	VDDA+VDDR, PLL Mode, @100MHz		0.7	1	mA	1,2
	I <sub>DDPD</sub>	VDD1.8, Outputs Low/Low		1.2	2	mA	1, 2
	I <sub>DDIODZ</sub>	VDDIO, Outputs Low/Low	0.005	0.01		mA	1, 2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Input clock stopped.

## Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	2.7	4	MHz	1,5
		-3dB point in Low BW Mode	1	1.4	2	MHz	1,5
PLL Jitter Peaking	t <sub>JPEAK</sub>	Peak Pass band Gain		1.2	2	dB	1
Duty Cycle	t <sub>DC</sub>	Measured differentially, PLL Mode	45	50.1	55	%	1
Duty Cycle Distortion	t <sub>DCD</sub>	Measured differentially, Bypass Mode @100MHz	-1	0	1	%	1,3
Skew, Input to Output	t <sub>pdBYP</sub>	Bypass Mode, V <sub>T</sub> = 50%	3000	3600	4500	ps	1
	t <sub>pdPLL</sub>	PLL Mode V <sub>T</sub> = 50%	0	92	200	ps	1,4
Skew, Output to Output	t <sub>sk3</sub>	V <sub>T</sub> = 50%		28	50	ps	1,4
Jitter, Cycle to cycle	t <sub>jcyc-cyc</sub>	PLL mode		16	50	ps	1,2
		Additive Jitter in Bypass Mode		0.1	25	ps	1,2

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

<sup>4</sup> All outputs at default slew rate

<sup>5</sup> The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

## Electrical Characteristics–Phase Jitter Parameters

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage per VDD, VDDIO of normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	t <sub>jphPCIEG1</sub>	PCIe Gen 1		34	52	86	ps (p-p)	1,2,3
	t <sub>jphPCIEG2</sub>	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.9	1.4	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.2	2.5	3.1	ps (rms)	1,2
	t <sub>jphPCIEG3</sub>	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	0.6	1	ps (rms)	1,2,4
	t <sub>jphSGMII</sub>	125MHz, 1.5MHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		1.9	2	NA	ps (rms)	1,6
Additive Phase Jitter, Bypass Mode	t <sub>jphPCIEG1</sub>	PCIe Gen 1		0.6	5	N/A	ps (p-p)	1,2,3
	t <sub>jphPCIEG2</sub>	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.3	N/A	ps (rms)	1,2,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.05	0.1	N/A	ps (rms)	1,2,5
	t <sub>jphPCIEG3</sub>	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.05	0.1	N/A	ps (rms)	1,2,4,5
	t <sub>jphSGMII</sub>	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		0.15	0.3	N/A	ps (rms)	1,6

<sup>1</sup> Applies to all outputs, with device driven by 9FG432AKLF or equivalent.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> Subject to final radification by PCI SIG.

<sup>5</sup> For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>]

<sup>6</sup> Applies to all differential outputs

## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation		
Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
Beginning Byte = N		ACK
Data Byte Count = X		ACK
Beginning Byte N		ACK
O	X Byte	O
O		O
O		O
Byte N + X - 1		ACK
P	stoP bit	

**Note: SMBus Address is Latched on SADR pin.**

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation		
Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
Beginning Byte = N		ACK
RT Repeat starT		ACK
Slave Address		
RD	ReaD	
ACK		ACK
ACK		Data Byte Count=X
O		X Byte
O		
O		
O		
Byte N + X - 1		Beginning Byte N
ACK		O
ACK		O
ACK		O
ACK		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

SMBus Table: Output Enable Register <sup>1</sup>

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE7	Output Enable	RW	Low/Low	Enabled	1
Bit 6	DIF OE6	Output Enable	RW	Low/Low	Enabled	1
Bit 5	DIF OE5	Output Enable	RW	Low/Low	Enabled	1
Bit 4	DIF OE4	Output Enable	RW	Low/Low	Enabled	1
Bit 3	DIF OE3	Output Enable	RW	Low/Low	Enabled	1
Bit 2	DIF OE2	Output Enable	RW	Low/Low	Enabled	1
Bit 1	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 0	DIF OE0	Output Enable	RW	Low/Low	Enabled	1

1. A low on these bits will override the OE# pin and force the differential output Low/Low

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PLLMODERB1	PLL Mode Readback Bit 1	R	See PLL Operating Mode Table		Latch
Bit 6	PLLMODERB0	PLL Mode Readback Bit 0	R			Latch
Bit 5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
Bit 4	PLLMODE1	PLL Mode Control Bit 1	RW <sup>1</sup>	See PLL Operating Mode Table		0
Bit 3	PLLMODE0	PLL Mode Control Bit 0	RW <sup>1</sup>			0
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.7V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.8V	11 = 0.9V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL DIF7	Adjust Slew Rate of DIF7	RW	2.0V/ns	3.0V/ns	1
Bit 6	SLEWRATESEL DIF6	Adjust Slew Rate of DIF6	RW	2.0V/ns	3.0V/ns	1
Bit 5	SLEWRATESEL DIF5	Adjust Slew Rate of DIF5	RW	2.0V/ns	3.0V/ns	1
Bit 4	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	2.0V/ns	3.0V/ns	1
Bit 3	SLEWRATESEL DIF3	Adjust Slew Rate of DIF3	RW	2.0V/ns	3.0V/ns	1
Bit 2	SLEWRATESEL DIF2	Adjust Slew Rate of DIF2	RW	2.0V/ns	3.0V/ns	1
Bit 1	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	2.0V/ns	3.0V/ns	1
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	2.0V/ns	3.0V/ns	1

SMBus Table: Frequency Select Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	FREQ_SEL_EN	Enable SW selection of frequency	RW	SW frequency change disabled	SW frequency change enabled	0
Bit 4	FSEL1	Freq. Select Bit 1	RW <sup>1</sup>	See Frequency Select Table		0
Bit 3	FSEL0	Freq. Select Bit 0	RW <sup>1</sup>			0
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL FB	Adjust Slew Rate of FB	RW	2.0V/ns	3.0V/ns	1

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

Byte 4 is Reserved and reads back 'hFF'

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

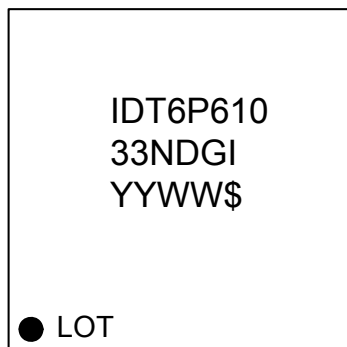
SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGV, 01 = DBV, 10 = DMV, 11 = Reserved		0
Bit 6	Device Type0		R			1
Bit 5	Device ID5	Device ID	R	001000 binary or 08 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			1
Bit 2	Device ID2		R			0
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7		Reserved				0
Bit 6		Reserved				0
Bit 5		Reserved				0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

## Marking Diagram



### Notes:

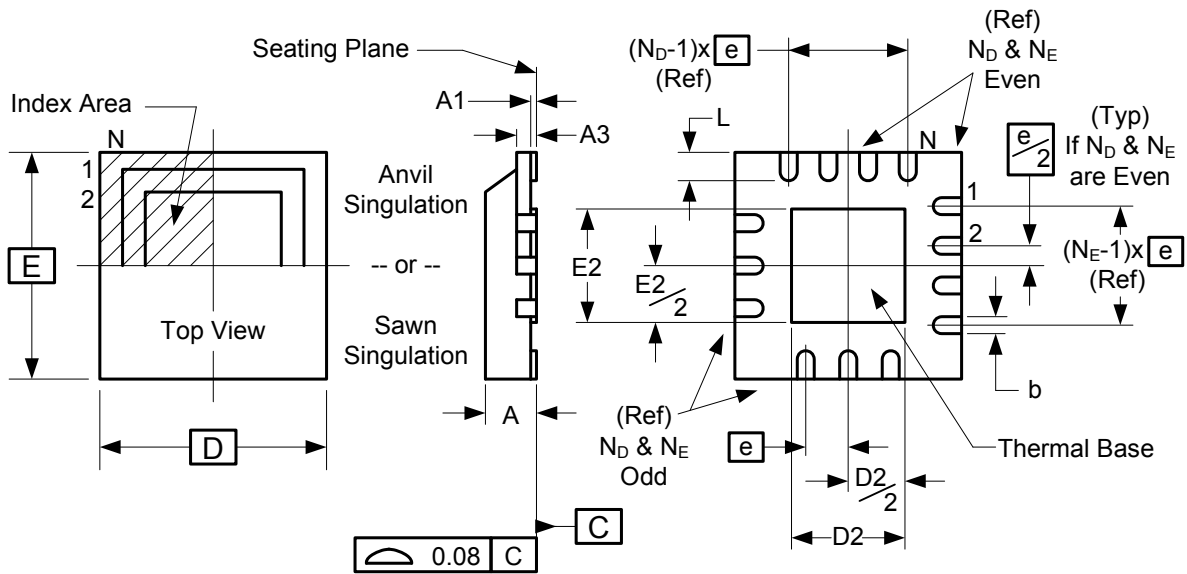
1. "LOT" is the lot sequence number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "\$" is the assembly mark code.
4. "G" denotes RoHS compliant package.
5. "I" denotes industrial temperature range device.

## Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	$\theta_{JC}$	Junction to Case	NDG48	33	°C/W	1
	$\theta_{Jb}$	Junction to Base		2.1	°C/W	1
	$\theta_{JA00}$	Junction to Air, still air		37	°C/W	1
	$\theta_{JA1}$	Junction to Air, 1 m/s air flow		30	°C/W	1
	$\theta_{JA3}$	Junction to Air, 3 m/s air flow		27	°C/W	1
	$\theta_{JA5}$	Junction to Air, 5 m/s air flow		26	°C/W	1

<sup>1</sup>ePad soldered to board

### Package Outline and Package Dimensions (NDG48)



Symbol	Millimeters	
	Min	Max
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.40 BASIC	
D x E BASIC	6.00 x 6.00	
D2 MIN./MAX.	3.95	4.25
E2 MIN./MAX.	3.95	4.25
L MIN./MAX.	0.30	0.50
N <sub>D</sub>	12	
N <sub>E</sub>	12	

### Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
6P61033NDGI	Trays	48-pin VFQFPN	-40 to +85° C
6P61033NDGI8	Tape and Reel	48-pin VFQFPN	-40 to +85° C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

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**Revision History**

Rev.	Issue Date	Initiator	Description	Page #
A	2/25/2013	RDW	Initial Release	-



**IDT6P61033**

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