

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

# NB6L14S

## 2.5 V 1:4 AnyLevel™ Differential Input to LVDS Fanout Buffer/Translator

The NB6L14S is a differential 1:4 Clock or Data Receiver and will accept AnyLevel differential input signals: LVPECL, CML, LVDS, or HSCL. These signals will be translated to LVDS and four identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6L14S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6L14S has a wide input common mode range from  $GND + 50\text{ mV}$  to  $V_{CC} - 50\text{ mV}$ . Combined with the  $50\ \Omega$  internal termination resistors at the inputs, the NB6L14S is ideal for translating a variety of differential or single-ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6L14S is the 2.5 V version of the NB6N14S and is offered in a small 3 mm x 3 mm 16-QFN package. Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

The NB6L14S is a member of the ECLinPS MAX™ family of high performance products.

### Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Single Power Supply;  $V_{CC} = 2.5 \pm 5\%$
- $V_{REF\_AC}$  Reference Output
- These are Pb-Free Devices

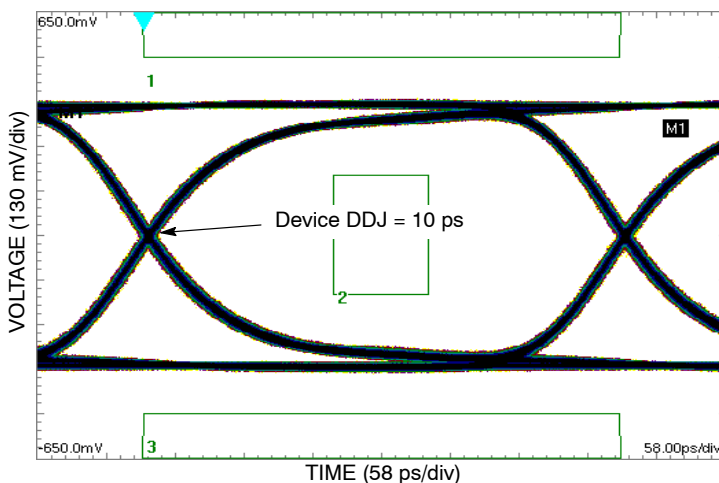


Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400\text{ mV}$ ; Input Signal DDJ = 14 ps)



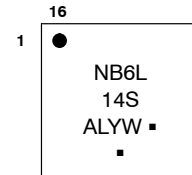
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



QFN-16  
MN SUFFIX  
CASE 485G



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

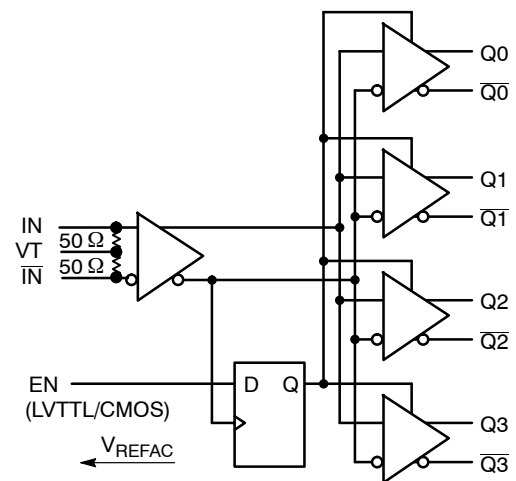


Figure 1. Logic Diagram

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# NB6L14S

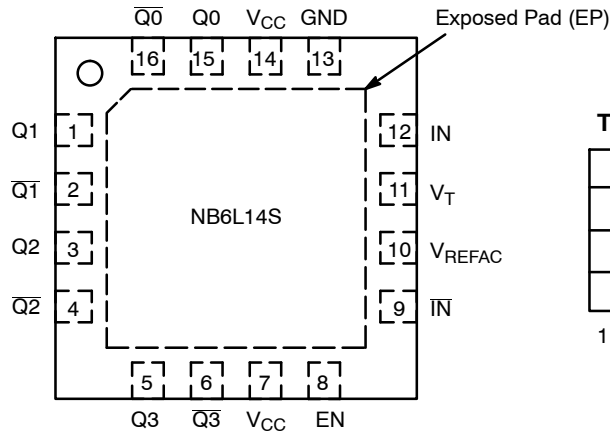


Figure 3. NB6L14S Pinout, 16-pin QFN (Top View)

Table 1. TRUTH TABLE

IN	$\overline{\text{IN}}$	EN	Q	$\overline{\text{Q}}$
0	1	1	0	1
1	0	1	1	0
x	x	0	0 (Note 1)	1 (Note 1)

1. On next transition of the input signal (IN).

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q1	LVDS Output	Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
2	$\overline{\text{Q1}}$	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
3	Q2	LVDS Output	Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
4	$\overline{\text{Q2}}$	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
5	Q3	LVDS Output	Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
6	$\overline{\text{Q3}}$	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
7	V <sub>CC</sub>	-	Positive Supply Voltage.
8	EN	LVTTTL / LVCMOS Input	Synchronous Output Enable. When LOW, Q outputs will go LOW and Qb outputs will go HIGH on the next negative transition of IN input. The internal DFF register is clocked on the falling edge of IN input; see Figure 26. The EN pin has an internal pullup resistor and defaults HIGH when left open.
9	$\overline{\text{IN}}$	LVPECL, CML, LVDS	Inverted Differential Input
10	V <sub>REFAC</sub>	LVPECL Output	The V <sub>REFAC</sub> reference output can only be used to rebias capacitor-coupled differential or single-ended input signals. For the capacitor-coupled IN and/or INb inputs, V <sub>REFAC</sub> should be connected to the VT pin and bypassed to ground with a 0.01 $\mu\text{F}$ capacitor.
11	V <sub>T</sub>	LVPECL Output	Internal 100 $\Omega$ Center-tapped Termination Pin for IN and $\overline{\text{IN}}$
12	IN	LVPECL, CML, LVDS	Non-inverted Differential Input. (Note 2)
13	GND	-	Negative Supply Voltage.
14	V <sub>CC</sub>	-	Positive Supply Voltage.
15	Q0	LVDS Output	Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
16	$\overline{\text{Q0}}$	LVDS Output	Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

2. In the differential configuration, when the input termination pin (VT) is connected to a termination voltage or left open, and if no signal is applied on IN/ $\overline{\text{IN}}$  inputs, then the device will be susceptible to self-oscillation.

# NB6L14S

**Table 3. ATTRIBUTES**

Characteristics	Value
Moisture Sensitivity (Note 3)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
ESD Protection Human Body Model Machine Model	> 2 kV > 200 V
Transistor Count	745
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	Positive Power Supply	GND = 0 V		3.8	V
$V_{IN}$	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	3.8	V
$I_{IN}$	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		35 70	mA mA
$I_{OSC}$	Output Short Circuit Current Line-to-Line (Q to $\bar{Q}$ ) Line-to-End (Q or $\bar{Q}$ to GND)	Q or $\bar{Q}$ Q to $\bar{Q}$ to GND	Continuous Continuous	12 24	mA
$I_{REF\_AC}$	$V_{REF\_AC}$ Sink/Source Current			$\pm 0.5$	mA
$T_A$	Operating Temperature Range	QFN-16		-40 to +85	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}$ C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	$^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	1S2P (Note 4)	QFN-16	4.0	$^{\circ}$ C/W
$T_{sol}$	Wave Solder Pb-Free			265	$^{\circ}$ C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NB6L14S

**Table 5. DC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{CC}$	Power Supply Current (Note 9)		65	100	mA

**DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED** (Figures 17, 18, 22, and 24)

$V_{th}$	Input Threshold Reference Voltage Range (Note 8)	GND +100		$V_{CC} - 100$	mV
$V_{IH}$	Single-ended Input HIGH Voltage	$V_{th} + 100$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage	GND		$V_{th} - 100$	mV
$V_{REFAC}$	Reference Output Voltage (Note 11)	$V_{CC} - 1.600$	$V_{CC} - 1.425$	$V_{CC} - 1.300$	V

**DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 10, 12, NO TAG, NO TAG, 23, and 25)

$V_{IHD}$	Differential Input HIGH Voltage	100		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	GND		$V_{IHD} - 100$	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration)	GND + 50		$V_{CC} - 50$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	100		$V_{CC}$	mV
$R_{TIN}$	Internal Input Termination Resistor	40	50	60	$\Omega$

**LVDS OUTPUTS** (Note 5)

$V_{OD}$	Differential Output Voltage	250		450	mV
$\Delta V_{OD}$	Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 10)	0	1	25	mV
$V_{OS}$	Offset Voltage (Figure 21)	1125		1375	mV
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 10)	0	1	25	mV
$V_{OH}$	Output HIGH Voltage (Note 6)		1425	1600	mV
$V_{OL}$	Output LOW Voltage (Note 7)	900	1075		mV

**LVTTTL/LVCMOS INPUT, EN**

$V_{IH}$	Input HIGH Voltage	2.0		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage	GND		0.8	V
$I_{IH}$	Input HIGH Current	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150		150	$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. LVDS outputs require 100  $\Omega$  receiver termination resistor between differential pair. See Figure 20.

6.  $V_{OHmax} = V_{OSmax} + \frac{1}{2} V_{ODmax}$ .

7.  $V_{OLmax} = V_{OSmin} - \frac{1}{2} V_{ODmax}$ .

8.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.

9. Input termination pins open at the DC level within  $V_{CMR}$  and output pins loaded with  $R_L = 100\ \Omega$  across differential.

10. Parameter guaranteed by design verification not tested in production.

11.  $V_{REFAC}$  used to rebias capacitor-coupled inputs only (see Figures 17 and 18).

# NB6L14S

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ; (Note 12)

Symbol	Characteristic	-40°C to +85°C			Unit
		Min	Typ	Max	
$f_{inMax}$	Maximum Input Clock Frequency	2.0			GHz
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (Figure 4)	$f_{in} \leq 1.0\text{ GHz}$ 220 $f_{in} = 1.5\text{ GHz}$ 200 $f_{in} = 2.0\text{ GHz}$ 170	350 300 270		mV
$f_{DATA}$	Maximum Operating Data Rate	2.5			Gb/s
$t_{PLH}$ , $t_{PHL}$	Differential Input to Differential Output, IN to Q Propagation Delay @ 100 MHz	300	450	600	ps
$t_s$ $t_h$	Setup Time Hold Time	300 500	20 20		
$t_{SKEW}$	Within Device Skew (Note 17) Device-to-Device Skew (Note 16)		5 30	20 200	ps
$t_{JITTER}$	RMS Random Clock Jitter (Note 14) Deterministic Jitter (Note 15)		$f_{in} = 2.0\text{ GHz}$ 0.5 5.0 $f_{DATA} \leq 2.488\text{ Gb/s}$	0.8 20	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 13)	100		$V_{CC} - GND$	mV
$t_r$ $t_f$	Output Rise/Fall Times @ 250 MHz (20% – 80%)	70	150	225	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing  $V_{INPPmin}$  with 50% duty cycle clock source and  $V_{CC} - 1400\text{ mV}$  offset. All loading with an external  $R_L = 100\ \Omega$ . Input edge rates 150 ps (20%–80%). See Figure 20.

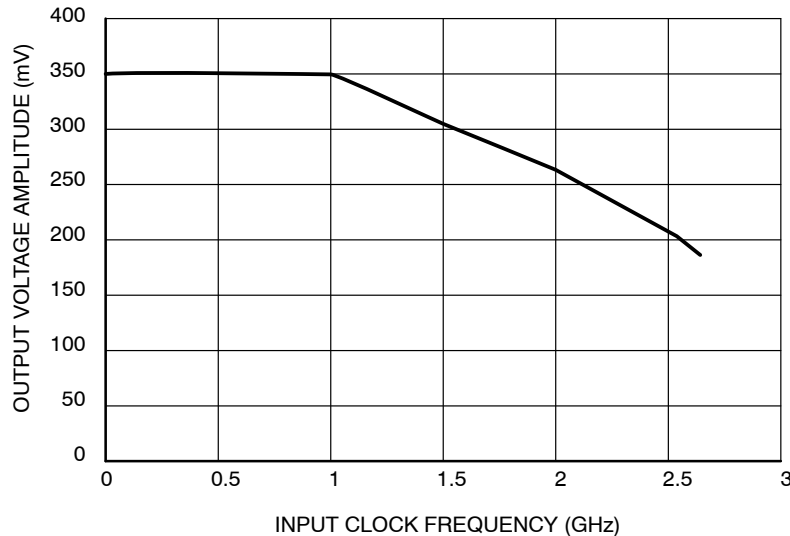
13. Input voltage swing is a single-ended measurement operating in differential mode.

14. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.

15. Deterministic jitter with input NRZ data at PRBS 2<sup>23</sup>-1 and K28.5.

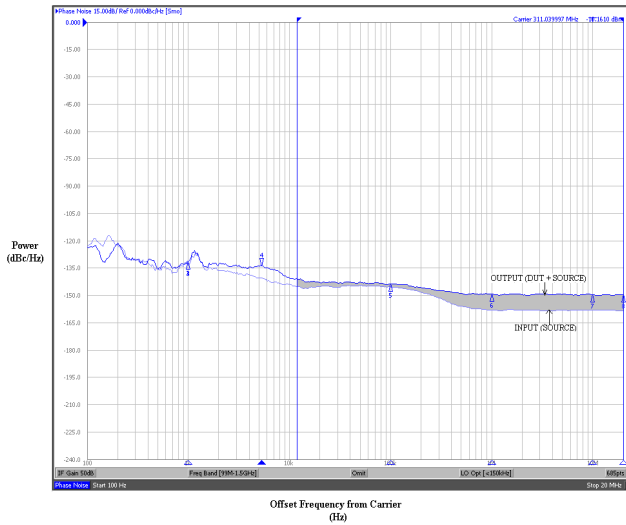
16. Skew is measured between outputs under identical transition @ 250 MHz.

17. The worst case condition between  $Q0/\bar{Q}0$  and  $Q1/\bar{Q}1$  from either  $D0/\bar{D}0$  or  $D1/\bar{D}1$ , when both outputs have the same transition.

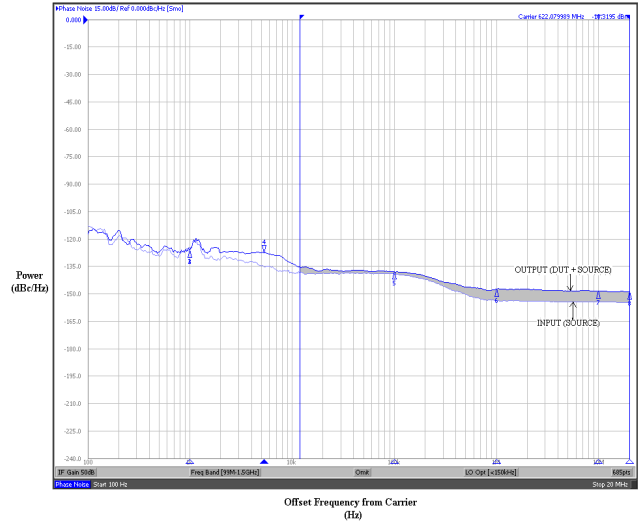


**Figure 4. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Input Clock Frequency ( $f_{in}$ ) and Temperature (@  $V_{CC} = 2.5\text{ V}$ )**

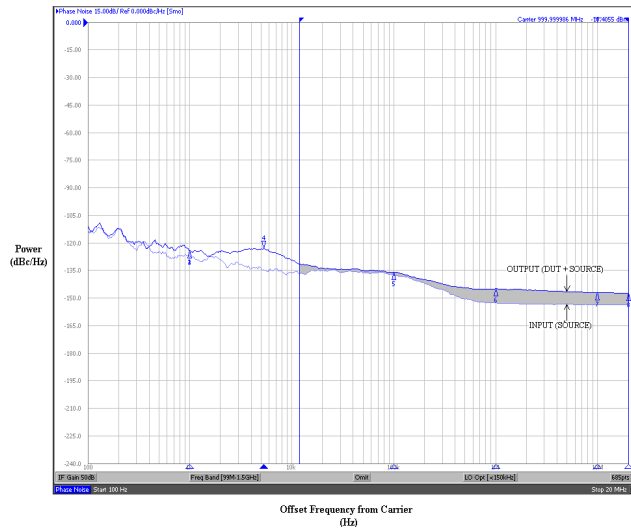
# NB6L14S



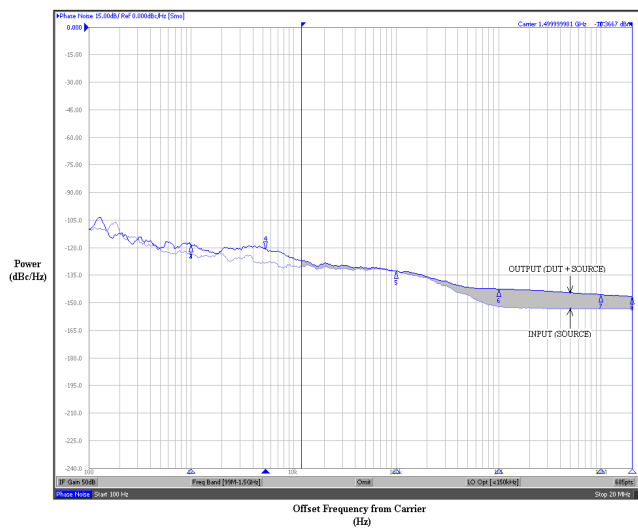
**Figure 5. Typical Phase Noise Plot at  $f_{\text{carrier}} = 311.04 \text{ MHz}$**



**Figure 6. Typical Phase Noise Plot at  $f_{\text{carrier}} = 622.08 \text{ MHz}$**



**Figure 7. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1 \text{ GHz}$**

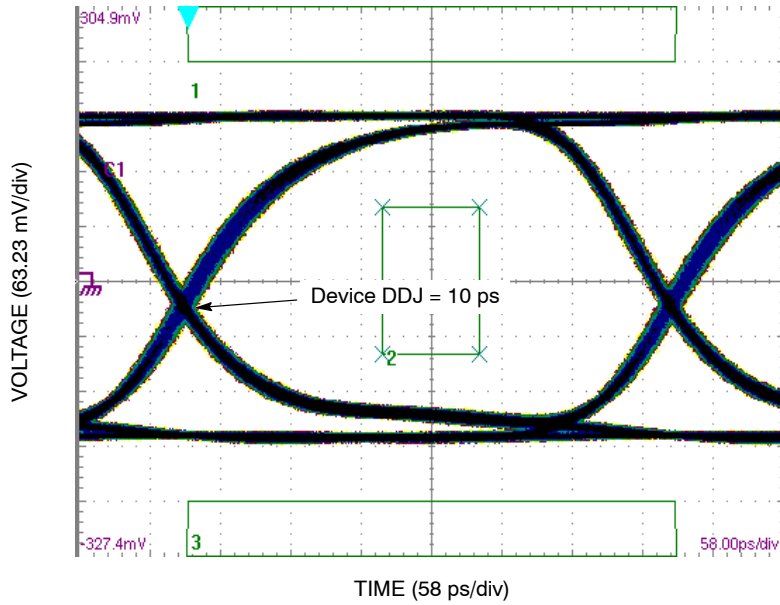


**Figure 8. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1.5 \text{ GHz}$**

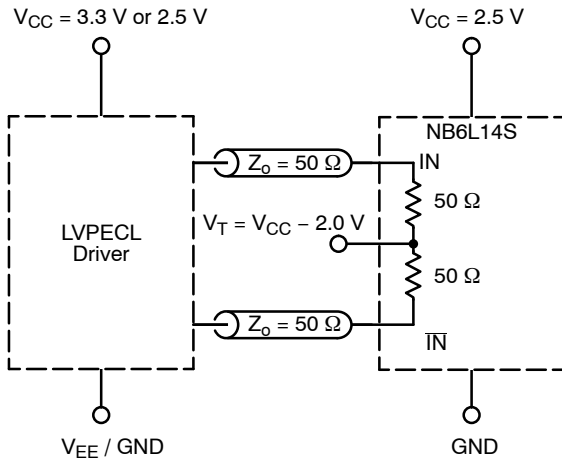
The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L14S device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 1.5 GHz respectively at an operating voltage of 2.5 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 65 fs, 29 fs, 24 fs and 20 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

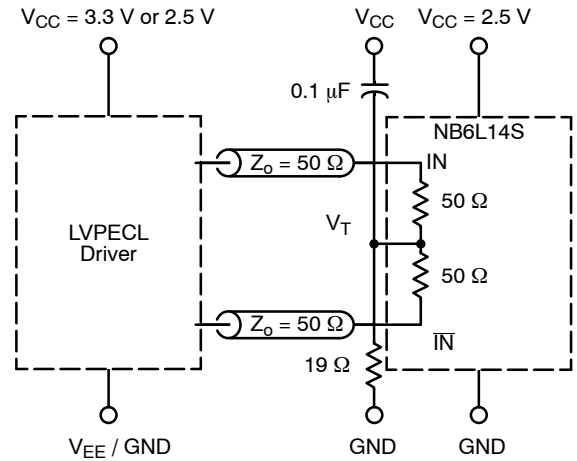
# NB6L14S



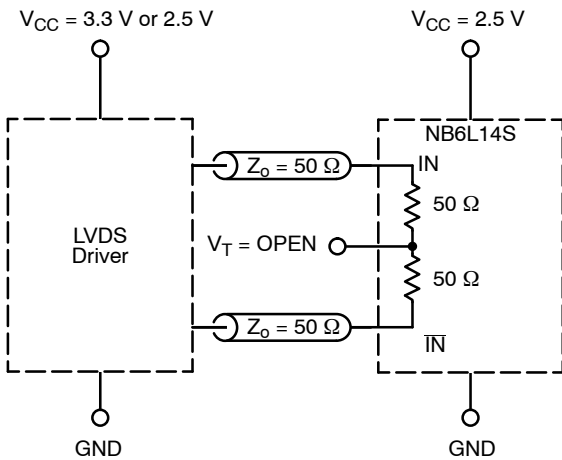
**Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  and OC48 mask ( $V_{INPP} = 100$  mV; Input Signal DDJ = 14 ps)**



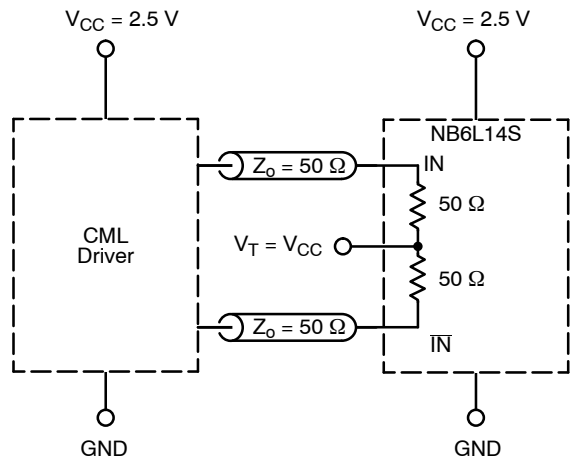
**Figure 10. LVPECL Interface**



**Figure 11. LVPECL Y-Termination Interface**



**Figure 12. LVDS Interface**



**Figure 13. CML Interface**



# NB6L14S

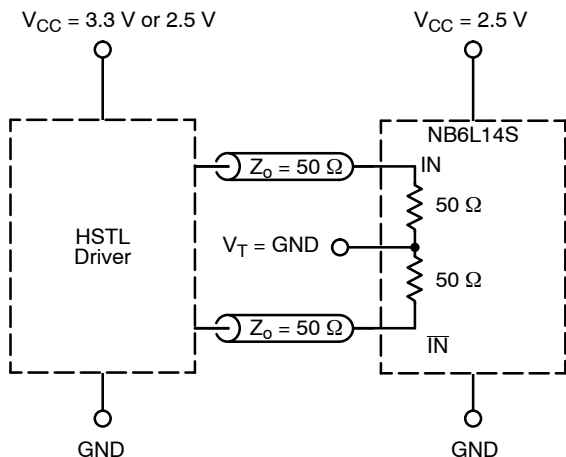


Figure 14. HSTL Interface

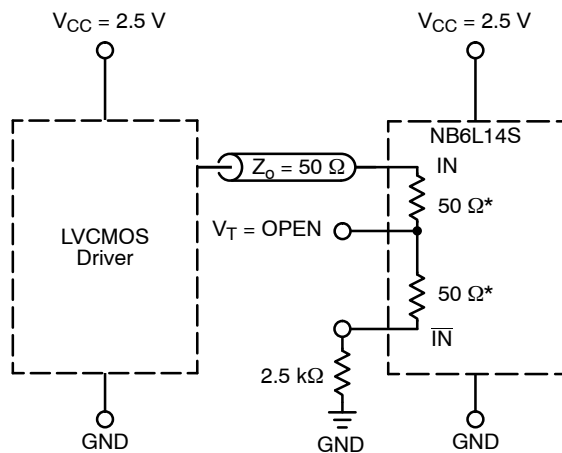


Figure 15. LVCMOS Interface

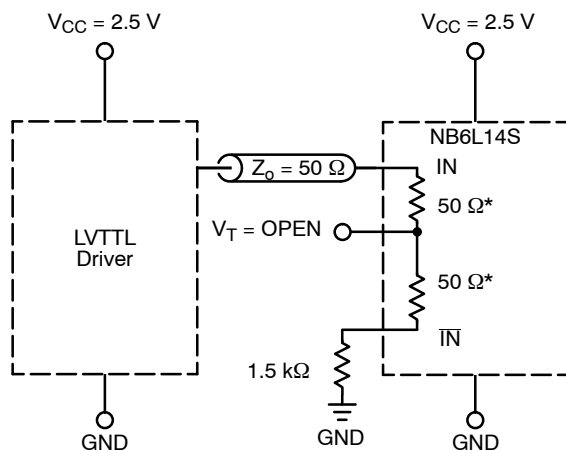


Figure 16. LVTTTL Interface

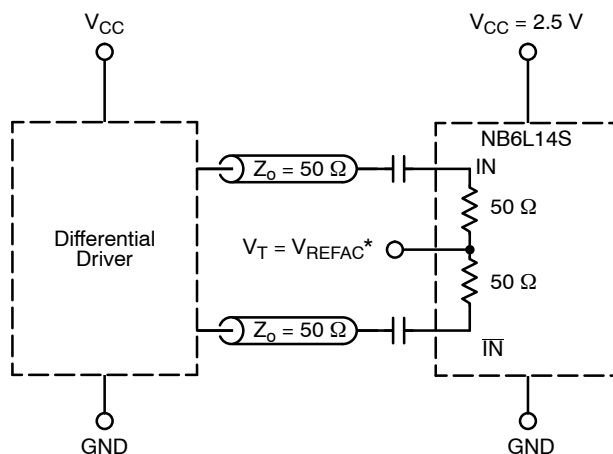


Figure 17. Capacitor-Coupled Differential Interface ( $V_T$  Connected to  $V_{REF\_AC}$ )

\* $V_{REF\_AC}$  bypassed to ground with a 0.1  $\mu$ F capacitor.

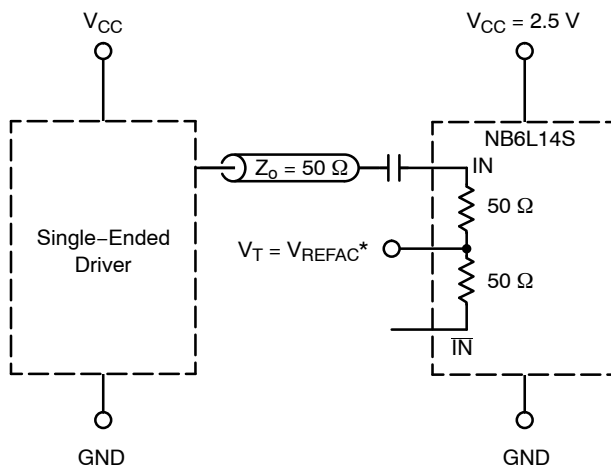


Figure 18. Capacitor-Coupled Single-Ended Interface ( $V_T$  Connected to  $V_{REF\_AC}$ )

\* $V_{REF\_AC}$  bypassed to ground with a 0.1  $\mu$ F capacitor.

# NB6L14S

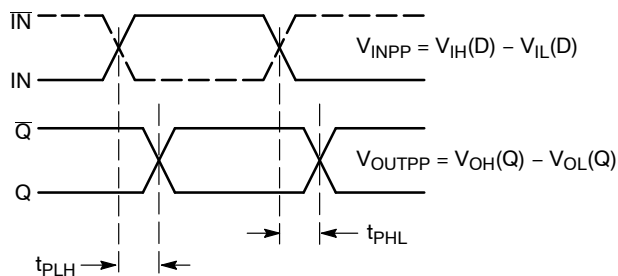


Figure 19. AC Reference Measurement

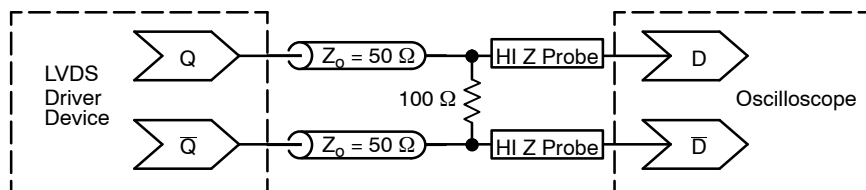


Figure 20. Typical LVDS Termination for Output Driver and Device Evaluation

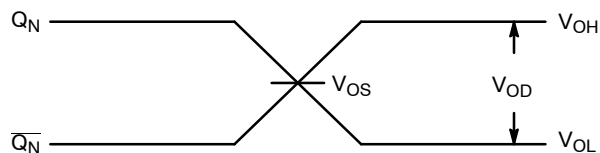


Figure 21. LVDS Output

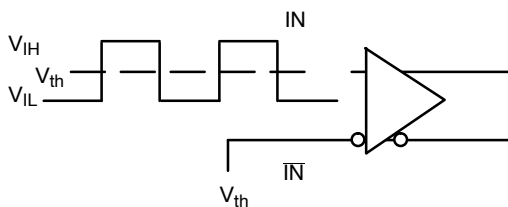


Figure 22. Differential Input Driven Single-Ended

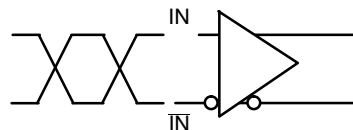


Figure 23. Differential Inputs Driven Differentially

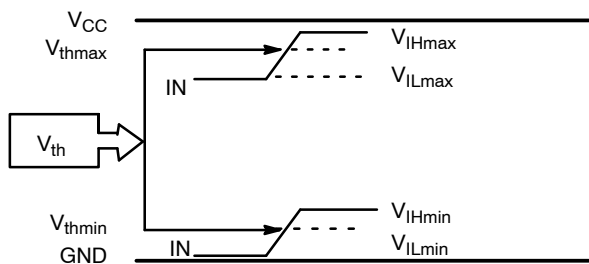


Figure 24.  $V_{th}$  Diagram

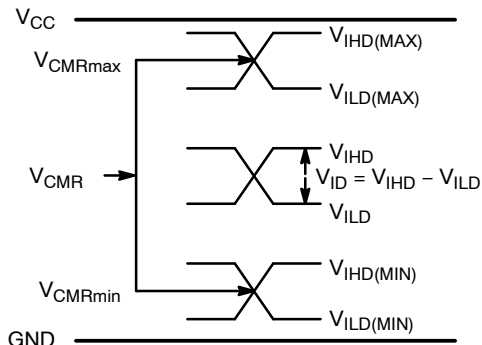


Figure 25.  $V_{CMR}$  Diagram

# NB6L14S

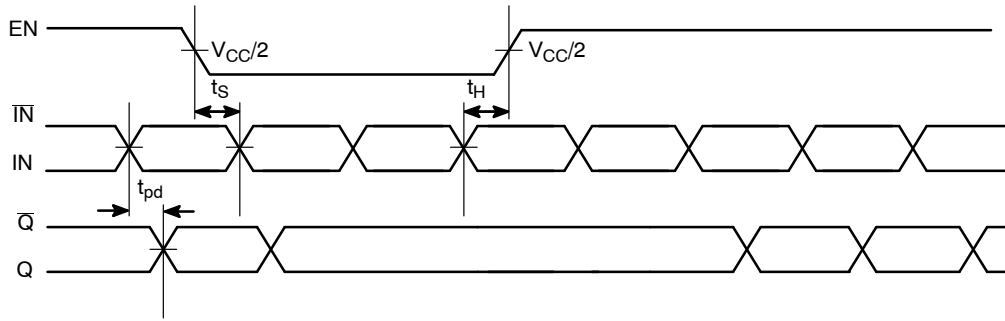


Figure 26. EN Timing Diagram

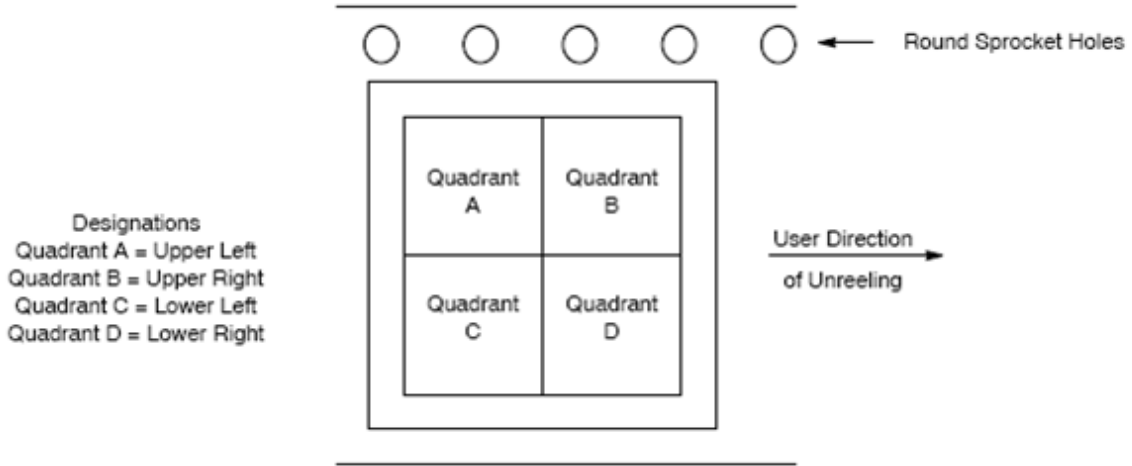


Figure 27. Tape and Reel Pin 1 Quadrant Orientation

## ORDERING INFORMATION

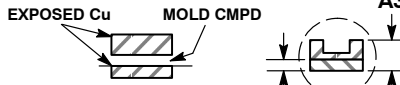
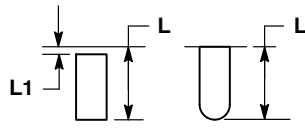
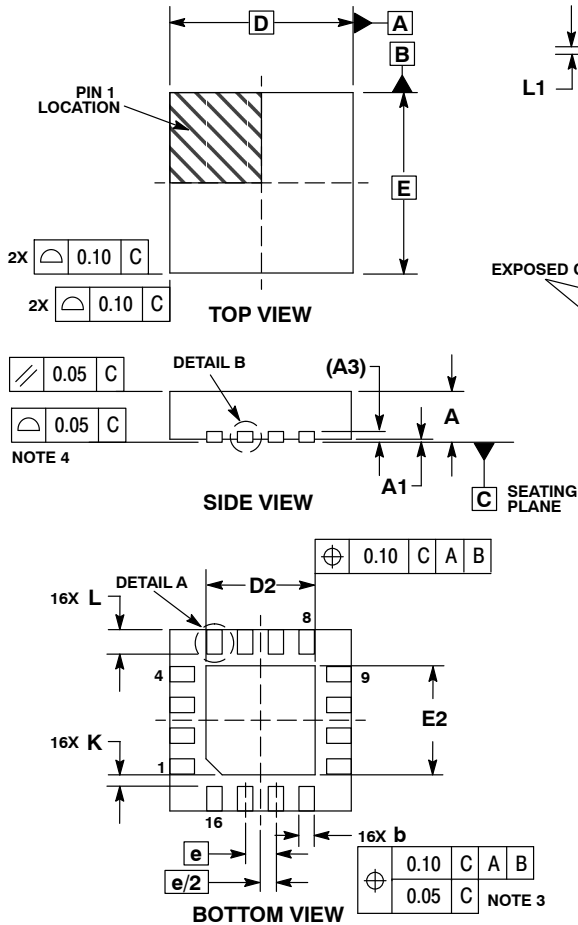
Device	Package	Shipping†
NB6L14SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB6L14SMNTXG	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 27)
NB6L14SMNTWG	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel (Pin 1 Orientation in Quadrant A, Figure 27)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NB6L14S

## PACKAGE DIMENSIONS

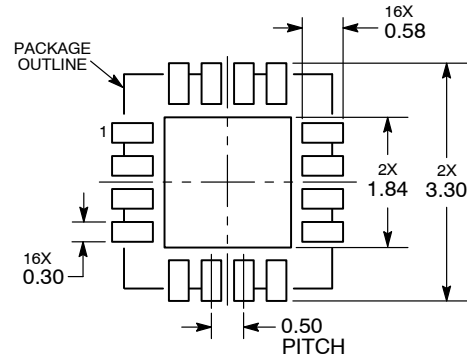
QFN16 3x3, 0.5P  
CASE 485G-01  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.18	TYP
L	0.30	0.50
L1	0.00	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

AnyLevel and ECLinPS MAX are trademarks of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative