

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

### General Description

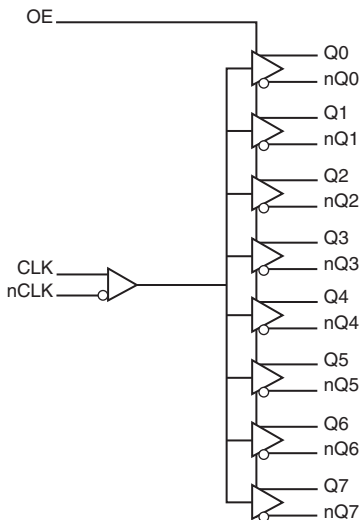
The 85408 is a low skew, high performance 1-to-8 Differential-to-LVDS Clock Distribution Chip. The 85408 CLK, nCLK pair can accept most differential input levels and translates them to 3.3V LVDS output levels. Utilizing Low Voltage Differential Signaling (LVDS), the 85408 provides a low power, low noise, low skew, point-to-point solution for distributing LVDS clock signals.

Guaranteed output and part-to-part skew specifications make the 85408 ideal for those applications demanding well defined performance and repeatability.

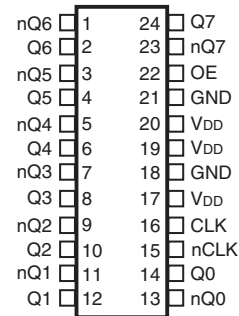
### Features

- Eight differential LVDS output pairs
- CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSSL, SSTL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, HCSSL) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 550ps (maximum)
- Propagation delay: 2.4ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment



**85408**  
**24-Lead TSSOP**  
**4.4mm x 7.8mm x 0.925mm package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	nQ6, Q6	Output		Differential output pair. LVDS interface levels.
3, 4	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
5, 6	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 8	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
9, 10	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
11, 12	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
13, 14	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
15	nCLK	Input	Pullup	Inverting differential clock input.
16	CLK	Input	Pulldown	Non-inverting differential clock input.
17, 19, 20	V <sub>DD</sub>	Power		Positive supply pins.
18, 21	GND	Power		Power supply ground.
22	OE	Input	Pullup	Output enable. Controls the enabling and disabling of outputs Qx, nQx. When HIGH, the outputs are enabled. When LOW, the outputs are in High-Impedance. LVCMOS / LVTTTL interface levels.
23, 24	nQ7, Q7	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance (per output)			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

**Table 3A. Output Enable Function Table**

Inputs	Outputs
OE	Q[0:7], nQ[0:7]
0	High-Impedance
1	Active (default)

**Table 3B. Clock Input Function Table**

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q[0:7]	nQ[0:7]		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, *Wiring the Differential Input to Accept Single-Ended Levels*.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	70°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				90	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK	$V_{DD} = V_{IN} = 3.465V$		5	
$I_{IL}$	Input Low Current	CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nCLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

**Table 4D. LVDS DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	400	600	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change	$R_L = 100\Omega$			50	mV
$V_{OS}$	Offset Voltage	$R_L = 100\Omega$	1.125	1.4	1.6	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change	$R_L = 100\Omega$			50	mV
$I_{OZ}$	High Impedance Leakage		-10		+10	$\mu A$
$I_{OFF}$	Power Off Leakage		-1		+1	$\mu A$
$I_{OSD}$	Differential Output Short Circuit Current				-5.5	mA
$I_{OS}/I_{OSB}$	Output Short Circuit Current				-12	mA

**Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1		1.6		2.4	ns
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: (12kHz – 20MHz)		167		fs
$tsk(o)$	Output Skew; NOTE 2, 4				50	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4				550	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	50		600	ps
odc	Output Duty Cycle		45		55	%
$t_{PZL}, t_{PZH}$	Output Enable Time; NOTE 5				5	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time; NOTE 5				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at  $f \leq 622\text{MHz}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crossing point of the input to the differential output crossing point.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

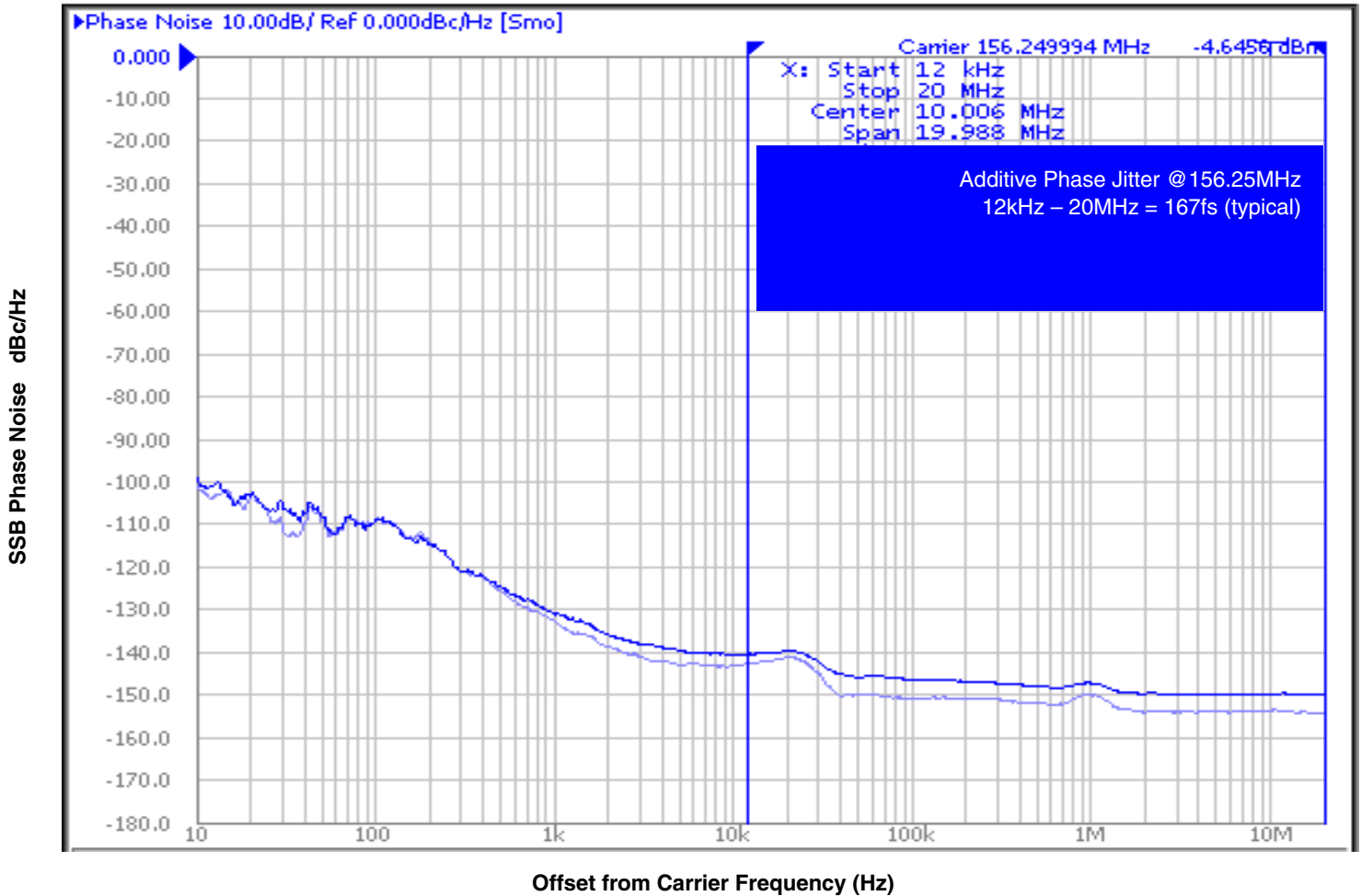
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

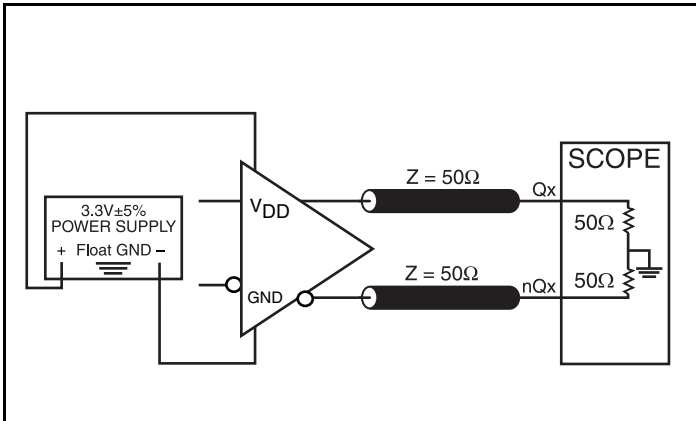
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



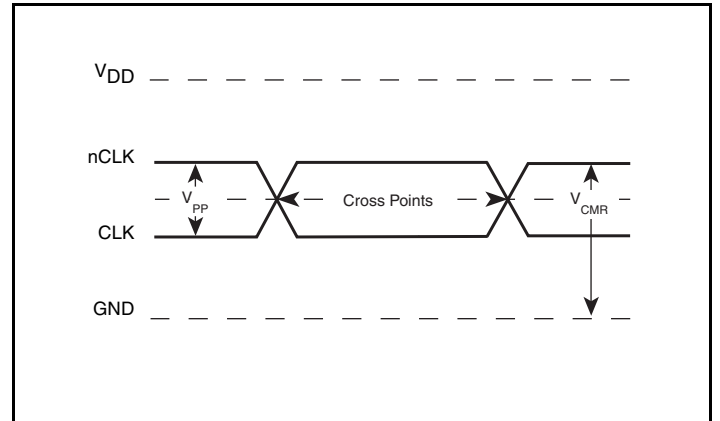
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This

is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

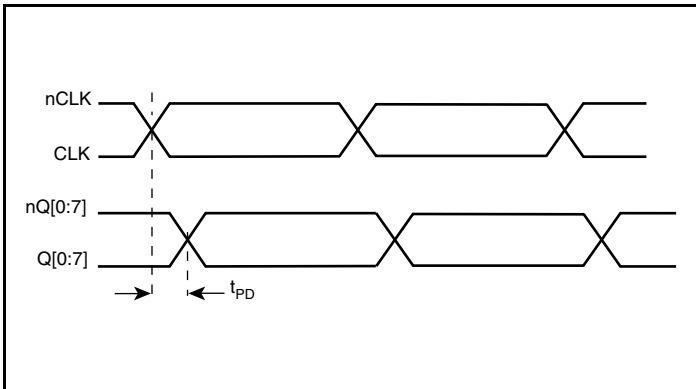
## Parameter Measurement Information



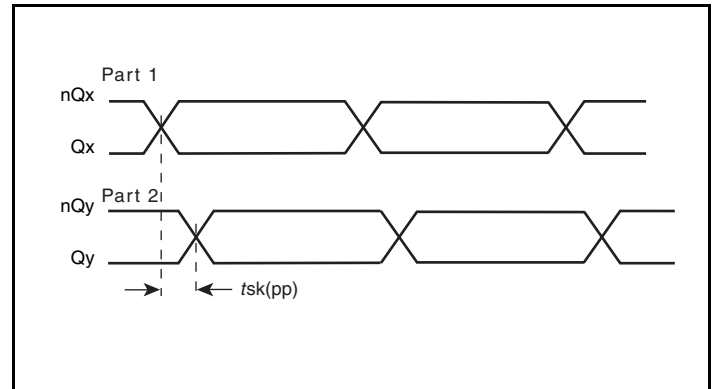
3.3V LVDS Output Load AC Test Circuit



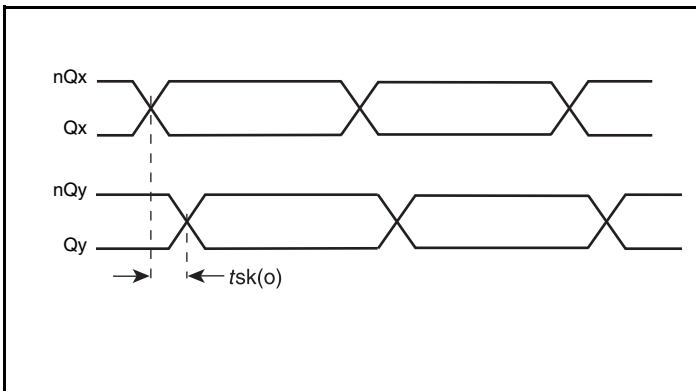
Differential Input Level



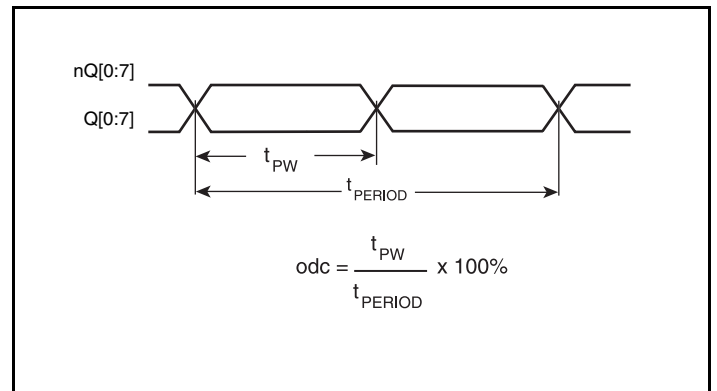
Propagation Delay



Part-to-Part Skew



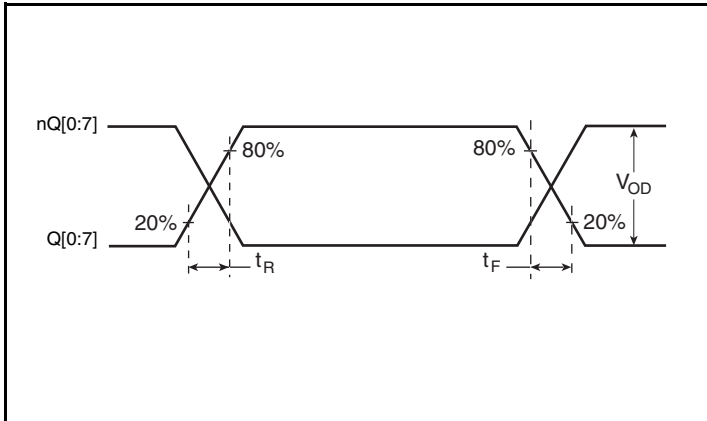
Output Skew



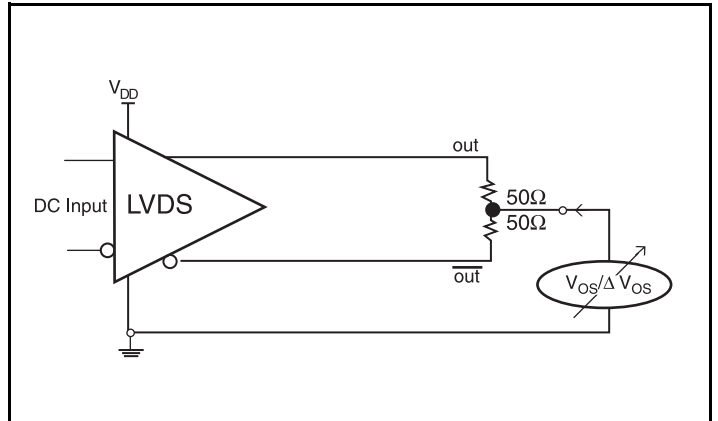
Output Duty Cycle/Pulse Width/Period



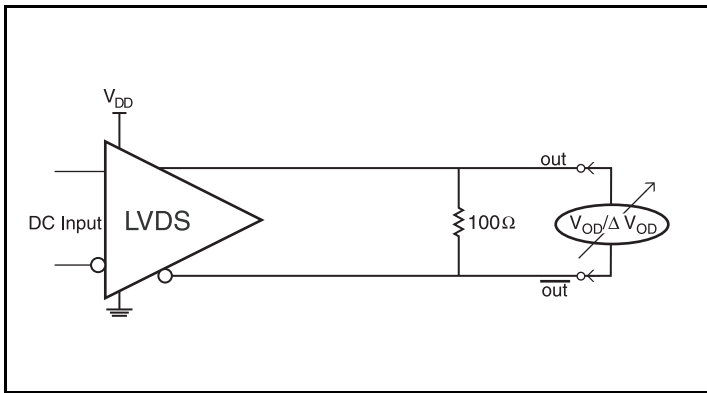
Parameter Measurement Information, continued



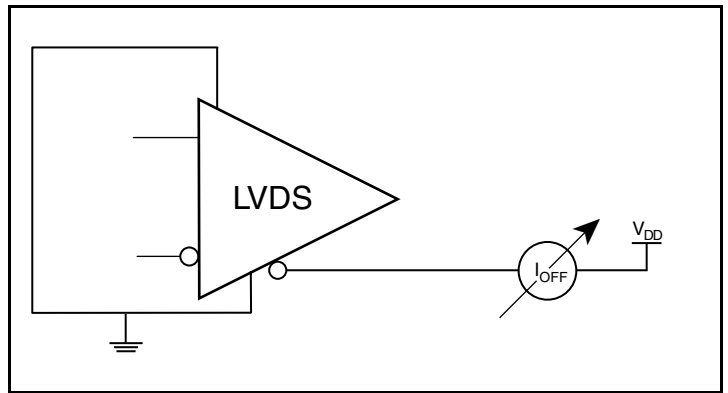
Output Rise/Fall Time



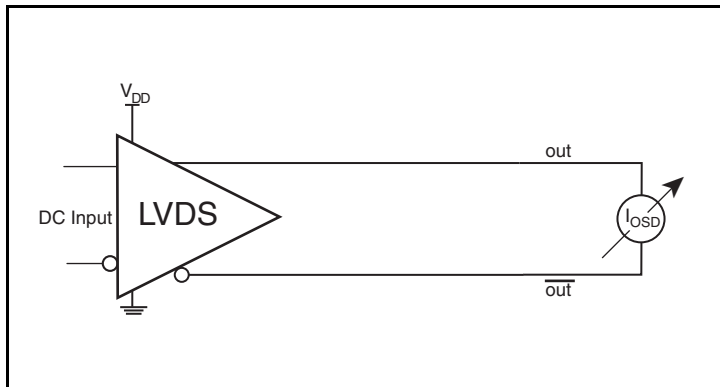
Offset Voltage Setup



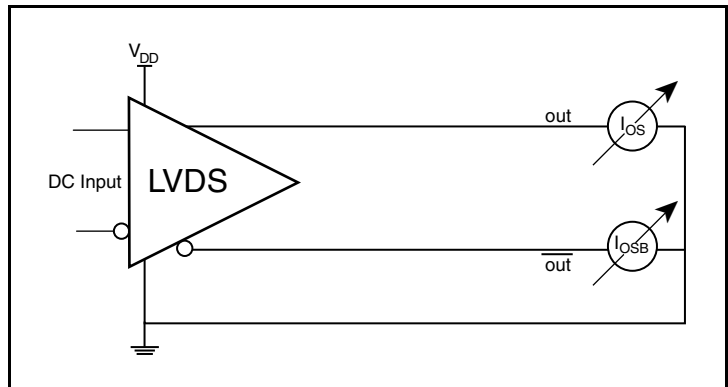
Differential Output Voltage Setup



Power Off Leakage Setup



Differential Output Short Circuit Setup



Output Short Circuit Current Setup

## Application Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

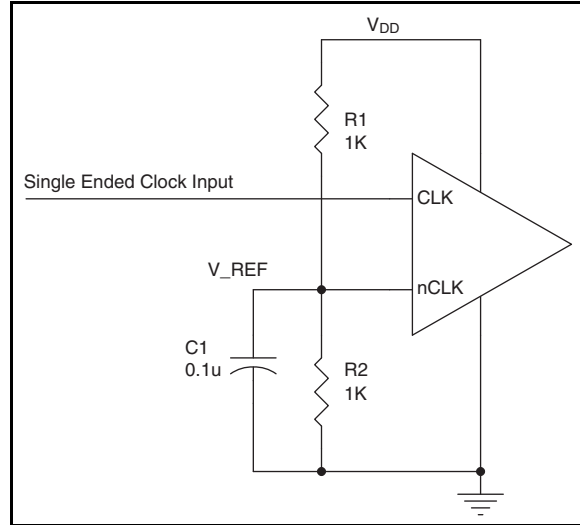


Figure 1. Single-Ended Signal Driving Differential Input

### Recommendations for Unused Output Pins

#### Outputs:

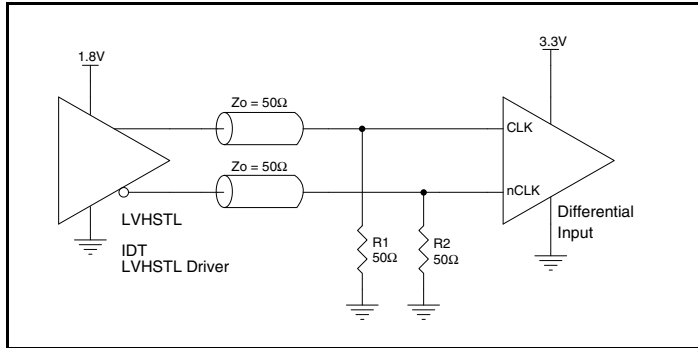
##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, there should be no trace attached.

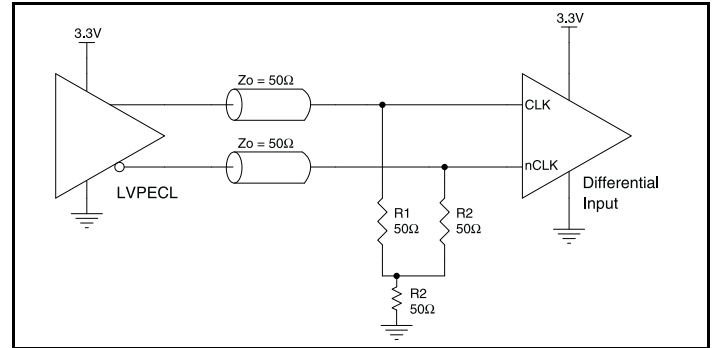
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

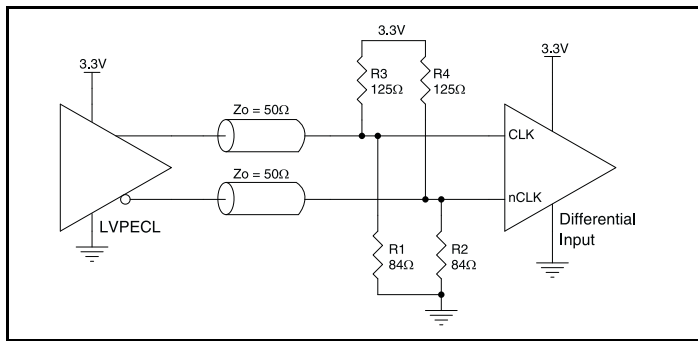
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



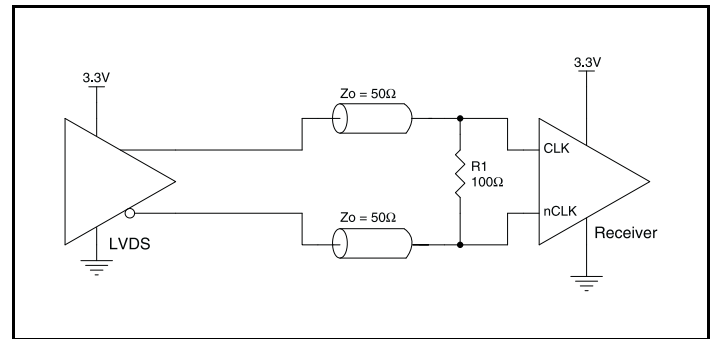
**2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



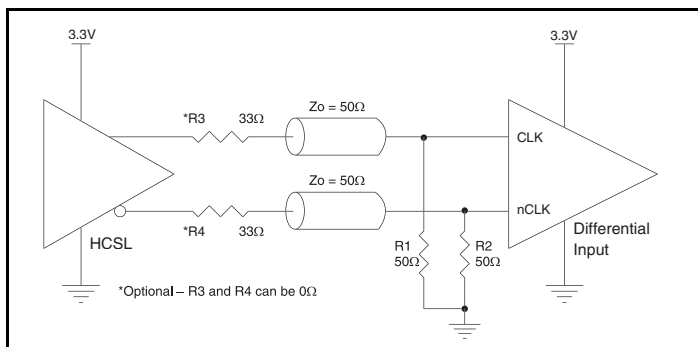
**Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



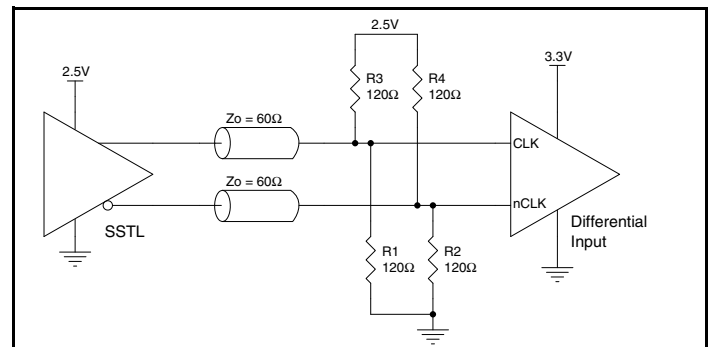
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**

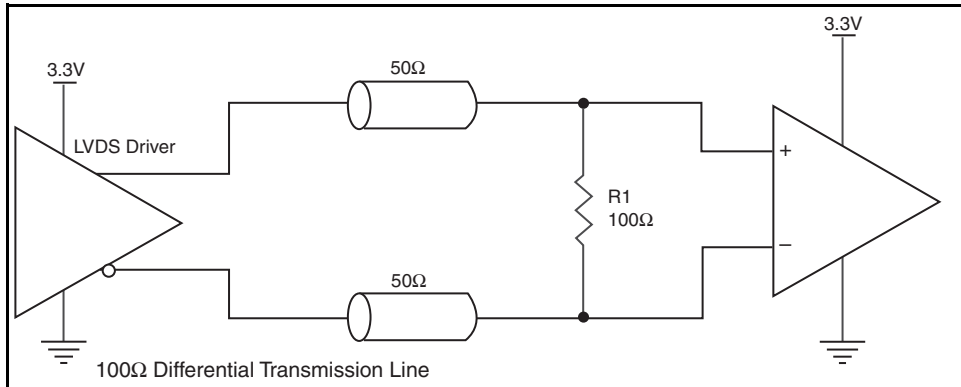


**Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

### 3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3*. In a  $100\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of  $100\Omega$  across near the receiver input. For a multiple

LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.



**Figure 3. Typical LVDS Driver Termination**

## Power Considerations

This section provides information on power dissipation and junction temperature for the 85408. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 85408 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 90mA = 311.85mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.312\text{W} * 70^\circ\text{C}/\text{W} = 91.8^\circ\text{C}.$$

This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65.0°C/W	62°C/W

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead TSSOP

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65.0°C/W	62°C/W

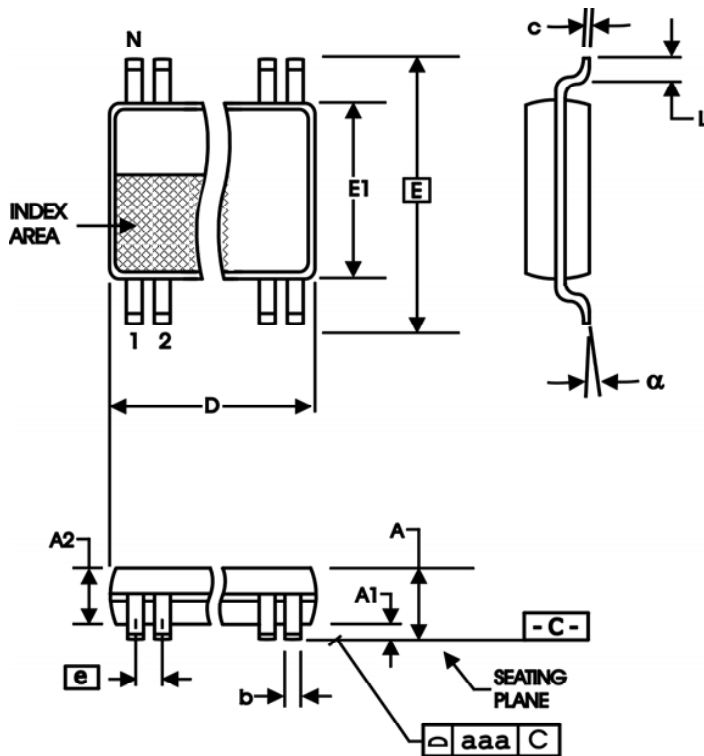
## Transistor Count

The transistor count for 85408 is: 1821

Pin compatible with SN65LVDS104

## Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP



All Dimensions in Millimeters		
Symbol	Minimum	Maximum
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.05	0.15

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85408BGLF	ICS85408BGLF	"Lead-Free" 24 Lead TSSOP	Tube	0°C to 70°C
85408BGLFT	ICS85408BGLF	"Lead-Free" 24 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T6 T8	9 11	Reliability Table - revised air flow from Linear Feet per Minute to Meters per Second. Ordering Information Table - corrected typo in Part/Order Number from ICS8540BG to ICS85408BG.	5/6/04
A		1	Pin Assignment - corrected package information from 300-MIL to 173-MIL.	8/25/04
A	T8	1 11	Features Section - added <i>Lead-Free</i> bullet. Corrected Block Diagram. Ordering Information Table - added <i>Lead-Free</i> information.	4/25/05
A	T8	11	Ordering Information Table - added <i>Lead-Free</i> part number.	12/6/07
B	T5	5 6 12	AC Characteristics Table - added Additive Phase Jitter spec. Added Additive Phase Jitter Plot. Added <i>Power Considerations</i> section. Converted datasheet format.	6/24/09
C	T9	1 14	Features section - removed leaded device references. Ordering information - removed leaded devices. PDN CQ-13-02 expired. Updated datasheet format.	1/5/15





**Corporate Headquarters**  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA

**Sales**  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
www.IDT.com

**Tech Support**  
email: [clocks@idt.com](mailto:clocks@idt.com)

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2015 Integrated Device Technology, Inc.. All rights reserved.