阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

General Description

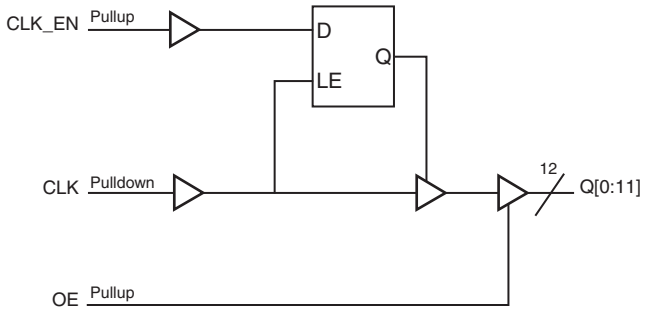
The 8312 is a low skew, 1-to-12 LVCMOS/ LVTTL Fanout Buffer and a member of the family of High Performance Clock Solutions from IDT. The 8312 single-ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The 8312 is characterized at full 3.3V, 2.5V, and 1.8V, mixed 3.3V/2.5V, 3.3V/1.8V and 2.5V/1.8V output operating supply modes. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the 8312 ideal for high performance, single ended applications that also require a limited output voltage.

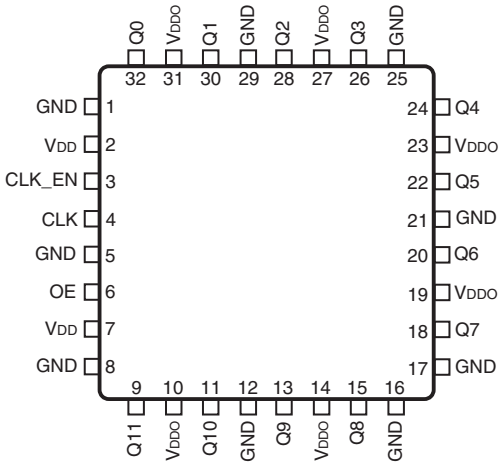
Features

- Twelve LVCMOS/LVTTL outputs
- CLK input supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 150ps (maximum)
- Supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
  1.8V/1.8V
- 0°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8312

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 5, 8, 12, 16, 17, 21, 25, 29	GND	Power		Power supply ground.
2, 7	V_{DD}	Power		Positive supply pins.
3	CLK_EN	Input	Pullup	Synchronous control for enabling and disabling clock outputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
6	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q[0:11]. LVCMOS / LVTTL interface levels.
9, 11, 13, 15, 18, 20, 22, 24, 26, 28, 30, 32	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
10, 14, 19, 23, 27, 31	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V			19	pF
		V_{DDO} = 2.625V			18	pF
		V_{DDO} = 2V			16	pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		7		Ω
		V_{DDO} = 2.5V ± 5%		7		Ω
		V_{DDO} = 1.8V ± 0.2V		10		Ω

Function Tables

Table 3A. Output Enable and Clock Enable Function Table

Inputs		Outputs
OE	**CLK_EN**	**Q [0:11]**
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

Table 3B. Output Enable and Clock Enable Function Table

Inputs			Outputs
OE	**CLK_EN**	**CLK**	**Q [0:11]**
1	1	0	LOW
1	1	1	HIGH

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4D. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4E. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4F. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4G. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
			V_{DD} = 2.0V	0.65*V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		1.3	V
			V_{DD} = 2.625V	-0.3		0.7	V
			V_{DD} = 2.0V	-0.3		0.35*V_{DD}	V
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V or 2.625V or 2.0V			150	µA
		OE, CLK_EN	V_{DD} = V_{IN} = 3.465V or 2.625V or 2.0V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V or 2.625V or 2.0V, V_{IN} = 0V	-5			µA
		OE, CLK_EN	V_{DD} = 3.465V or 2.625V or 2.0V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%	2.6			V
			V_{DDO} = 2.5V ± 5%;	1.8			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -1mA	2			V
			V_{DDO} = 1.8V ± 0.2V	V_{DD} – 0.3			V
			V_{DDO} = 1.8V ± 0.2V; I_{OH} = -100µA	V_{DD} – 0.2			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%			0.5	V
			V_{DDO} = 2.5V ± 5%;			0.45	V
			V_{DDO} = 2.5V ± 5%; I_{OL} = 1mA			0.4	V
			V_{DDO} = 1.8V ± 0.2V			0.35	V
			V_{DDO} = 1.8V ± 0.2V; I_{OL} = 100µA			0.2	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq 250MHz$	1.2	1.9	2.5	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.037		ps
*t*sk(o)	Output Skew; NOTE 2, 5				125	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f \leq 200MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq 250MHz$	1.4	2.3	3.2	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.022		ps
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.1	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f \leq 150MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5C. AC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0°C$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq 200MHz$	1.6	3.3	4.8	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.172		ps
*t*sk(o)	Output Skew; NOTE 2, 5				140	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				2.3	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		800	ps
odc	Output Duty Cycle	$f \leq 100MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5D. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq 250MHz$	1.4	2.1	2.7	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.045		ps
*t*sk(o)	Output Skew; NOTE 2, 5				135	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				900	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f \leq 150MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5E. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq$ 200MHz	1.4	2.4	3.4	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.136		ps
*t*sk(o)	Output Skew; NOTE 2, 5				145	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.3	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f \leq$ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

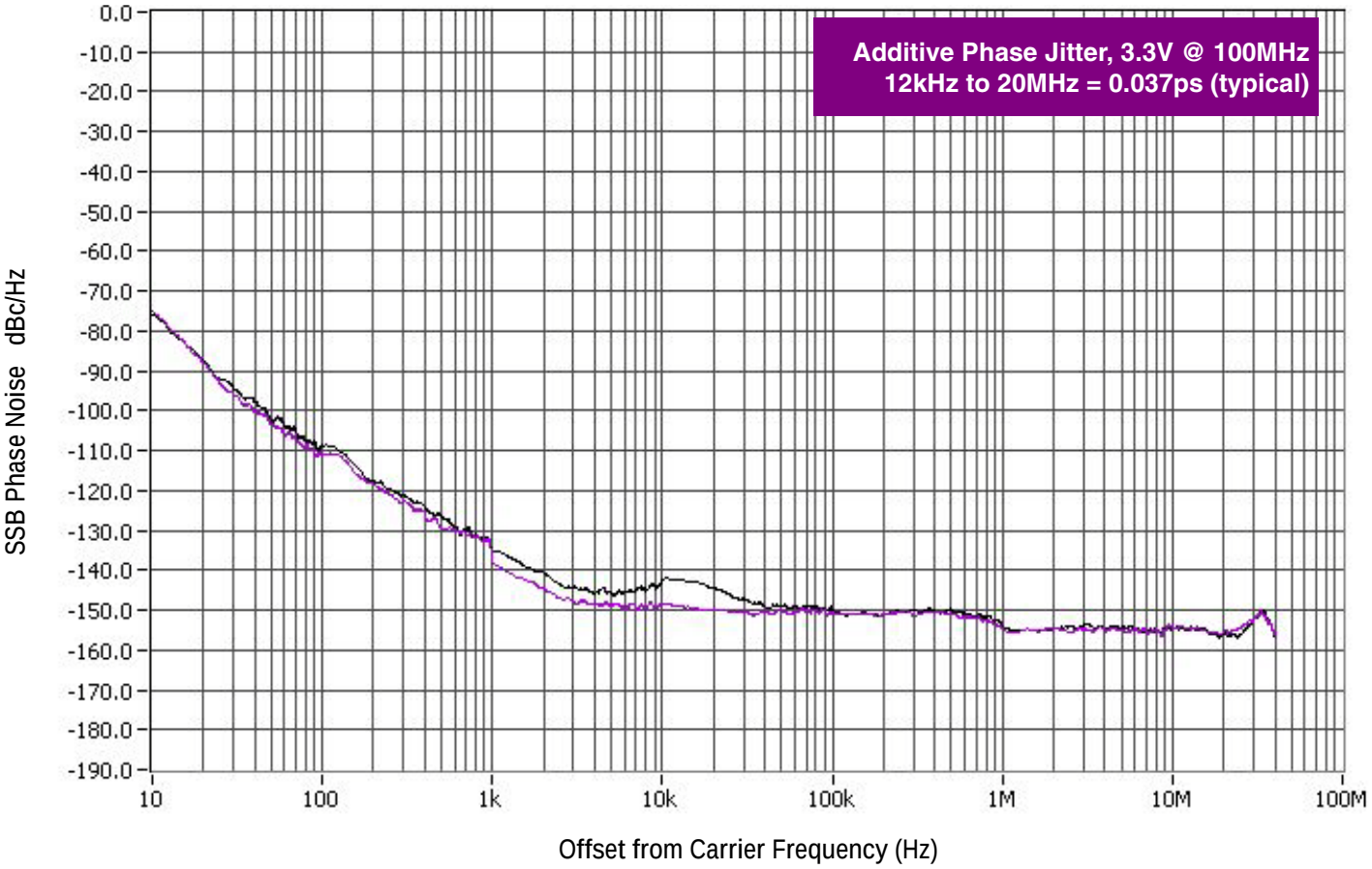
Table 5F. AC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = 0°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq$ 200MHz	1.5	2.6	3.7	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.114		ps
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.5	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f \leq$ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

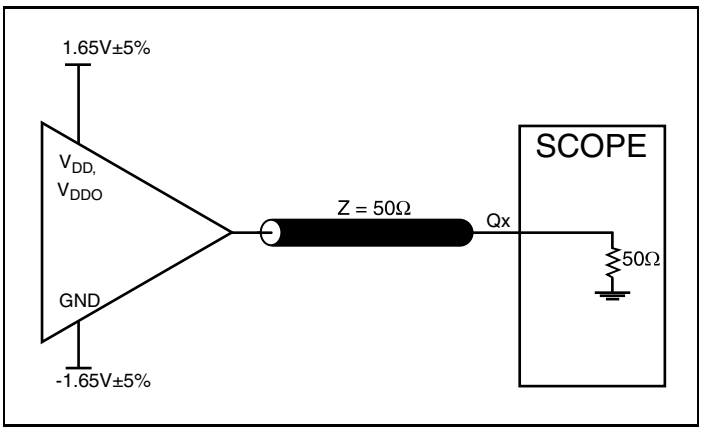
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

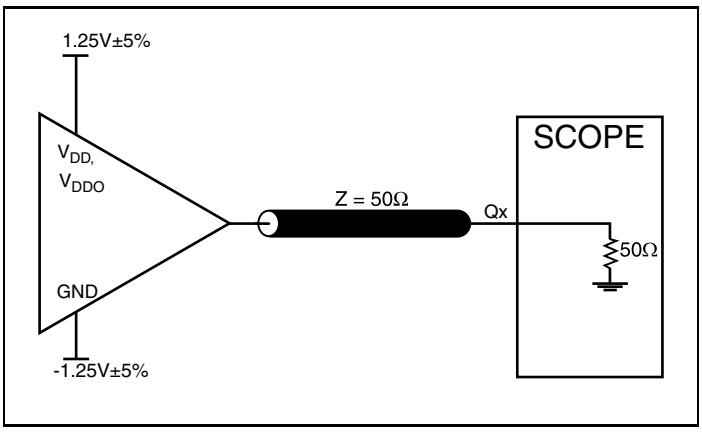


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

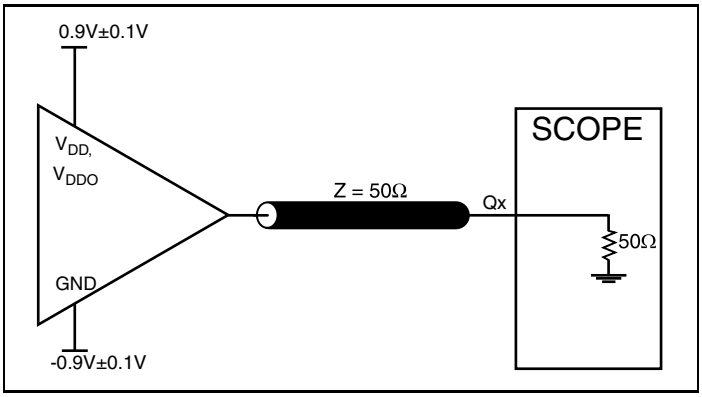
Parameter Measurement Information



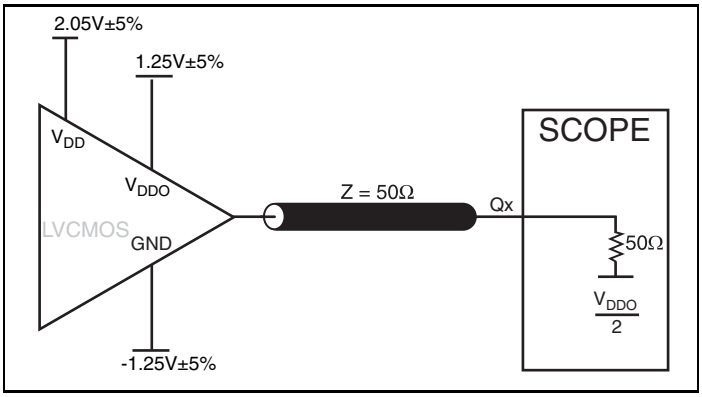
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



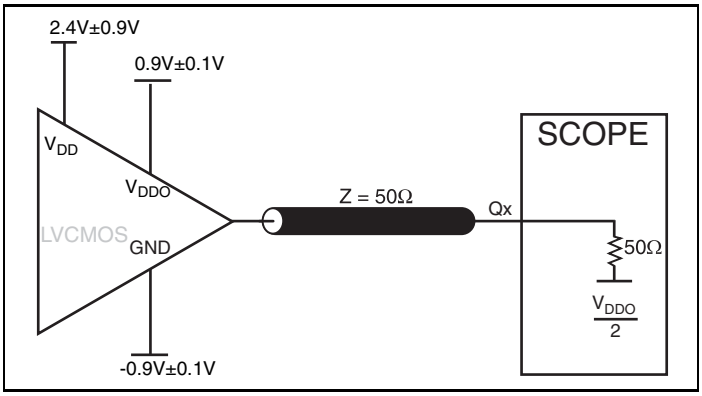
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



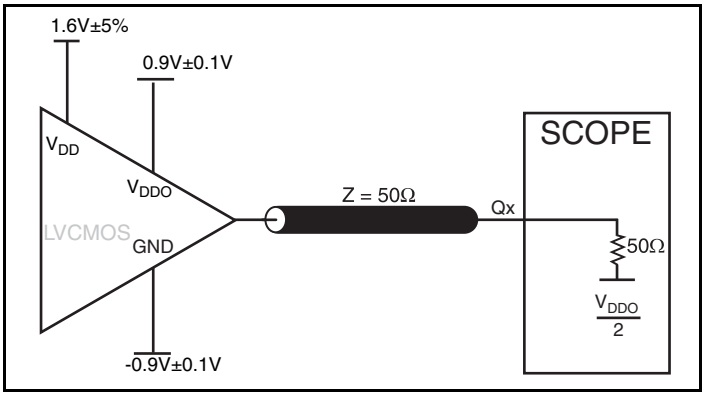
1.8V Core/1.8V LVCMOS Output Load AC Test Circuit



3.3V Core/2.5V LVCMOS Output Load AC Test Circuit

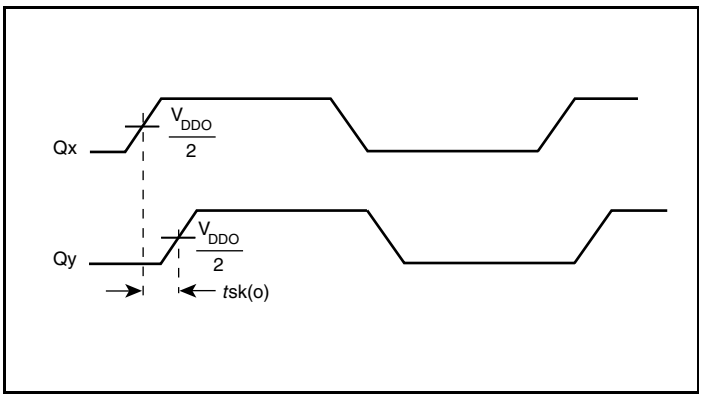


3.3V Core/1.8V LVCMOS Output Load AC Test Circuit

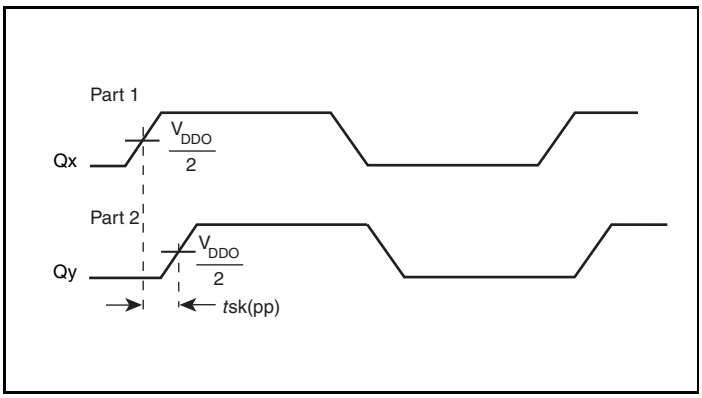


2.5V Core/1.8V LVCMOS Output Load AC Test Circuit

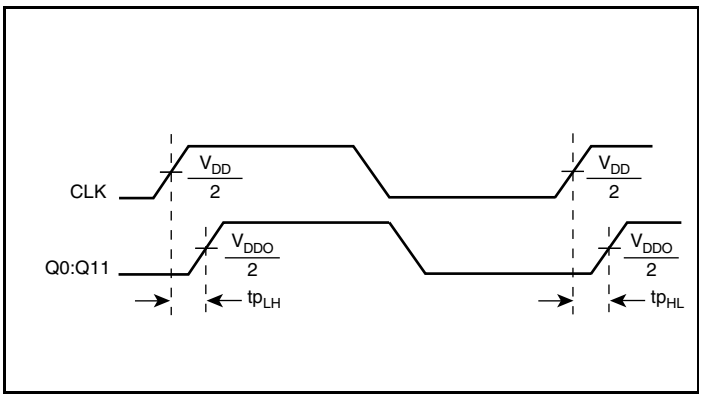
Parameter Measurement Information, continued



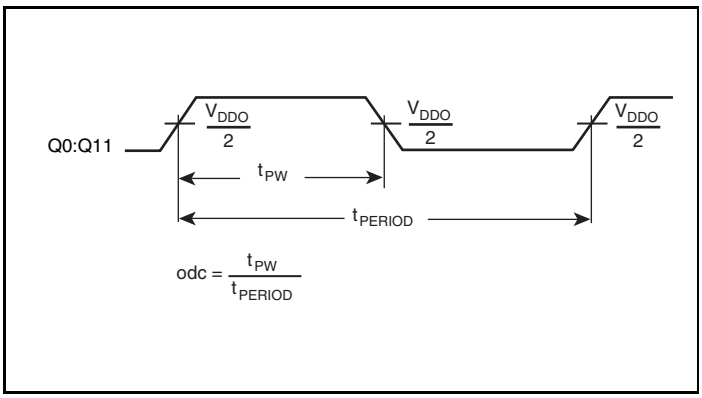
Output Skew



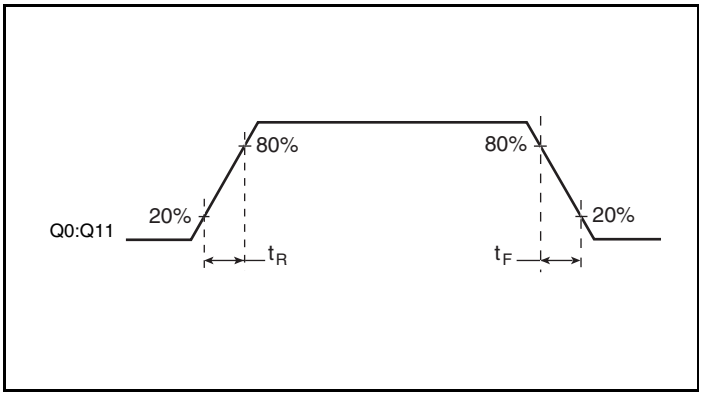
Part-to-Part Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs:

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8312 is: 339

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

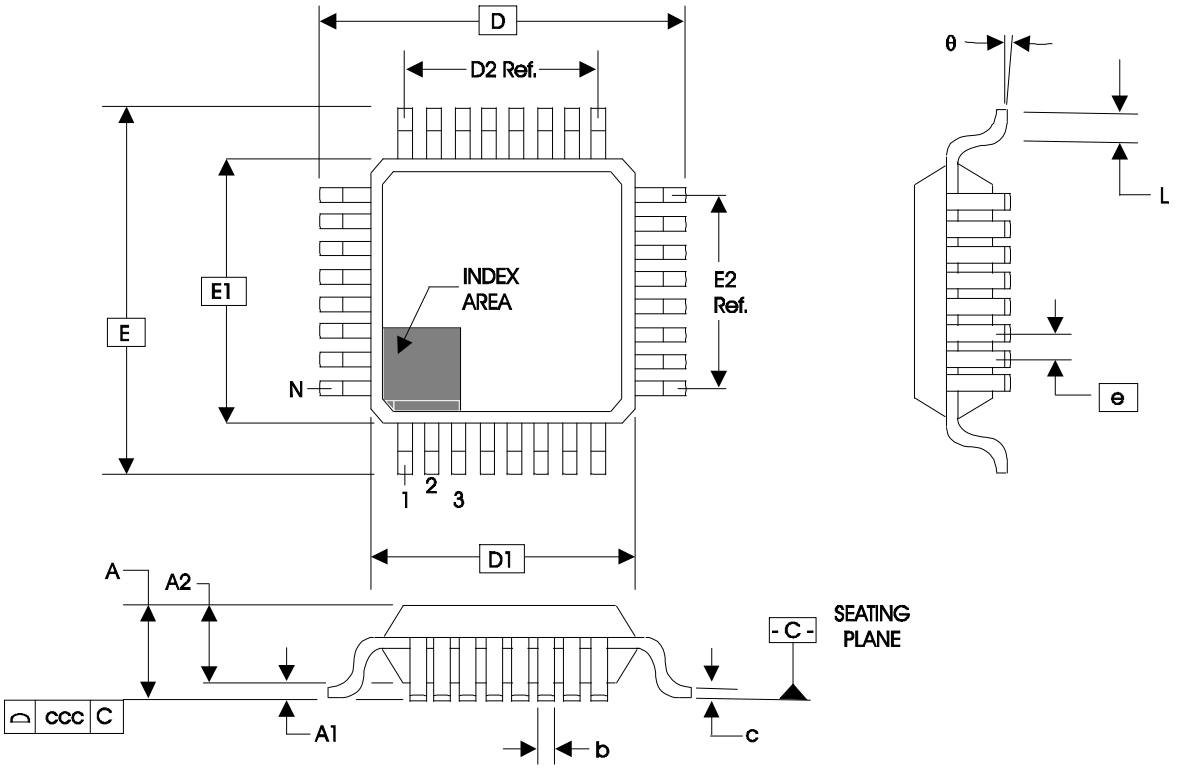


Table 7. Package Dimensions for 32 Lead LQFP

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10
N		32	

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8312AYLF	ICS8312AYLF	“Lead-Free” 32 Lead LQFP	Tray	0°C to 85°C
8312AYLFT	ICS8312AYLF	“Lead-Free” 32 Lead LQFP	Tape & Reel	0°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T2 T4A - T4F	2 3	Pin Characteristics table - added category $C_{PD.}$ Power Supply tables - changed $_{IDD}$ & I_{DDO} max. current spec to 10µA and removed typical value.	2/25/03
C	 T2	1 2	Features section - corrected Output Skew typo error from 160ps to 150ps. Pin Characteristics table - changed C_{IN} 4pF max. to 4pF typical.	5/17/04
C	T8	11	Added Lead-Free part number to Ordering Information Table.	6/14/04
D	T5A - T5F	7 - 9 10 13	Added Additive Phase Jitter specs to AC Tables. Added Additive Phase Jitter Plot. Added *Recommendations for Unused Input & Output Pins* section. Updated datasheet to new format.	7/3/08
D	T8	16	Removed leaded orderable parts from Ordering Information table	11/14/12
D		1 1 16 16	Removed ICS Chip and HiPerClockS under General Description. Removed ICS in the part numbers. Removed reference to leaded parts in the Features Section. Removed LF note at the bottom of the Ordering Information table. Removed the quantity of 1000 from the Tape & Reel in the Ordering information table. Updated datasheet header and footer.	12/11/15

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.idt.com/go/support