阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任
  何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无
  法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获
  得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描
  叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有"数据手册"字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets".

NB7L11M

2.5 V/3.3 V Differential 1:2 Clock/Data Fanout Buffer/Translator with CML Outputs and Internal Termination

ON Semiconductor®

Description

The NB7L11M is a differential 1-to-2 clock/data distribution chip with internal source termination and CML output structure, optimized for low skew and minimal jitter. The device is functionally equivalent to the EP11, LVEP11, or SG11 devices. Device produces two identical output copies of clock or data operating up to 8 GHz or 12 Gb/s, respectively. As such, NB7L11M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications.

Inputs incorporate internal 50 Ω termination resistors and accept LVPECL, CML, LVCMOS, LVTTL, or LVDS (See Table 6). Differential 16 mA CML output provides matching internal 50 Ω terminations, and 400 mV output swings when externally terminated, 50 Ω to V_{CC} (See Figure 14).

The device is offered in a low profile 3x3 mm 16-pin QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency up to 8 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- < 0.5 ps of RMS Clock Jitter
- < 10 ps of Data Dependent Jitter
- 30 ps Typical Rise and Fall Times
- 110 ps Typical Propagation Delay
- 3 ps Typical Within Device Skew
- Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- CML Output Level (400 mV Peak-to-Peak Output) Differential Output Only
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V/3.3 V LVEL, LVEP, EP and SG Devices
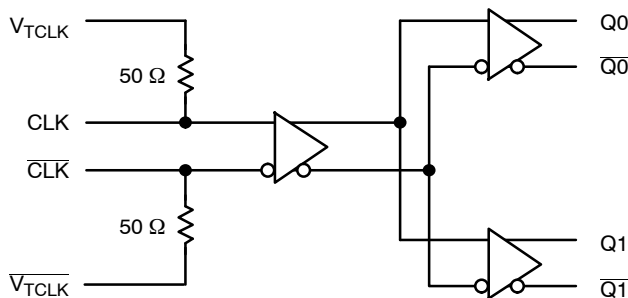- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

QFN–16
MN SUFFIX
CASE
485G–01

MARKING DIAGRAM*
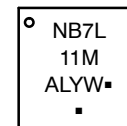
NB7L
11M
ALYW■
■

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
■	= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NB7L11MMNG	QFN–16 (Pb-Free)	123 Units/Tube
NB7L11MMNR2G	QFN–16 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Figure 1. Logic Diagram

NB7L11M
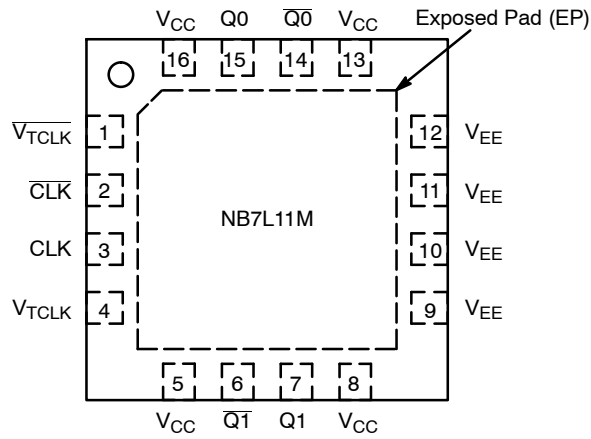
Figure 2. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{V_{TCLK}}$	−	Internal 50 Ω Termination Pin for $\overline{CLK}$
2	$\overline{CLK}$	LVPECL, CML, LVCMOS, LVTTL, LVDS	Inverted Differential Clock/Data Input. (Note 1)
3	CLK	LVPECL, CML, LVCMOS, LVTTL, LVDS	Non−inverted Differential Clock/Data Input. (Note 1)
4	V_{TCLK}	−	Internal 50 Ω Termination Pin for CLK
5,8,13,16	V_{CC}	−	Positive Supply Voltage. All V_{CC} pins must be externally connected to a Power Supply to guarantee proper operation.
6	$\overline{Q1}$	CML Output	Inverted $\overline{CLK}$ output 1 with internal 50 Ω source termination resistor. (Note 2)
7	Q1	CML Output	Non−inverted CLK output 1 with internal 50 Ω source termination resistor. (Note 2)
9,10,11,12	V_{EE}	−	Negative Supply Voltage. All V_{EE} pins must be externally connected to a Power Supply to guarantee proper operation.
14	$\overline{Q0}$	CML Output	Inverted $\overline{CLK}$ output 0 with internal 50 Ω source termination resistor. (Note 2)
15	Q0	CML Output	Non−inverted CLK output 0 with internal 50 Ω source termination resistor. (Note 2)
−	EP	−	Exposed Pad. The thermally exposed pad on package bottom (see case drawing) must be attached to a heatsinking conduit. It is recommended to connect the EP to the lower potential (V_{EE}).

1. In the differential configuration when the input termination pins (V_{TCLK}, $\overline{V_{TCLK}}$) are connected to a common termination voltage or left open, and if no signal is applied on CLK and $\overline{CLK}$ then the device will be susceptible to self−oscillation.
2. CML outputs require 50 Ω receiver termination resistor to V_{CC} for proper operation.

NB7L11M

Table 2. ATTRIBUTES

Characteristics	Value

ESD Protection
    Human Body Model
    Machine Model
    Charged Device Model
	> 1500 V
	> 50 V
	> 500 V

Moisture Sensitivity (Note 1)	Pb-Free Pkg
QFN-16	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	285
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	$V_{EE} = 0$ V		3.6	V
V_I	Input Voltage	$V_{EE} = 0$ V	$V_{EE} \perp \uparrow V_I \perp \uparrow V_{CC}$	3.6	V
V_{INPP}	Differential Input Voltage $|CLK - \overline{CLK}|$	$V_{CC} - V_{EE} \geq 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $|V_{CC} - V_{EE}|$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA
I_{out}	Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range	QFN−16		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 1)	0 lfpm 500 lfpm	QFN−16	42 36	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 1)	QFN−16	3 to 4	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 4. DC CHARACTERISTICS, CLOCK Inputs, CML Outputs

(V_{CC} = 2.375 V to 3.465 V, V_{EE} = 0 V, T_A = −40°C to +85°C) (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Input and Outputs open)		85	105	mA
V_{OH}	Output HIGH Voltage (Note 2)	V_{CC} − 60	V_{CC} − 20	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 2)	V_{CC} − 530	V_{CC} − 420	V_{CC} − 360	mV

Differential Input Driven Single-Ended (see Figures 10 & 12) (Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{th}	Input Threshold Reference Voltage Range (Note 3)	1125		V_{CC} − 75	mV
V_{IH}	Single-ended Input HIGH Voltage (Note 4)	V_{th} + 75		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage (Note 4)	V_{EE}		V_{th} − 75	mV

Differential Inputs Driven Differentially (see Figures 11 & 13) (Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{IHCLK}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILCLK}	Differential Input LOW Voltage	V_{EE}		V_{CC} − 75	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	1163		V_{CC} − 38	mV
V_{ID}	Differential Input Voltage (V_{IHCLK} − V_{ILCLK})	75		2500	mV
I_{IH}	Input HIGH Current CLK / $\overline{CLK}$ (V_{TCLK}/$\overline{V_{TCLK}}$ Open)	0	25	100	μA
I_{IL}	Input LOW Current CLK / $\overline{CLK}$ (V_{TCLK}/$\overline{V_{TCLK}}$ Open)	−10	0	10	μA
R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω
$R_{Temp\ Coef}$	Internal I/O Termination Resistor Temperature Coefficient		6.38		mΩ/°C

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}.
2. CML outputs require 50 Ω receiver termination resistors to V_{CC} for proper operation.
3. V_{th} is applied to the complementary input when operating in single-ended mode.
4. V_{CMR} min varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}.

Table 5. AC CHARACTERISTICS (V_{CC} = 2.375 V to 3.465 V, V_{EE} = 0 V; Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@$V_{INPPmin}$) (See Figure 3) $\quad f_{in} \leq 6$ GHz $\quad f_{in} \leq 8$ GHz	280 140	400 300		280 140	400 300		280 140	400 300		mV
f_{data}	Maximum Operating Data Rate	10	12		10	12		10	12		Gb/s
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	70	110	150	70	110	150	70	110	150	ps
t_{SKEW}	Duty Cycle Skew (Note 2) Within-Device Skew Device-to-Device Skew (Note 3)		2.0 3.0 20	5.0 15 50		2.0 3.0 20	5.0 15 50		2.0 3.0 20	5.0 15 50	ps
t_{JITTER}	RMS Random Clock Jitter (Note 4) $\quad f_{in} = 6$ Ghz $\quad f_{in} = 8$ Ghz Peak/Peak Data Dependent Jitter (Note 5) $\quad f_{in} = 2.488$ Gb/s $\quad f_{data} = 5$ Gb/s $\quad f_{data} = 10$ Gb/s		0.2 0.2 2.0 3.0 5.0	0.5 0.5 5.0 8.0 10		0.2 0.2 2.0 3.0 5.0	0.5 0.5 5.0 8.0 10		0.2 0.2 2.0 3.0 5.0	0.5 0.5 5.0 8.0 10	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 6)	75	400	2500	75	400	2500	75	400	2500	mV
t_r t_f	Output Rise/Fall Times @ 1 Ghz (20% – 80%) Q, $\overline{Q}$		30	60		30	60		30	60	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured by forcing V_{INPP} (TYP) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20% – 80%).
2. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw– and Tpw+ @1 GHz.
3. Device to device skew is measured between outputs under identical transition @ 1 GHz.
4. Additive RMS jitter with 50% duty cycle clock signal at 8 GHz & 10 GHz.
5. Additive peak-to-peak data dependent jitter with input NRZ data at PRBS 2^{23}–1.
6. V_{INPP} (MAX) cannot exceed V_{CC} – V_{EE}. Input voltage swing is a single-ended measurement operating in differential mode.
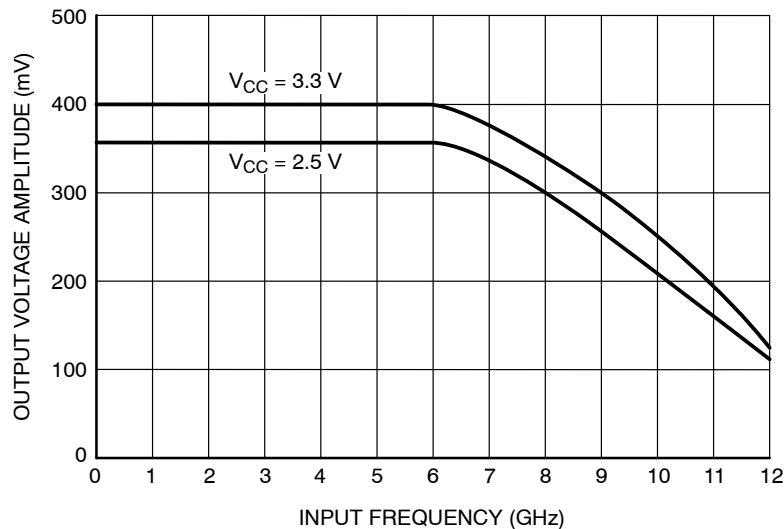
Figure 3. Output Voltage Amplitude (V_{OUTPP}) Versus Input Clock Frequency (f_{in}) at Ambient Temperature (Typical) (V_{INPP} = 400 mV)
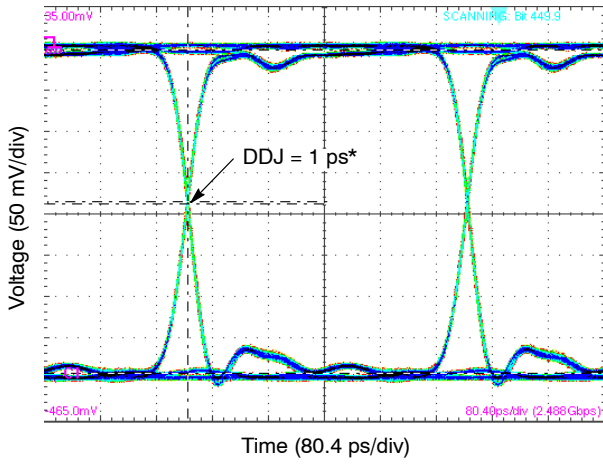
Figure 4. Typical Output Waveform at 2.488 Gb/s
with PRBS 2^23−1 (V$_{inpp}$ = 75 mV)

*Input signal DDJ = 6.4 ps
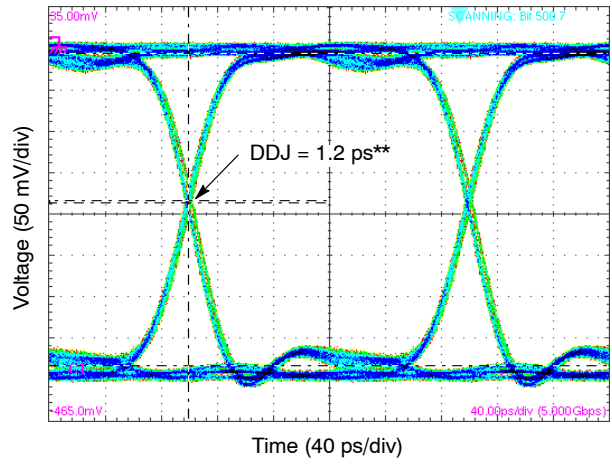
Figure 5. Typical Output Waveform at 5 Gb/s
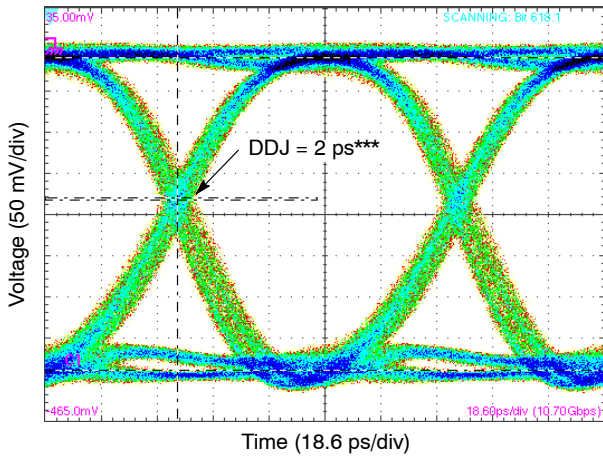with PRBS 2^23−1 (V$_{inpp}$ = 75 mV)

**Input signal DDJ = 7.2 ps

Figure 6. Typical Output Waveform at 10.7 Gb/s
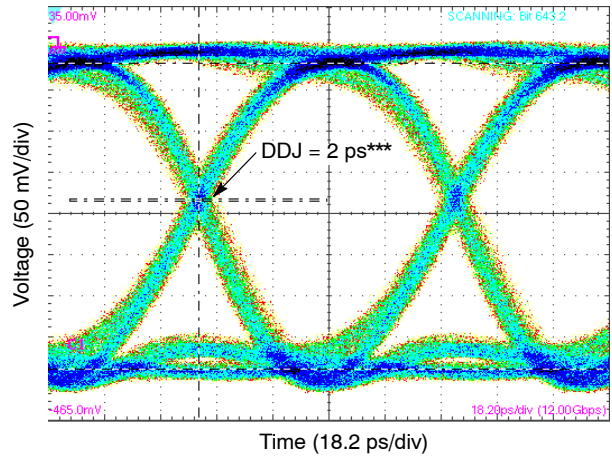with PRBS 2^23−1 (V$_{inpp}$ = 75 mV)

***Input signal DDJ = 11 ps

Figure 7. Typical Output Waveform at 12 Gb/s
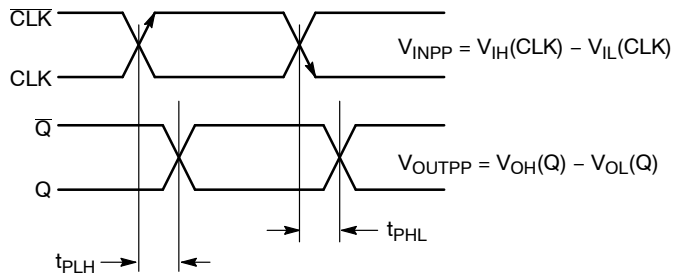with PRBS 2^23−1 (V$_{inpp}$ = 75 mV)

***Input signal DDJ = 13 ps

Figure 8. AC Reference Measurement

$V_{INPP} = V_{IH}(CLK) - V_{IL}(CLK)$

$V_{OUTPP} = V_{OH}(Q) - V_{OL}(Q)$
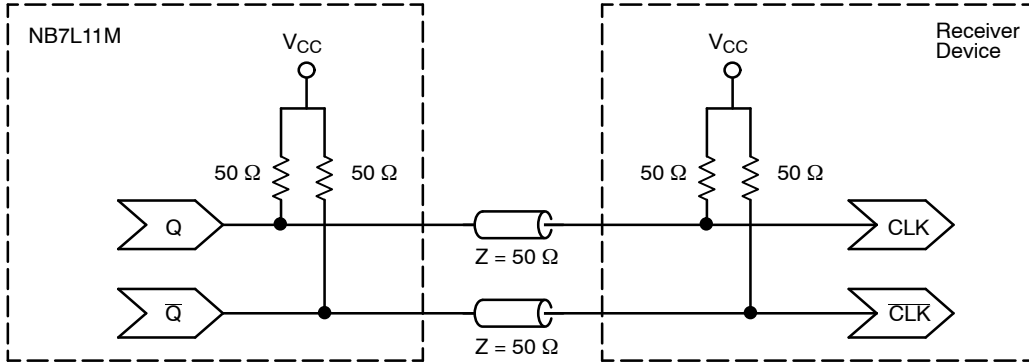
**Figure 9. Typical Termination for Output Driver Using External Termination Resistor
(Refer to Application Notes AND8020/D and AND8173/D)**
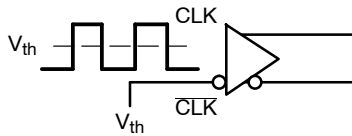
**Figure 10. Differential Input Driven
Single-Ended**
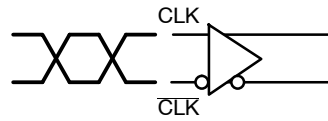
**Figure 11. Differential Inputs Driven
Differentially**
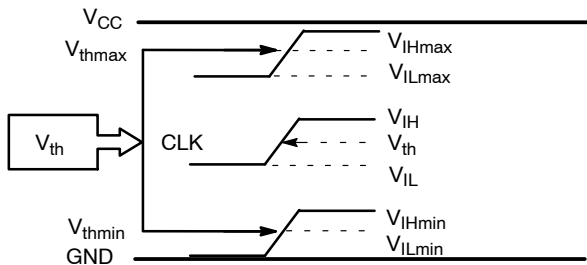
Figure 12. V$_{th}$ Diagram

$V_{(CLK)} = V_{IHCLK} - V_{ILCLK}$
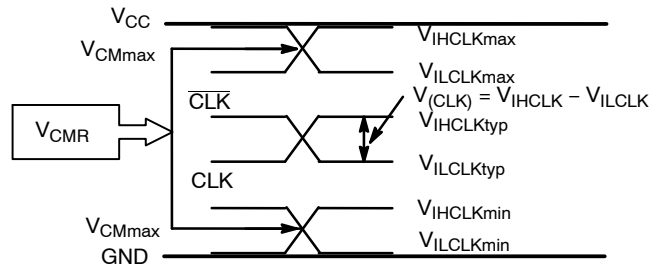
Figure 13. V$_{CMR}$ Diagram

NB7L11M
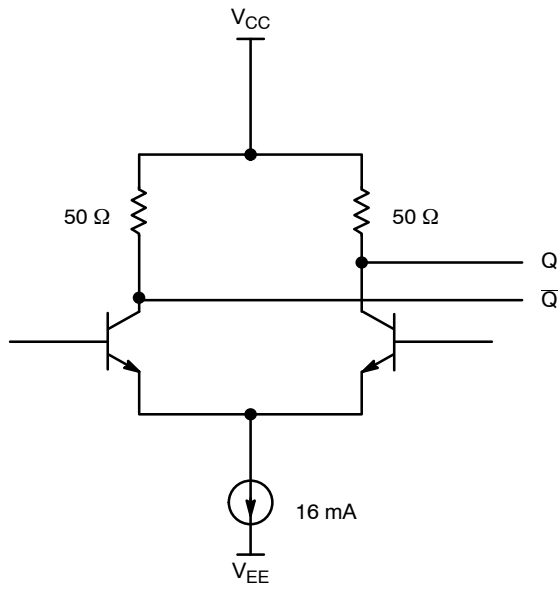
Figure 14. CML Output Structure

Table 6. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect V_{TCLK}, $\overline{V_{TCLK}}$ to V_{CC}
LVDS	Connect V_{TCLK}, $\overline{V_{TCLK}}$ together CLK input
AC-COUPLED	Bias V_{TCLK}, $\overline{V_{TCLK}}$ Inputs within (V_{CMR}) Common Mode Range
RSECL, LVPECL	Standard ECL Termination Techniques. See AND8020/D.
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs.

NB7L11M

Application Information

All NB7L11M inputs can accept PECL, CML, LVTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω).
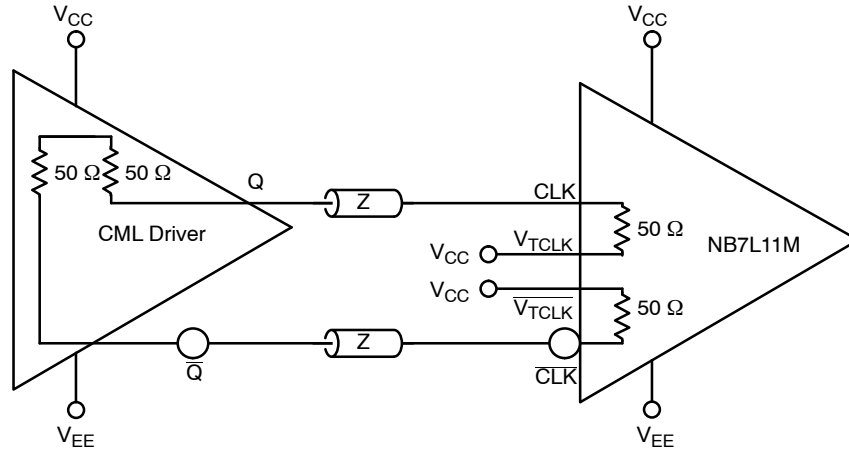
Figure 15. CML to CML Interface

Recommended R_T Values	
V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω
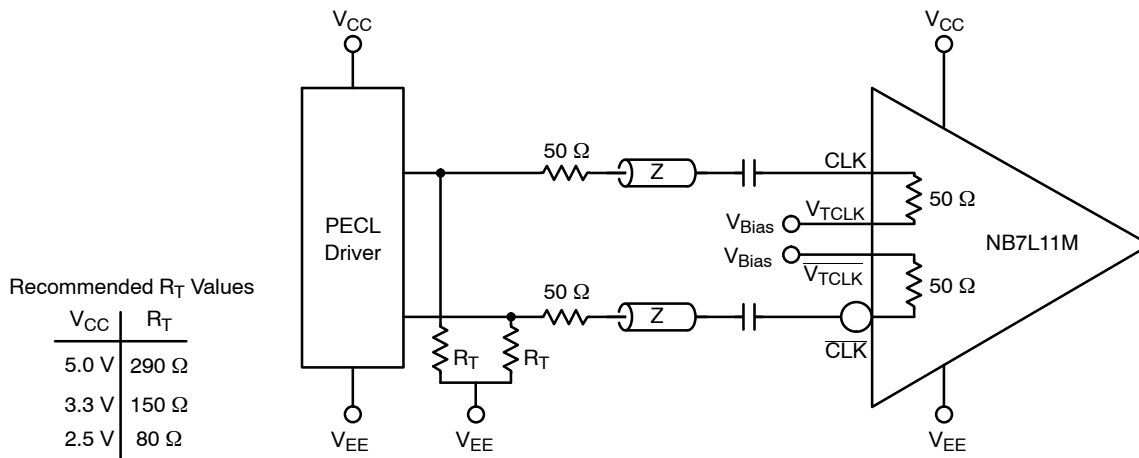
Figure 16. PECL to CML Receiver Interface

NB7L11M
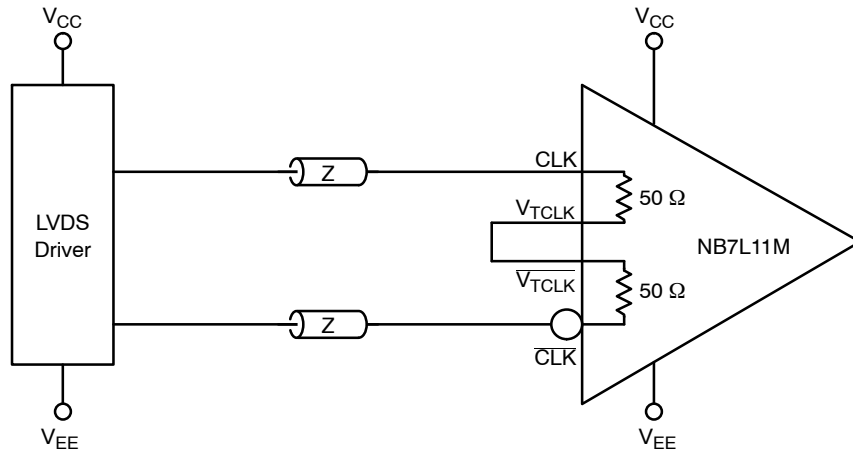
Figure 17. LVDS to CML Receiver Interface
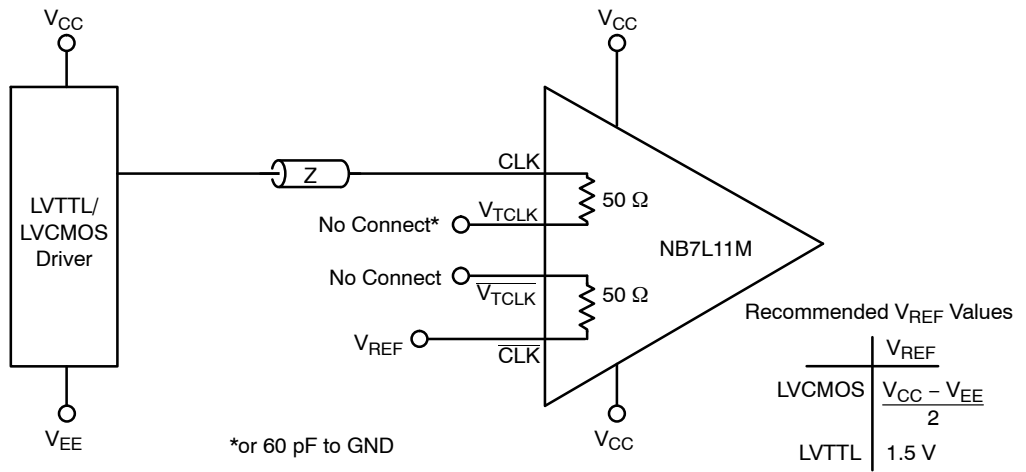
Figure 18. LVCMOS/LVTTL to CML Receiver Interface

Recommended V_{REF} Values

	V_{REF}
LVCMOS	$\dfrac{V_{CC} - V_{EE}}{2}$
LVTTL	1.5 V

*or 60 pF to GND

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G−01
ISSUE F

TOP VIEW

PIN 1 LOCATION

2X [⌴ 0.10 C]

2X [⌴ 0.10 C]

SIDE VIEW

[⟋ 0.05 C]

[⌴ 0.05 C]

NOTE 4

DETAIL B

(A3)

A

A1

[C] SEATING PLANE

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

L   L

L1

DETAIL B
ALTERNATE CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

A3

A1
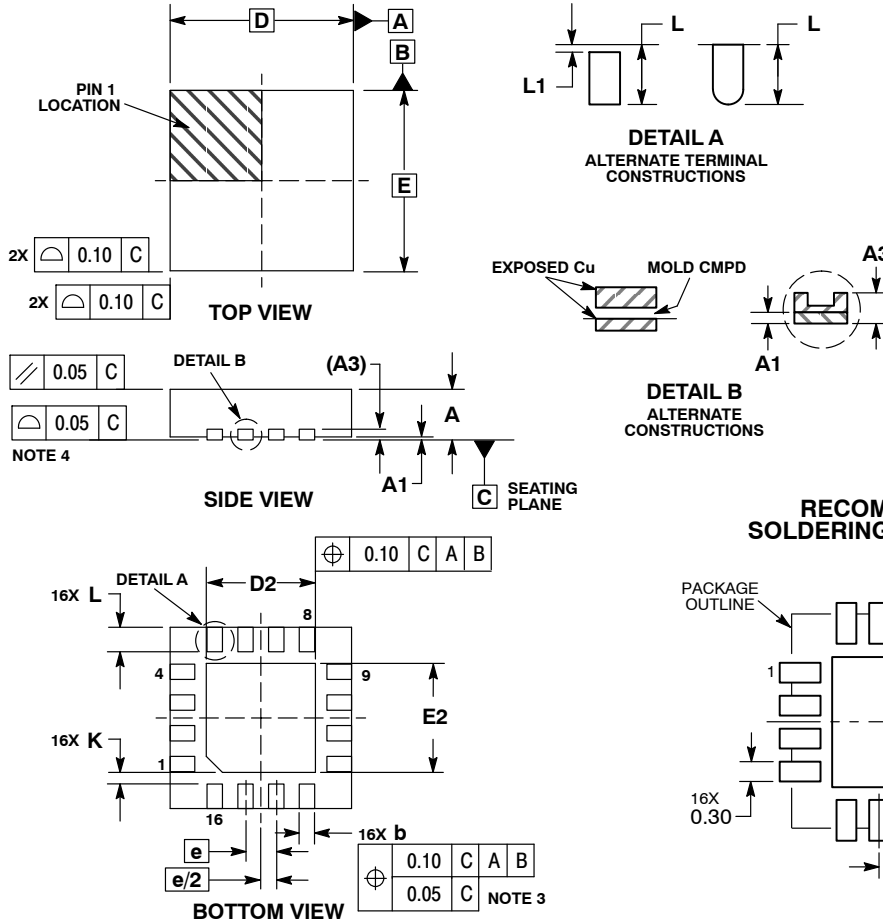
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

BOTTOM VIEW

[⊕ 0.10 C A B]

DETAIL A

D2

16X L

16X K

16X b

16X b

e

e/2

[⊕ 0.10 C A B]
[0.05 C] NOTE 3

E2

RECOMMENDED SOLDERING FOOTPRINT*

PACKAGE OUTLINE

16X 0.58

2X 1.84   2X 3.30

16X 0.30

0.50 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ECLinPS is a registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.