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General Description

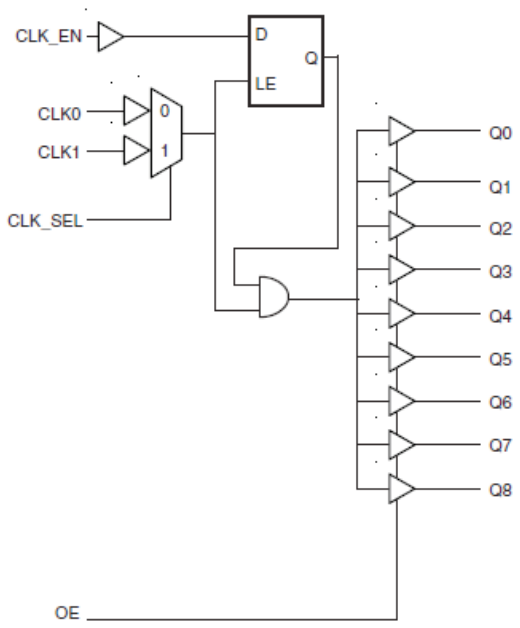
The 83947I-147 is a low skew, 1-to-9 LVCMOS/LVTTL Fanout Buffer. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 9 to 18 by utilizing the ability of the outputs to drive two series terminated lines.

Guaranteed output and part-to-part skew characteristics make the 83947I-147 ideal for high performance, 3.3V or 2.5V single ended applications.

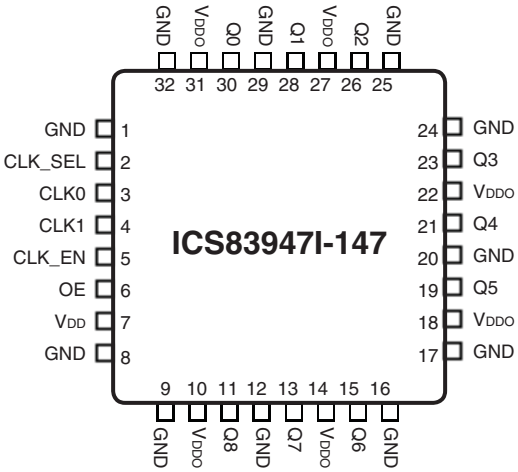
Features

- Nine LVCMOS/LVTTL outputs
- Selectable CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum output frequency: 250MHz
- Output skew: 115ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Additive phase jitter, RMS: 0.02ps (typical) @ 3.3V
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	GND	Power		Power supply ground.
2	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
3, 4	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVCMOS / LVTTL interface levels.
5	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTL interface levels.
6	OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels.
7	V_{DD}	Power		Core supply pin.
10, 14, 18, 22, 27, 31	V_{DDO}	Power		Output supply pins.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Q0 thru Q8 clock outputs. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			12		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
R_{OUT}	Output Impedance			7		Ω

Table 3. Output Enable and Clock Enable Function Table

Control Inputs		Output
OE	**CLK_EN**	**Q0:Q8**
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±0.3V$ or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	V
I_{DD}	Input Supply Current				50	mA
I_{DDO}	Output Supply Current				9	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±0.3V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		3.6	V
V_{IL}	Input Low Voltage					0.8	V
I_{IN}	Input Current	CLK0, CLK1, OE, CLK_SEL, CLK_EN		-100			µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 20mA			0.4	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, *3.3V Output Load Test Circuit Diagram.*

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 2.5V±5%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
		CLK_SEL, CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, OE, CLK_SEL, CLK_EN	$V_{DD} = V_{IN}$ = 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, OE, CLK_SEL, CLK_EN	V_{DD} = 32.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, *2.5V Output Load Test Circuit Diagram.*

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, NOTE 1	f ≤ 250MHZ	2		4.2	ns
*t*sk(o)	Output Skew; NOTE 2, 5	Measured on rising edge @V_{DDO}/2			115	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5	Measured on rising edge @V_{DDO}/2			500	ps
tjit(Ø)	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	(12KHz to 20MHz)		0.2		ps
t_R / t_F	Output Rise/Fall Time	0.8V to 2.0V	0.2		1	ns
t_{PW}	Output Pulse Width	f > 133MHz	t_{Period}/2 - 1		t_{Period}/2 + 1	ns
odc	Output Duty Cycle	f ≤ 133MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 4				10	ns
t_{DIS}	Output Disable Time; NOTE 4				10	ns
t_S	Clock Enable Setup Time		0			ns
t_S	Clock Enable Hold Time		1			ns

All parameters measured at frequencies less than or equal to 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

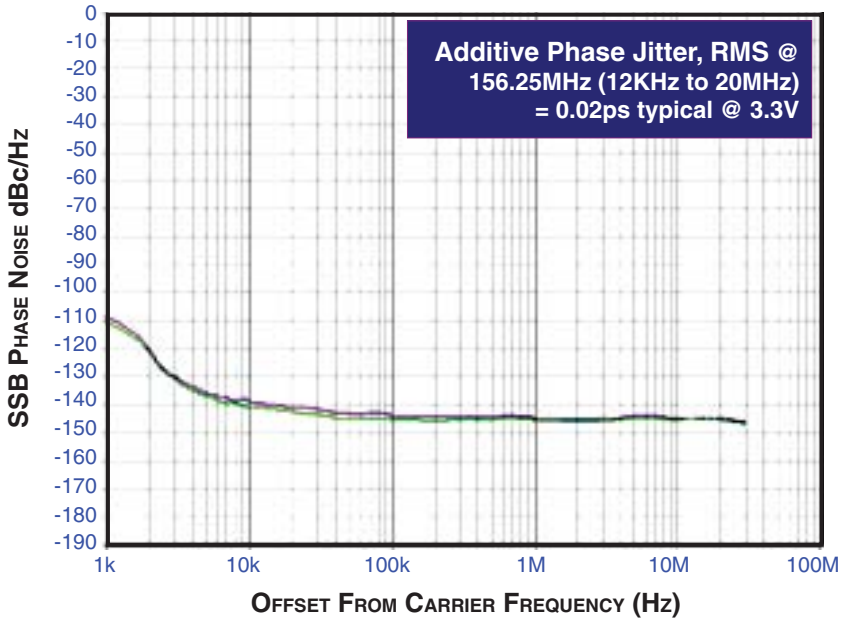
TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

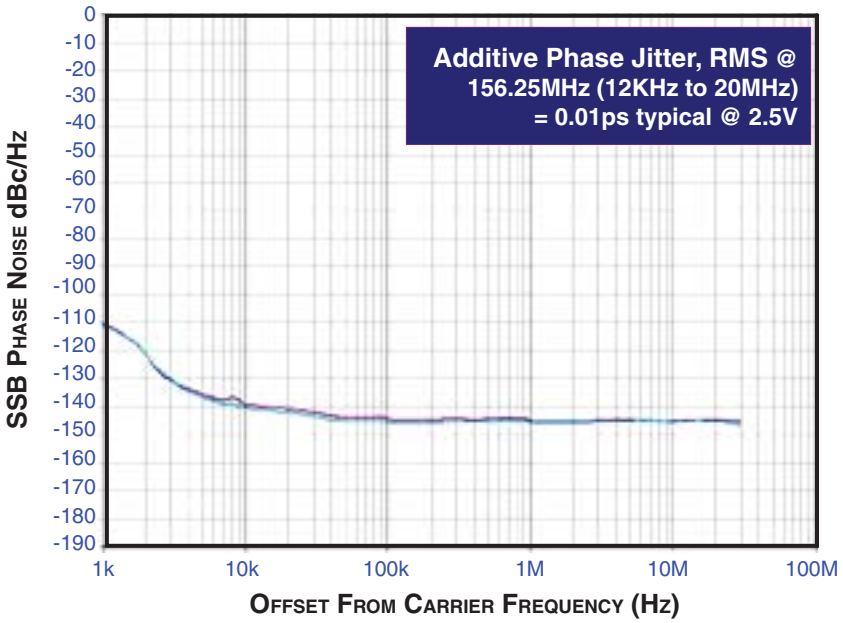
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay, NOTE 1	f ≤ 250MHZ	2.4		4.5	ns
tsk(o)	Output Skew; NOTE 2, 5	Measured on rising edge @V_{DDO}/2			130	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 5	Measured on rising edge @V_{DDO}/2			600	ps
tjit(Ø)	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	(12KHz to 20MHz)		0.1		ps
t_R / t_F	Output Rise/Fall Time	20% - 80%	300		800	ps
t_{PW}	Output Pulse Width		t_{Period}/2 - 1.2		t_{Period}/2 + 1.2	ns
t_{EN}	Output Enable Time; NOTE 4				10	ns
t_{DIS}	Output Disable Time; NOTE 4				10	ns
t_S	Clock Enable Setup Time		0			ns
t_S	Clock Enable Hold Time		1			ns

All parameters measured at frequencies less than or equal to 250MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

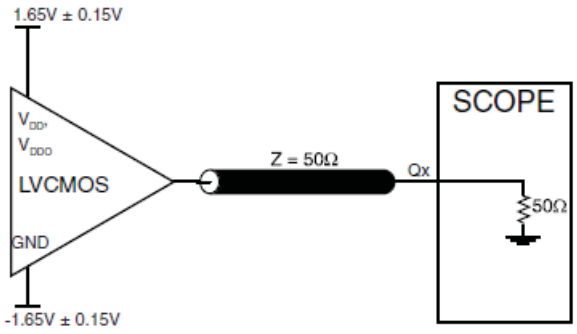
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



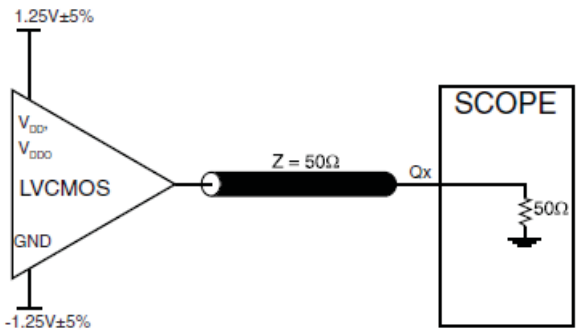


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

Parameter Measurement Information

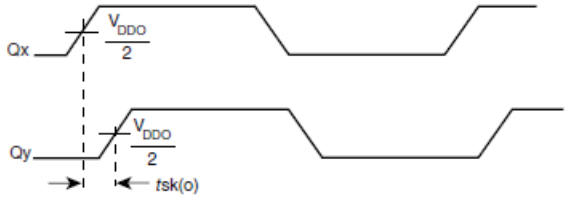


3.3V Output Load AC Test Circuit

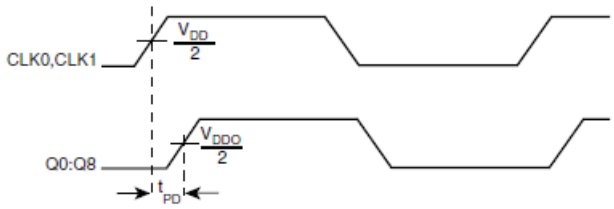


2.5V Output Load AC Test Circuit

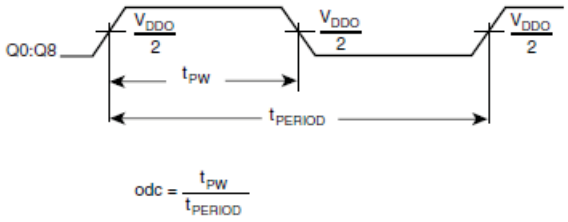
Part-to-Part Skew



Output Skew

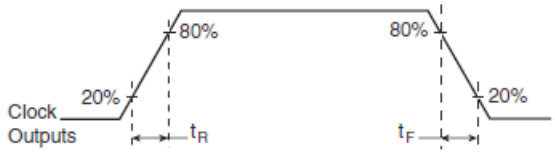


Propagation Delay



Output Duty Cycle/Pulse Width/Period

3.3V Output Rise/Fall Time



2.5V Output Rise/Fall Time

Application Schematic Example

Figure 1 shows an example of 83947I-147 application schematic. In this example, the device is operated at V_{CC}=3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVCMOS driver. For the LVCMOS output drivers, only one termination example is shown in this schematic. Additional termination approaches are shown in the LVCMOS Termination Application Note (refer to ICS website).

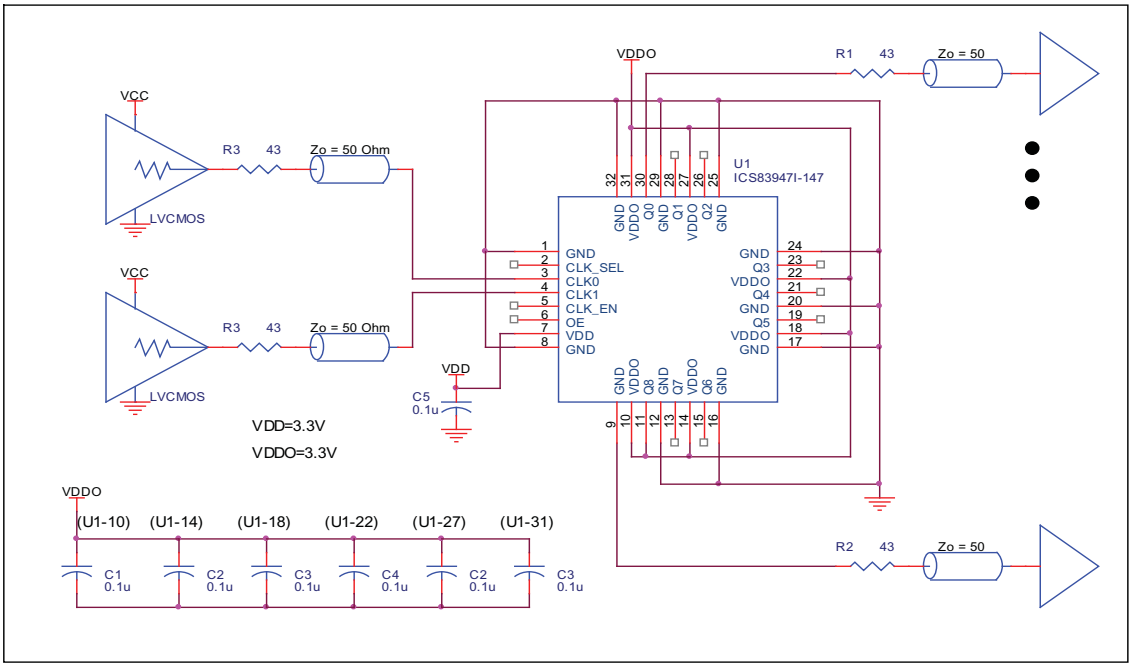


Figure 1. 83947I-147 Schematic Layout

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 83947I-147 is: 1040

Package Outline - Y Suffix for 32 Lead LQFP

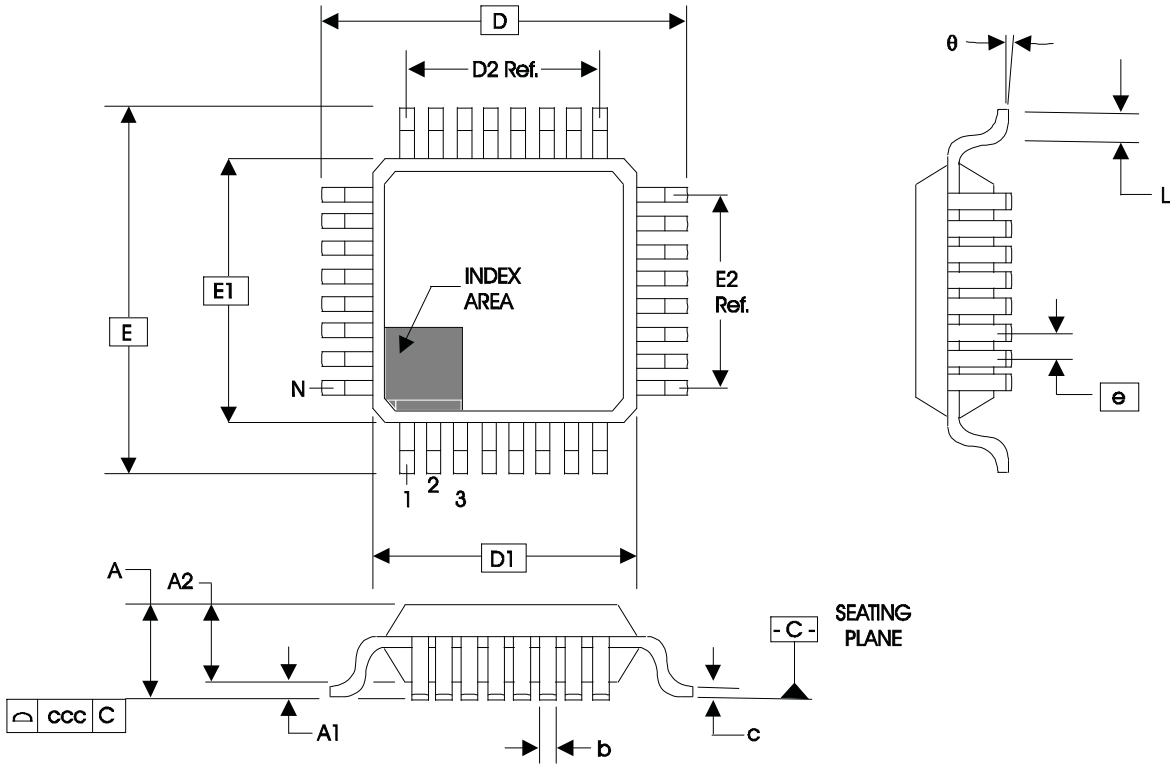


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83947AYI-147LF	ICS947AI147L	Lead-Free, 32 Lead LQFP	Tray	-40°C to 85°C
83947AYI-147LFT	ICS947AI147L	Lead-Free, 32 Lead LQFP	Tape & Reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	10 12	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/12/10
A	T8	10	Ordering Information Table - added lead-free ordering information. Deleted non lead-free ordering information. Deleted tape & reel count.	2/27/13
A			Removed ICS from part numbers where needed. Updated header and footer.	3/18/16

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