

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NB6L611

2.5V / 3.3V 1:2 Differential LVPECL Clock / Data Fanout Buffer

Multi-Level Inputs with Internal Termination

Description

The NB6L611 is a differential 1:2 clock or data fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VTD pins and will accept LVPECL, CML, LVDS, LVCMOS or LVTTTL logic levels.

The V_{REFAC} reference output can be used to rebias capacitor-coupled differential or single-ended input signals. When used, decouple V_{REFAC} with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When used, decouple V_{REFAC} with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{REFAC} output should be left open.

The device is housed in a small 3x3 mm 16 pin QFN package.

The NB6L611 is a member of the ECLinPS MAX™ family of high performance clock and data management products.

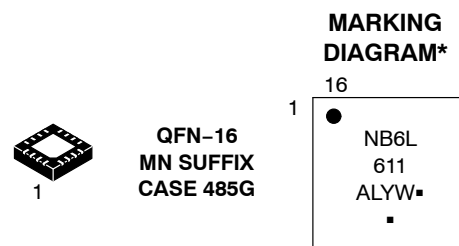
Features

- Input Clock Frequency > 4.0 GHz
- 280 ps Typical Propagation Delay
- 100 ps Typical Rise and Fall Times
- 0.5 ps maximum RMS Clock Jitter
- Differential LVPECL Outputs, 780 mV Amplitude, typical
- LVPECL Operating Range: V_{CC} = 2.375 V to 3.63 V with V_{EE} = 0 V
- NECL Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.63 V
- Internal Input Termination Resistors, 50 Ω
- V_{REFAC} Reference Output Voltage
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



ON Semiconductor®

<http://onsemi.com>



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

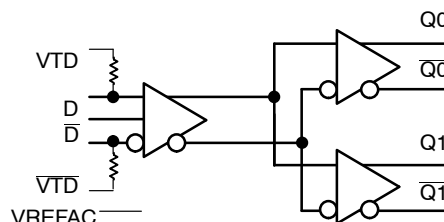


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NB6L611

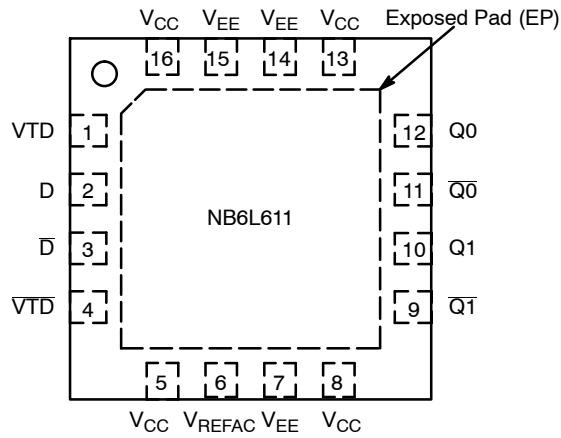


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTD	-	Internal 50 Ω Termination Pin for D input.
2	D	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input. Note1. Internal 50 Ω Resistor to Termination Pin, VTD.
3	\bar{D}	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input. Note 1. Internal 50 Ω Resistor to Termination Pin, \bar{VTD} .
4	\bar{VTD}	-	Internal 50 Ω Termination Pin for \bar{D} input.
5	VCC	-	Positive Supply Voltage
6	VREFAC		Output Reference Voltage for direct or capacitor coupled inputs
7	VEE	-	Negative Supply Voltage
8	VCC	-	Positive Supply Voltage
9	$\bar{Q1}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to VCC - 2.0 V.
10	Q1	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to VCC - 2.0 V.
11	$\bar{Q0}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to VCC - 2.0 V.
12	Q0	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to VCC - 2.0 V.
13	VCC	-	Positive Supply Voltage
14	VEE	-	Negative Supply Voltage
15	VEE	-	Negative Supply Voltage
16	VCC	-	Positive Supply Voltage
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to VEE on the PC board.

1. In the differential configuration when the input termination pins (VTD, \bar{VTD}) are connected to a common termination voltage or left open, and if no signal is applied on D/D input, then, the device will be susceptible to self-oscillation.
2. All VCC and VEE pins must be externally connected to a power supply for proper operation.

NB6L611

Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200V
Moisture Sensitivity	16-QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	V _{EE} = 0 V		4.0	V
V _{EE}	Negative Power Supply	V _{CC} = 0 V		-4.0	V
V _{IO}	Positive Input/Output Voltage Negative Input/Output Voltage	V _{EE} = 0 V V _{CC} = 0 V	-0.5 ≤ V _{Io} ≤ V _{CC} + 0.5 +0.5 ≥ V _{Io} ≥ V _{EE} - 0.5	4.5 -4.5	V V
V _{INPP}	Differential Input Voltage D - D̄			V _{CC} -V _{EE}	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		45 80	mA mA
I _{OUT}	Output Current (LVPECL Output)	Continuous Surge		50 100	mA mA
I _{VREFAC}	V _{REFAC} Sink/Source Current			±2.0	mA
T _A	Operating Temperature Range	16 QFN		-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	42 35	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 3)	QFN-16	4	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB6L611

Table 4. DC CHARACTERISTICS, Multi-Level Inputs $V_{CC} = 2.375\text{ V to }3.63\text{ V}$, $V_{EE} = 0\text{ V}$, or $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V to }-3.63\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
--------	----------------	-----	-----	-----	------

POWER SUPPLY CURRENT

I_{CC}	Power Supply Current (Inputs and Outputs Open)	30	45	60	mA
----------	--	----	----	----	----

LVPECL OUTPUTS (Notes 4 and 5)

V_{OH}	Output HIGH Voltage	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1075$ 2225 1425	$V_{CC} - 950$ 2350 1550	$V_{CC} - 825$ 2475 1675	mV
V_{OL}	Output LOW Voltage	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1875$ 1475 675	$V_{CC} - 1725$ 1575 775	$V_{CC} - 1625$ 1675 875	mV

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 9 and 10) (Note 6)

V_{th}	Input Threshold Reference Voltage Range (Note 7)	$V_{EE} + 1050$		$V_{CC} - 150$	mV
V_{IH}	Single-ended Input HIGH Voltage	$V_{th} + 150$		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage	V_{EE}		$V_{th} - 150$	mV
V_{ISE}	Single-ended Input Voltage Amplitude ($V_{IH} - V_{IL}$)	300		$V_{CC} - V_{EE}$	mV

V_{REFAC}

V_{REFAC}	Output Reference Voltage ($V_{CC} \geq 2.5\text{ V}$)	$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	mV
-------------	---	------------------	------------------	------------------	----

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 11, 12 and 13) (Note 8)

V_{IHD}	Differential Input HIGH Voltage	$V_{EE} + 1200$		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		$V_{CC} - 150$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	$V_{EE} + 150$		$V_{CC} - V_{EE}$	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note9)	$V_{EE} + 950$		$V_{CC} - 75$	mV
I_{IH}	Input HIGH Current D/\bar{D} , (V_{TD}/\bar{V}_{TD} Open)	-150		150	μA
I_{IL}	Input LOW Current D/\bar{D} , (V_{TD}/\bar{V}_{TD} Open)	-150		150	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor (Measured from D to VTD)	40	50	60	Ω
-----------	--	----	----	----	----------

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- LVPECL outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$ for proper operation.
- Input and output parameters vary 1:1 with V_{CC} .
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} minimum varies 1:1 with V_{EE} . V_{CMR} maximum varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

NB6L611

Table 5. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.63\text{ V}$, $V_{EE} = 0\text{ V}$, or $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V to }-3.63\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$; (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit	
V_{OUTPP}	Output Voltage Amplitude (@ V_{INPP}) (Note 14) (See Figure 3)	$f_{in} \leq 1.5\text{ GHz}$ 725 $f_{in} = 2.0\text{ GHz}$ 520 $f_{in} = 3.0\text{ GHz}$ 320 $f_{in} = 4.0\text{ GHz}$ 170	780 680 500 400		mV	
t_{PD}	Propagation Delay D to Q	225	280	375	ps	
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew Device to Device Skew (Note 12)		3	15 15 80	ps	
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq 4.0\text{ GHz}$	40	50	60	ps
t_{JITTER}	RMS Random Clock Jitter (Note 13)	$f_{in} \leq 4.0\text{ GHz}$		0.2	0.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14)	150		$V_{CC} - V_{EE}$	mV	
t_r, t_f	Output Rise/Fall Times @ 0.5 GHz (20% – 80%) Q, \bar{Q}		100	170	ps	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. All loading with an external $R_L = 50\ \Omega$ to $V_{CC} - 2.0\text{ V}$. Input edge rates 40 ps (20% – 80%).

11. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @ 0.5GHz.

12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.

13. Additive RMS jitter with 50% duty cycle clock signal.

14. Input and output voltage swing is a single-ended measurement operating in differential mode.

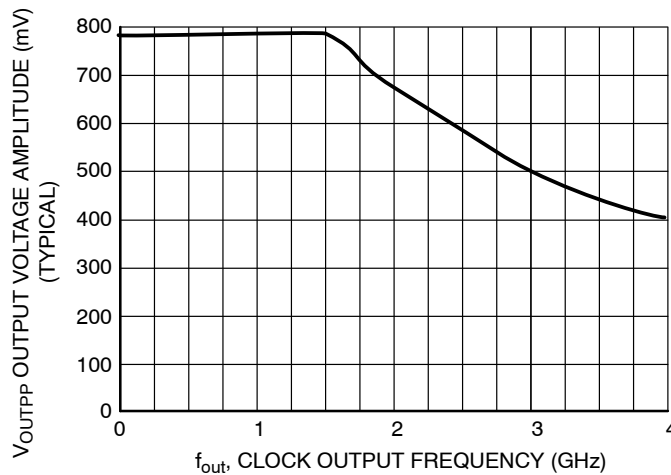


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Output Frequency at Ambient Temperature (Typical)

NB6L611

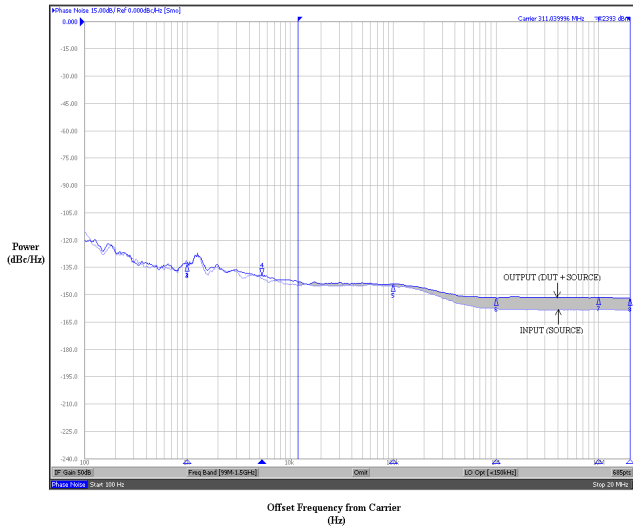


Figure 4. Typical Phase Noise Plot at $f_{\text{carrier}} = 311.04 \text{ MHz}$

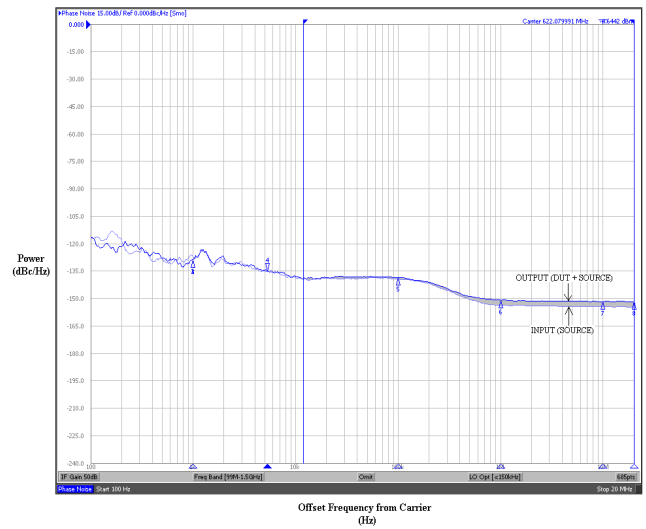


Figure 5. Typical Phase Noise Plot at $f_{\text{carrier}} = 622.08 \text{ MHz}$

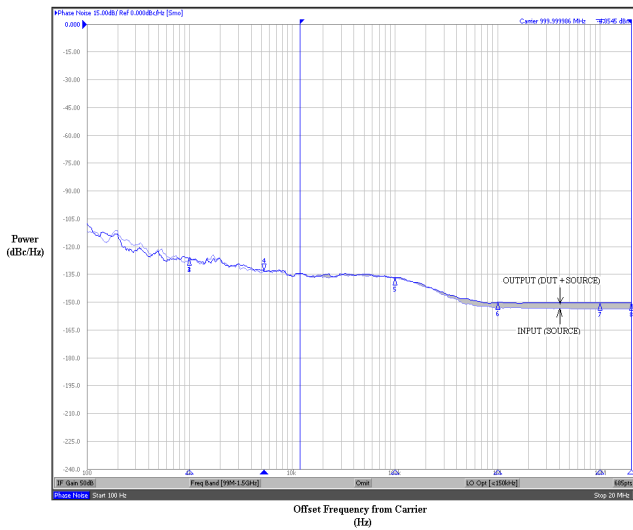


Figure 6. Typical Phase Noise Plot at $f_{\text{carrier}} = 1 \text{ GHz}$

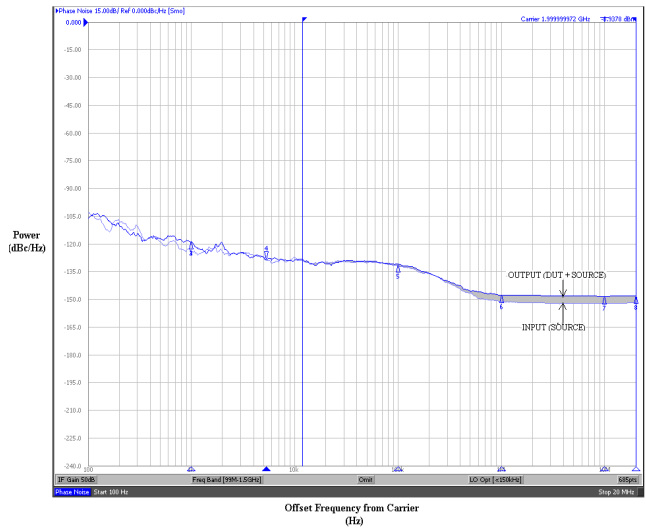


Figure 7. Typical Phase Noise Plot at $f_{\text{carrier}} = 2 \text{ GHz}$

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L611 device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 44 fs, 11 fs, 8 fs and 6 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

NB6L611

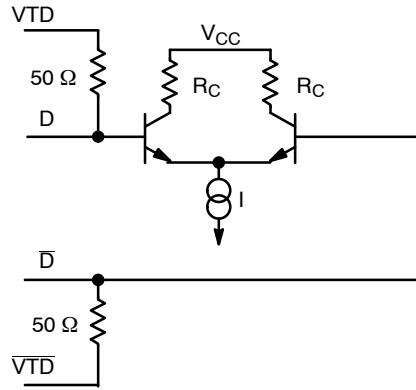


Figure 8. Input Structure

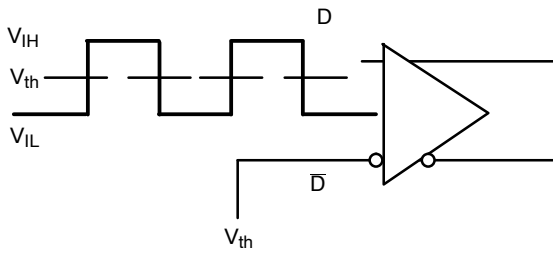


Figure 9. Differential Input Driven Single-Ended

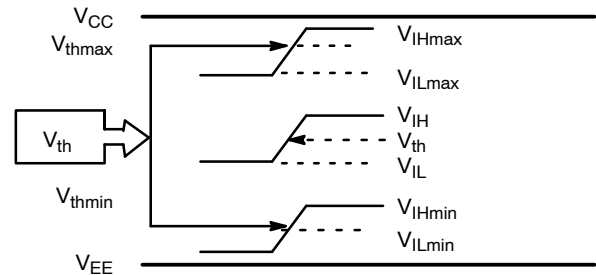


Figure 10. V_{th} Diagram

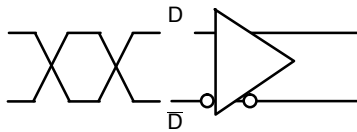


Figure 11. Differential Inputs Driven Differentially

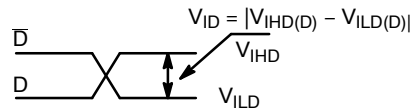


Figure 12. Differential Inputs Driven Differentially

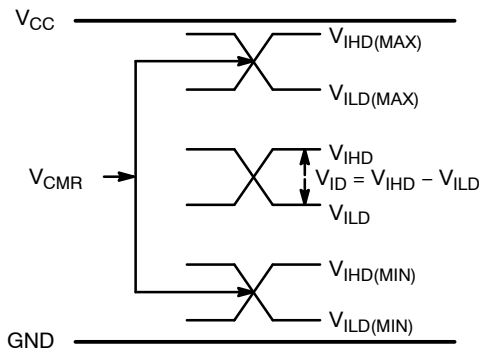


Figure 13. V_{CMR} Diagram

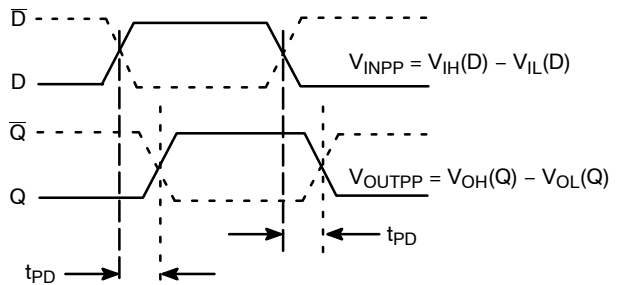


Figure 14. AC Reference Measurement

NB6L611

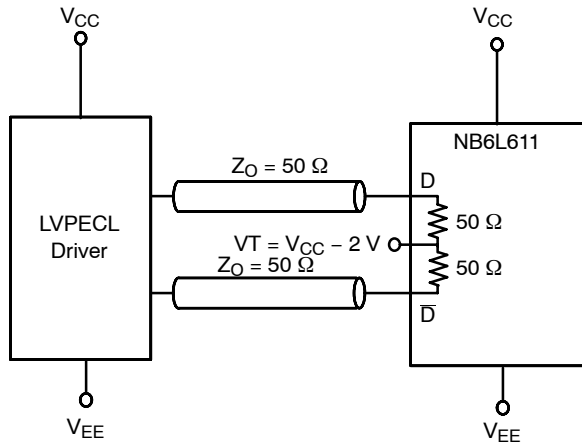


Figure 15. LVPECL Interface

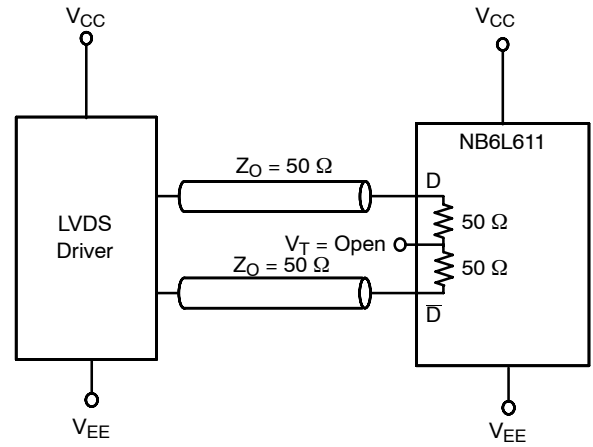


Figure 16. LVDS Interface

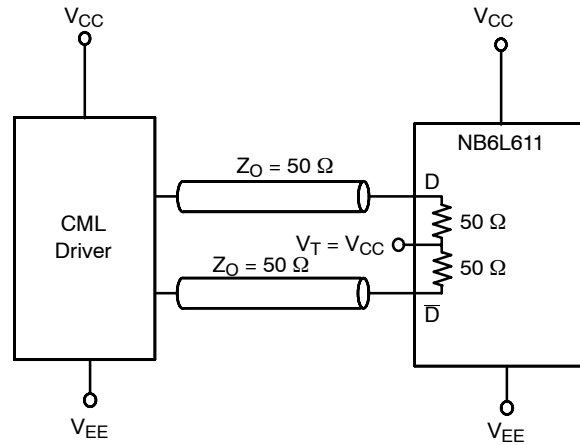


Figure 17. Standard 50 Ω Load CML Interface

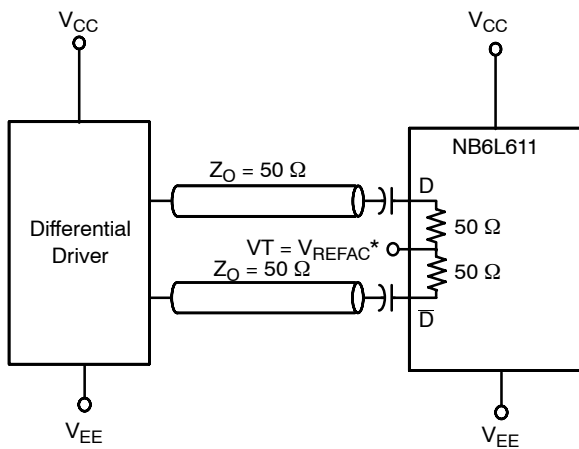


Figure 18. Capacitor-Coupled Differential Interface
(VT Connected to V_{REFAC})

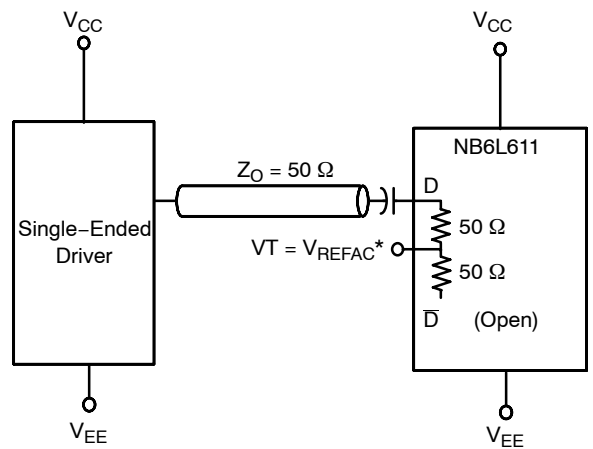
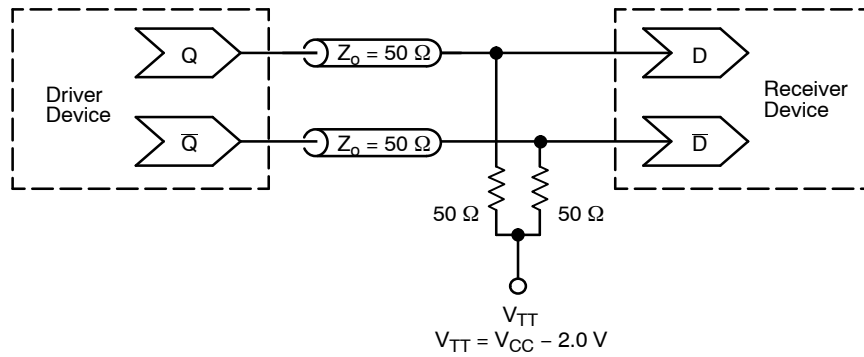


Figure 19. Capacitor-Coupled Single-Ended Interface
(VT Connected to V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μ F capacitor

NB6L611



**Figure 20. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

ORDERING INFORMATION

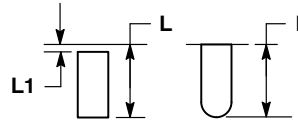
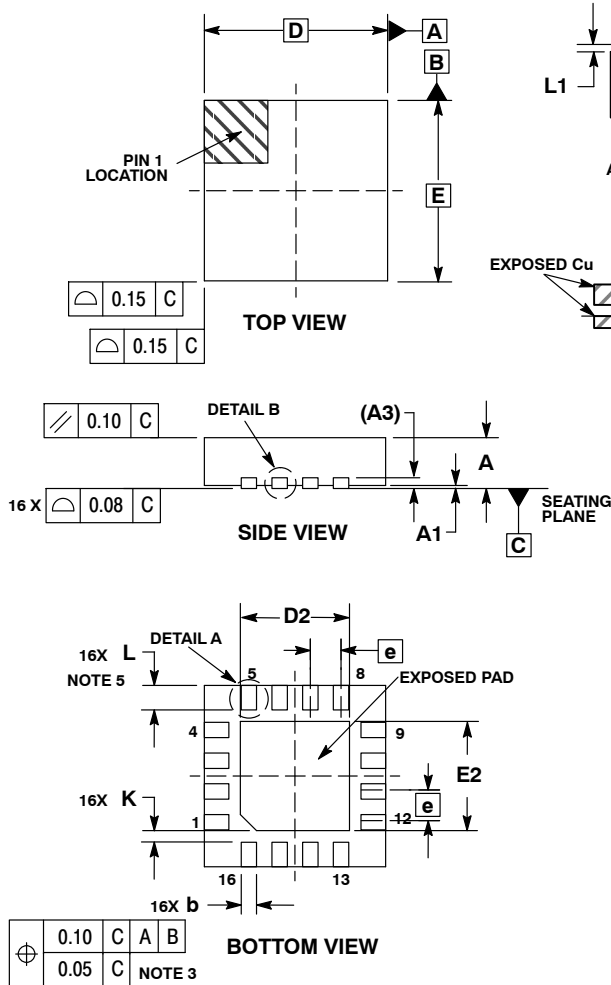
Device	Package	Shipping [†]
NB6L611MNG	QFN-16 (Pb-free)	123 Units / Rail
NB6L611MNR2G	QFN-16 (Pb-free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

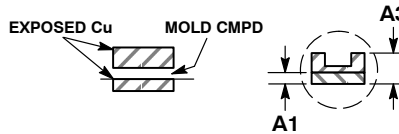
NB6L611

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G-01
ISSUE D



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



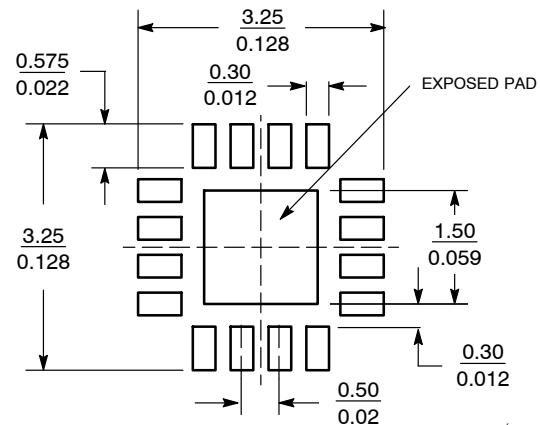
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50
L1	0.00	0.15

SOLDERING FOOTPRINT*



SCALE 10:1 ($\frac{\text{mm}}{\text{inches}}$)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NB6L611), may be covered by U.S. patents including 6,362,644. There may be other patents pending. ECLinPS MAX is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.