## General Description

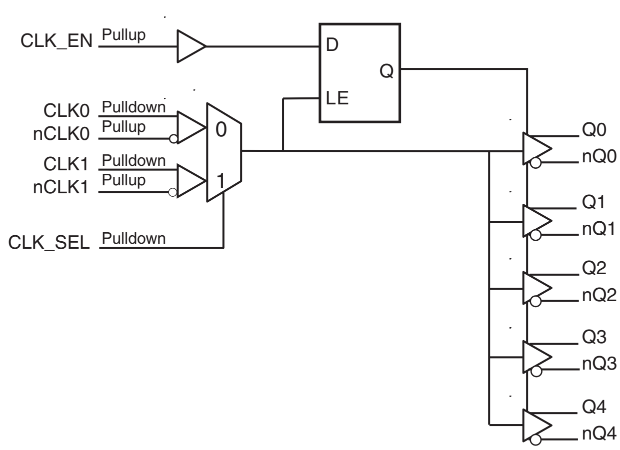
The 85304-01 is a low skew, high performance 1-to-5 Differential-to-3.3V LVPECL fanout buffer. The 85304-01 has two selectable clock inputs. The CLKx, nCLKx pairs can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt clock pulses on the outputs during asynchronous assertion/ deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 85304-01 ideal for those applications demanding well defined performance and repeatability.

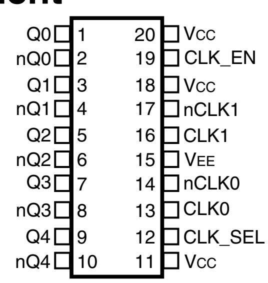
## Features

- Five 3.3V differential LVPECL output pairs
- Selectable differential CLKx, nCLKx input pairs
- CLKx, nCLKx input pairs can accept the following differential levels: LVDS, LVPECL, LVHSTL, SSTL and HCSL levels
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLKx inputs
- Output skew: 35ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2.1ns (maximum)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature

## Block Diagram




## Pin Assignment




**85304-01**

**20-Lead TSSOP**
**6.5mm x 4.4mm x 0.925mm package body**
**G Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | Q0, nQ0 | Output | | Differential output pair. LVPECL interface levels. |
| 3, 4 | Q1, nQ1 | Output | | Differential output pair. LVPECL interface levels. |
| 5, 6 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |
| 7, 8 | Q3, nQ3 | Output | | Differential output pair. LVPECL interface levels. |
| 9, 10 | Q4, nQ4 | Output | | Differential output pair. LVPECL interface levels. |
| 11, 18, 20 | $V_{CC}$ | Power | | Power supply pins. |
| 12 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVTTL/LVCMOS interface levels. |
| 13 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 14 | nCLK0 | Input | Pullup | Inverting differential clock input. |
| 15 | $V_{EE}$ | Power | | Negative supply pin. |
| 16 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 17 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 19 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced LOW, nQx outputs are forced HIGH. LVTTL/LVCMOS interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |

# Function Tables

### Table 3A. Control Input Function Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **CLK_EN** | **CLK_SEL** | **Selected Source** | **Q0:Q4** | **nQ0:nQ4** |
| 0 | 0 | CLK0, nCLK0 | Disabled; LOW | Disabled; HIGH |
| 0 | 1 | CLK1, nCLK1 | Disabled; LOW | Disabled; HIGH |
| 1 | 0 | CLK0, nCLK0 | Enabled | Enabled |
| 1 | 1 | CLK1, nCLK1 | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLKx, nCLKx inputs as described in Table 3B.

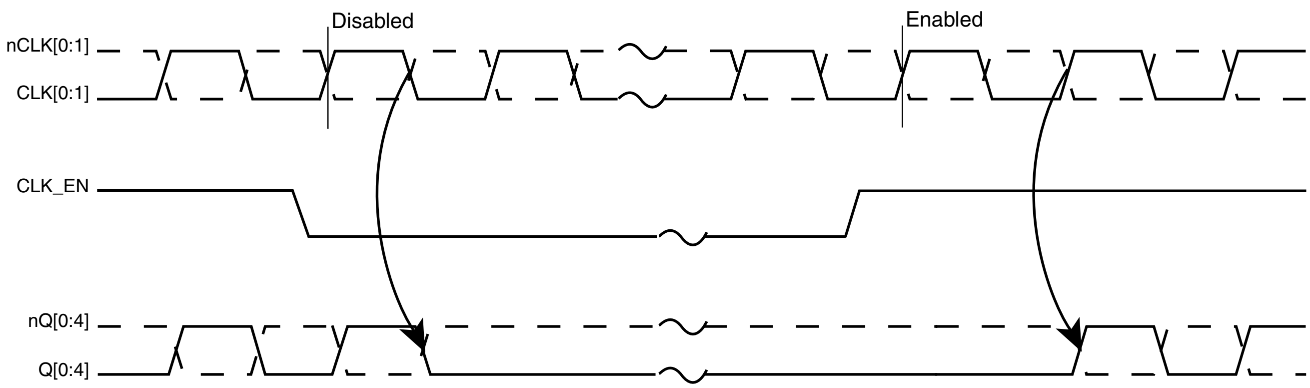



**Figure 1. CLK_EN Timing Diagram**

### Table 3B. Clock Input Function Table

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| **CLK0 or CLK1** | **nCLK0 or nCLK1** | **Q[0:4]** | **nQ[0:4]** | **Input to Output Mode** | **Polarity** |
| 0 | 1 | LOW | HIGH | Differential to Differential | Non-Inverting |
| 1 | 0 | HIGH | LOW | Differential to Differential | Non-Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | Single-Ended to Differential | Non-Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | Single-Ended to Differential | Non-Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | Single-Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | Single-Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information section, *Wiring the Differential Input to Accept Single-Ended Levels.*

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ =0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 55 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ =0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | 3.765 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK_EN | $V_{CC} = V_{IN}$ = 3.465V | | | 5 | µA |
| | | CLK_SEL | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK_EN | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | CLK_SEL | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ =0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | nCLK0, nCLK1 | $V_{CC} = V_{IN}$ = 3.465V | | | 5 | µA |
| | | CLK0, CLK1 | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | nCLK0, nCLK1 | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | CLK0, CLK1 | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 0.5 | | $V_{CC}$ – 0.85 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V
NOTE 2: Common mode input voltage is defined as $V_{IH}$.

**Table 4D. LVPECL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ =0V, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Current; NOTE 1 | | $V_{CC}$ – 1.4 | | $V_{CC}$ – 1.0 | µA |
| $V_{OL}$ | Output Low Current; NOTE 1 | | $V_{CC}$ – 2.0 | | $V_{CC}$ – 1.7 | µA |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 0.85 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$ – 2V.

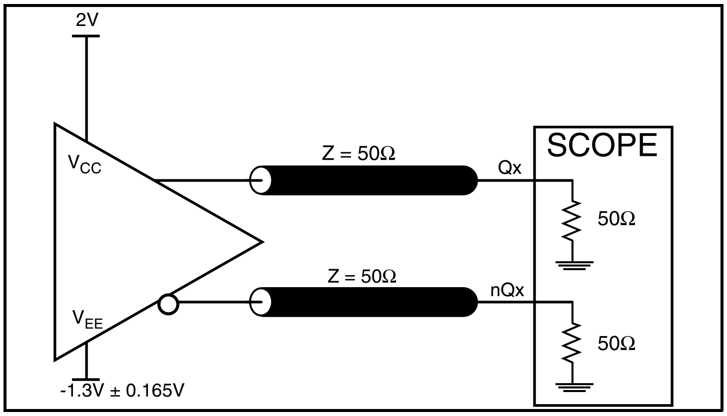
## AC Electrical Characteristics

**Table 5. AC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $V_{EE}$ =0V, $T_A$ = 0°C to 70°C

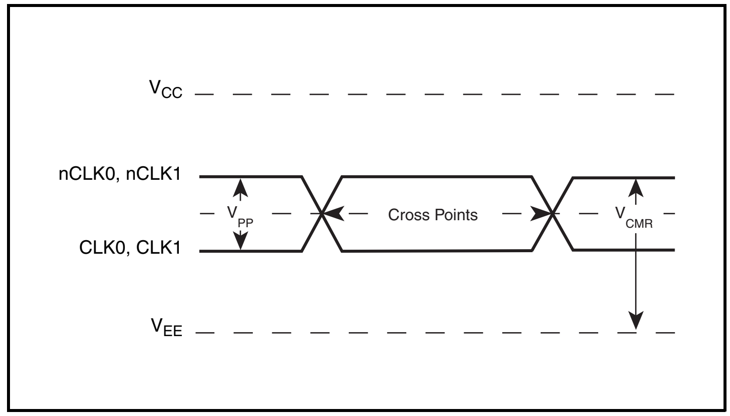
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | | 650 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | $f \leq$ 650MHz | 1.0 | | 2.1 | ns |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | | 35 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 150 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| odc | Output Duty Cycle | | 48 | 50 | 52 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 500MHz unless noted otherwise
NOTE: The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point. Measured at the output differential cross points.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

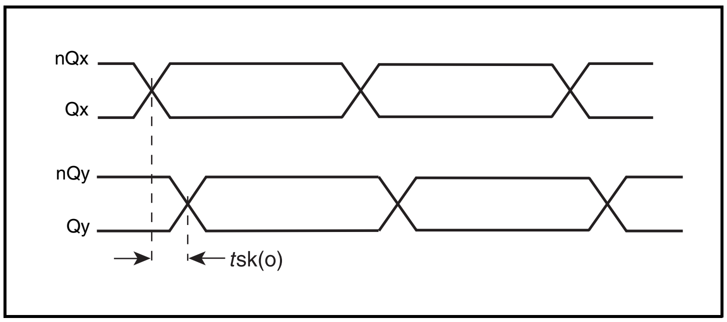
## Parameter Measurement Information



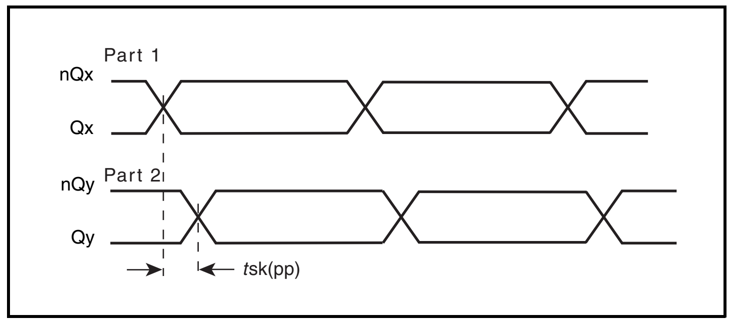

**3.3V Output Load Test Circuit**



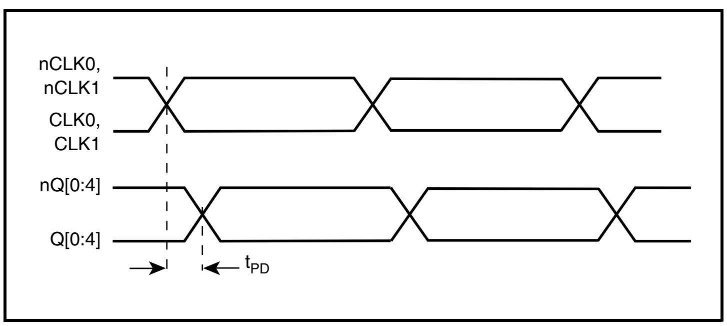

**Differential Input Level**



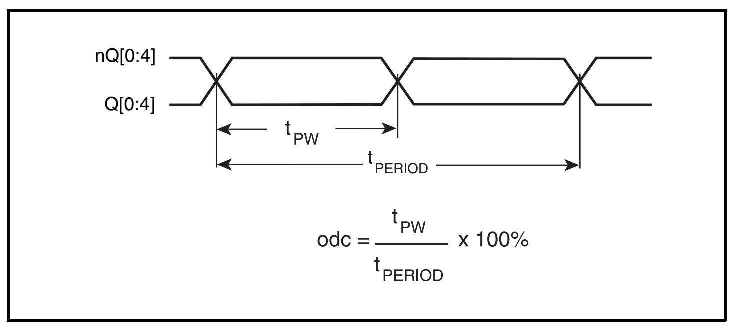

**Output Skew**



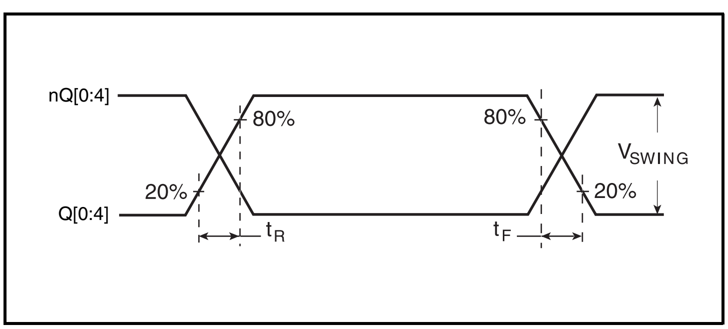

**Part-to-Part Skew**




**Output Duty Cycle/Pulse Width/Period**




**Output Duty Cycle/Pulse Width/Period**




**Output Rise/Fall Time**

# Applications Information

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

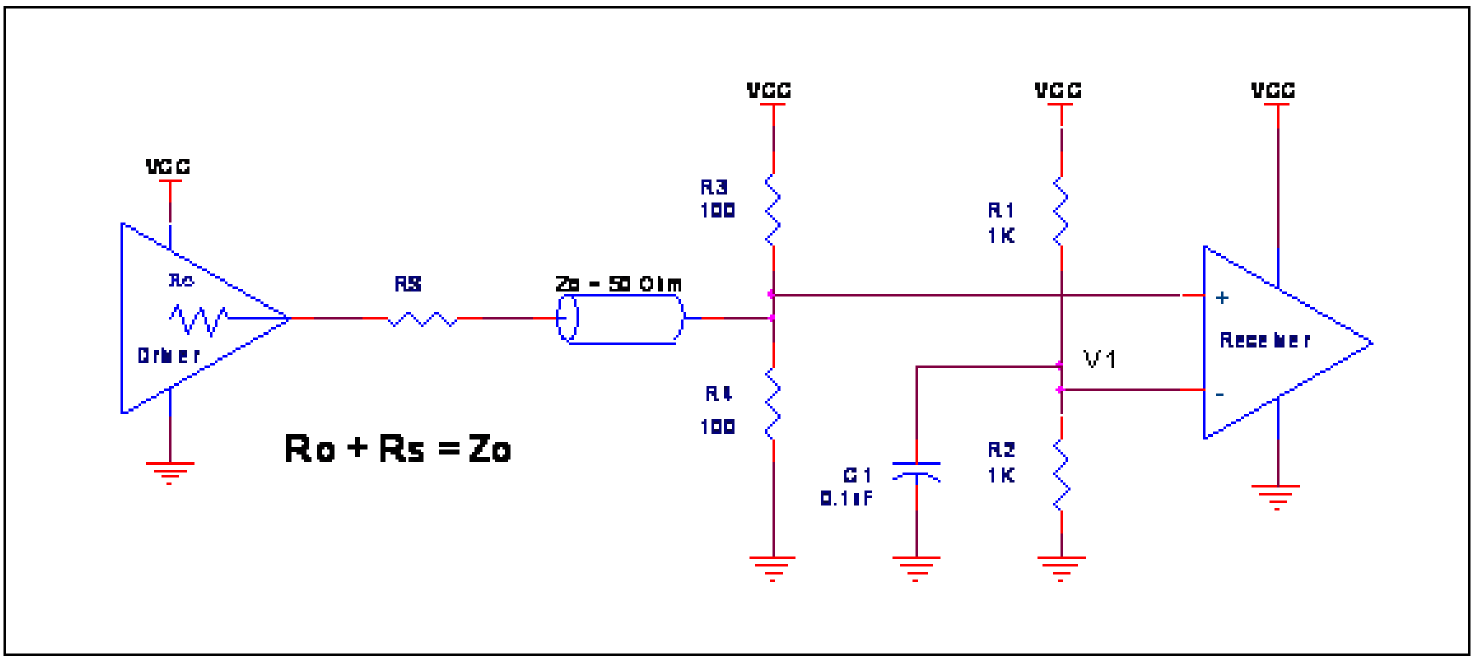



**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT's open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

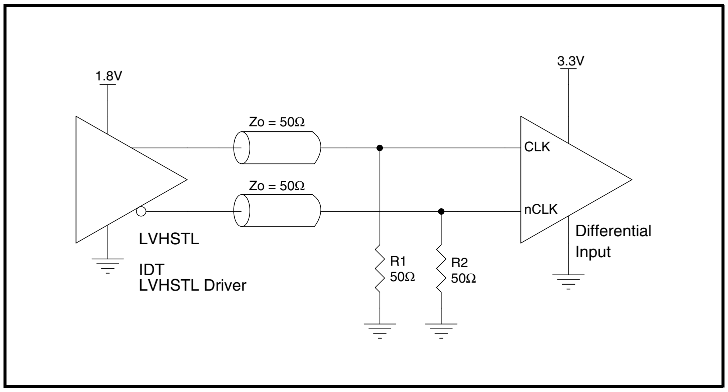



**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**

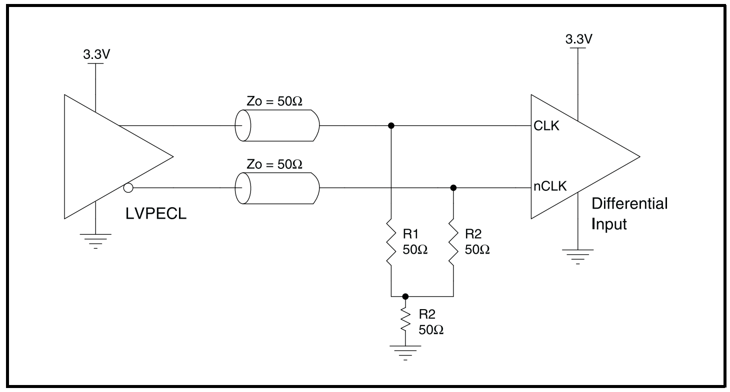



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

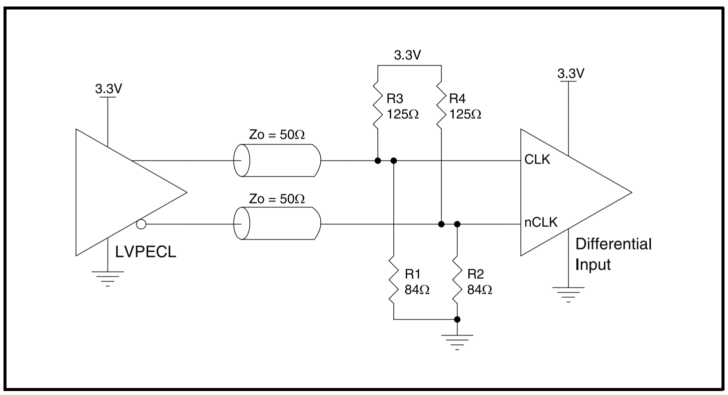



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

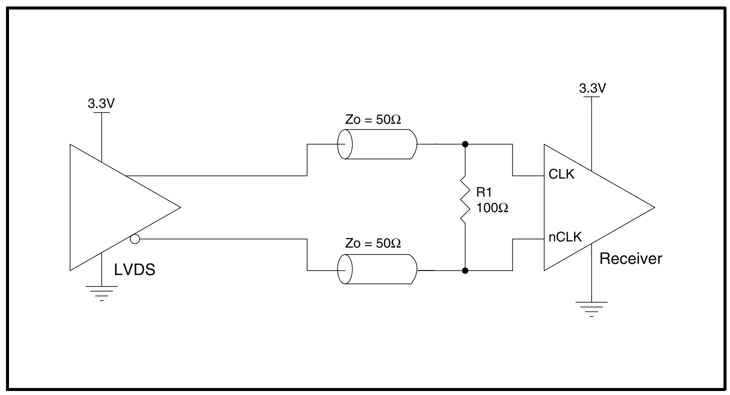



**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

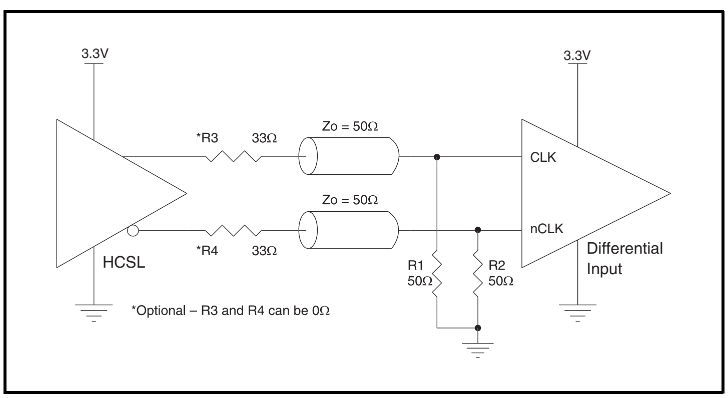



**Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

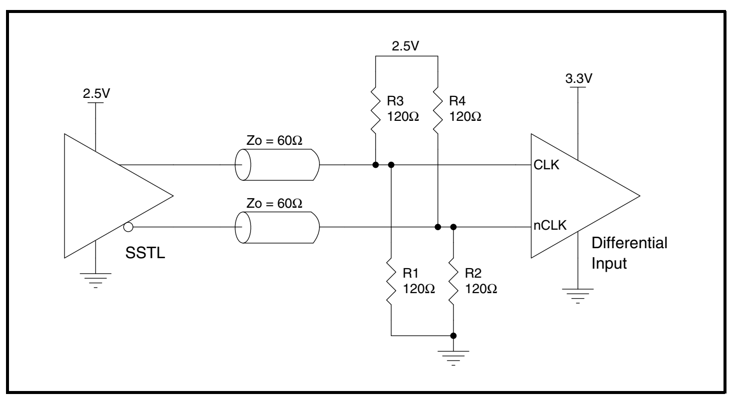



**Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullup or pulldown; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

### Outputs:

#### LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

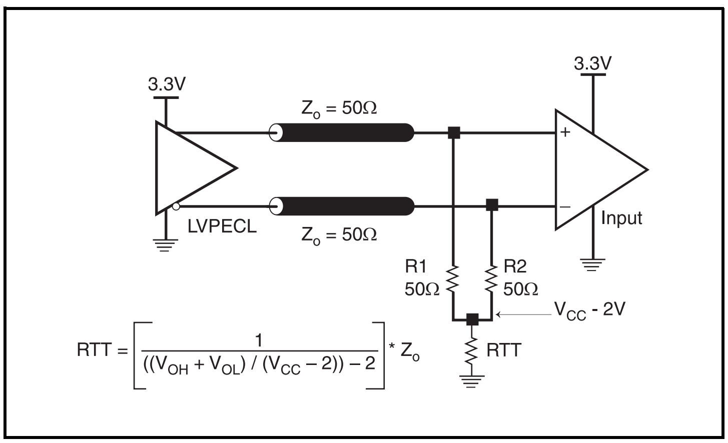



**Figure 3A. 3.3V LVPECL Output Termination**

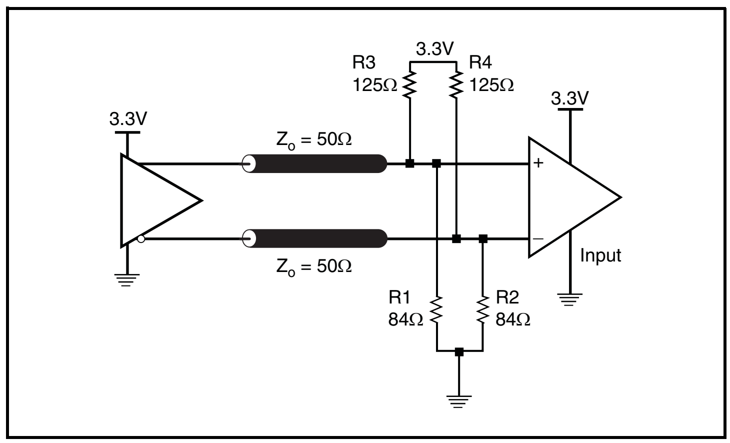



**Figure 3B. 3.3V LVPECL Output Termination**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 85304-01.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 85304-01 is the sum of the core power plus the output power dissipated due to loading.
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating output power dissipated due to loading.

- Power $(core)_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 55mA = **190.57mW**
- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 30.2mW = **151mW**

**Total Power**$_{\_MAX}$ (3.465V, with all outputs switching) = 190.57mW + 151mW = **341.57mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 73.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.342W * 73.2°C/W = 95°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

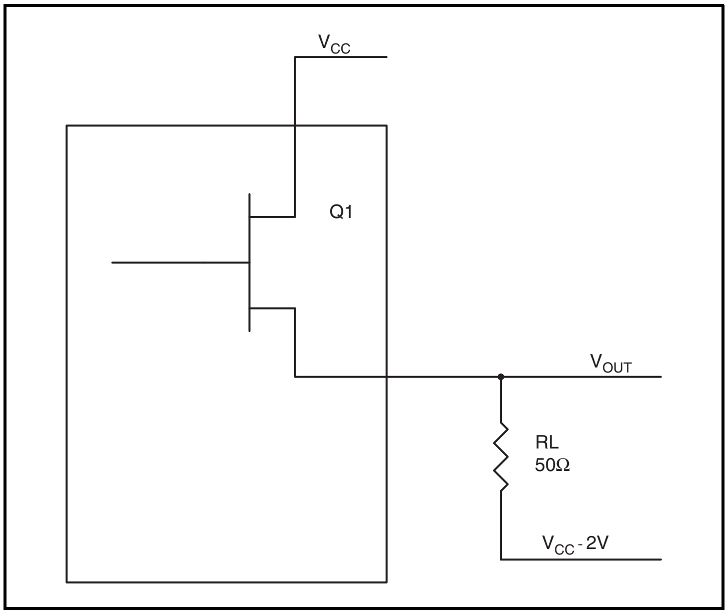



**Figure 4. LVPECL Driver Circuit and Termination**

To calculate output power dissipated due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 1.0V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{1.0V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 1.0V)/50\Omega] * 1.0V =$ **20mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

## Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

### Transistor Count

The transistor count for 85304-01 is: 489

## Package Outline and Package Dimensions

**Package Outline - G Suffix for 20 Lead TSSOP**

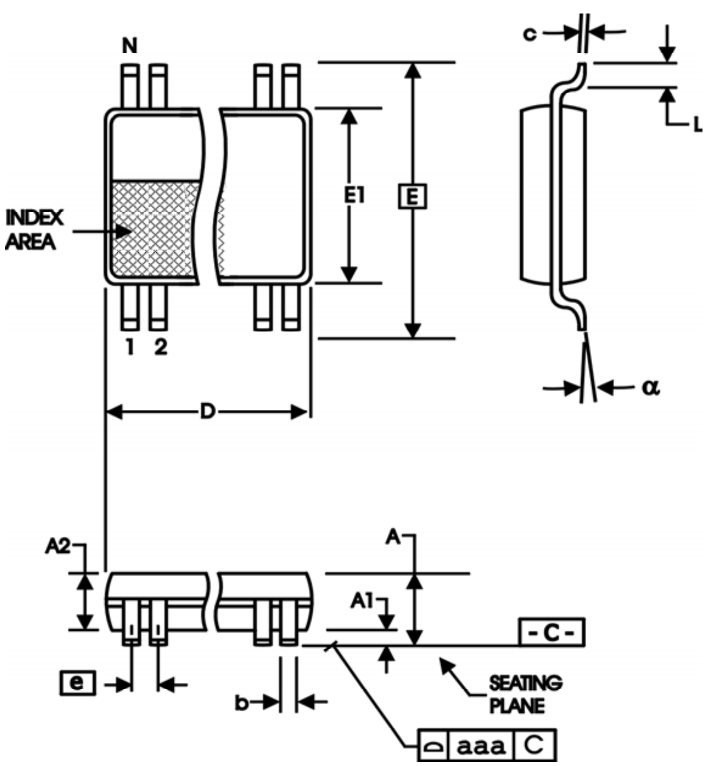



**Table 8. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| $\alpha$ | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 85304AG-01LF | ICS85304A01L | “Lead-Free” 20 Lead TSSOP | Tube | 0°C to 70°C |
| 85304AG-01LFT | ICS85304A01L | “Lead-Free” 20 Lead TSSOP | Tape & Reel | 0°C to 70°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | T4B<br>T4D<br>T5 | 4<br>5<br>5 | $V_{CMR}$ values changed from 1.5V min. to 0.5V min.; $V_{DD}$ max. to $V_{CC}$ - 0.85V max.<br>$V_{OH}$ values changed from 1.9µA min. to $V_{CC}$ - 1.4µA min.; 2.3µA max. to $V_{CC}$ - 1.0µA.<br>$V_{OL}$ values changed from 1.2µA min. to $V_{CC}$ - 2.0µA; 1.6µA max. to $V_{CC}$ - 1.7µA max.<br>Replaced $tp_{LH}$ and $tp_{HL}$ with $t_{PD}$ at the same values.<br>Replaced $t_{PW}$ and values of $t_{CYCLE}$/2 - 40 min., $t_{CYCLE}$/2 typ., $t_{CYCLE}$/2 + 40 max. with odc at values of 48% min., 50% typ., 52% max. | 5/14/01 |
| B | T4D<br>T5 | 5 | LVPECL DC Characteristics Table - added $I_{IH}$, $I_{IL}$, $V_{PP}$, and $V_{CMR}$ rows.<br>AC Characteristics Table - $t_R$ and $t_F$ values changed from 275ps min to 300ps min; 650ps max. to 700ps max. | 5/22/01 |
| C | T4D | 5 | Differential DC Characteristics Table - $V_{CMR}$ values changed from $V_{CC}$ - 0.85V max. to $V_{CC.}$ | 8/21/01 |
| C | | 3 | Revised Figure 1, CLK_EN Timing Diagram. | 10/17/01 |
| C | | 3 | Revised Figure 1, CLK_EN Timing Diagram. | 11/2/01 |
| C | T3B | 3 | Revised Inputs heading from CLK or CLK, nPCLK or nPCLK to CLK or PCLK, nCLK or nPCLK. | 12/28/01 |
| C | | 8 | Added *Termination for LVEPCL Output* section. | 5/30/02 |
| C | | 6<br><br>7 | 3.3V Output Load Test Circuit Diagram - corrected $V_{EE}$ = -1.3V ± 0.135V to $V_{EE}$ = -1.3V ± 0.165V.<br>Updated Output Rise/Fall Time Diagram. | 8/26/02 |
| D | <br>T2<br><br><br><br><br>T9 | 1<br>2<br>4<br>6<br>8<br>9<br>14 | Added Lead-Free bullet in Features section.<br>Pin Characteristics table - changed $C_{IN}$ 4pF max. to 4pF typical.<br>Absolute Maximum Ratings, updated Outputs rating.<br>Updated Parameter Measurement Information.<br>Added *Differential Clock Input Interface* section.<br>Added *LVPECL Clock Input Interface* section.<br>Ordering Information table - added Lead Free part number. | 6/17/04 |
| E | <br><br><br><br><br><br>T9 | <br><br>8<br><br>9<br>10<br>13 | Per Document Errata, NEN-08-03, corrected name of PCLK/nPCLK to CLK1/nCLK1 and changed CLK/nCLK to CLK0/nCLK0 throughout the datasheet.<br>Updated *Differential Clock Input Interface* section.<br>Deleted *LVPECL Clock Input Interface* section.<br>Added *Recommendations for Unused Input and Output Pins* section.<br>Power Considerations - corrected Junction Temperature calculations.<br>Ordering Information Table - corrected marking.<br>Updated format throughout the datasheet. | 6/20/08 |
| E | | 3 | Corrected Figure 1, CLK_EN Timing Diagram. | 7/8/08 |
| E | <br>T4[A:D]<br><br>T5<br><br><br>T9 | 1<br>4 - 5<br><br>5<br><br>7<br>13 | Features section - deleted package information<br>DC Characteristic Tables - corrected table heading temperature from -40°C to 85°C to 0°C to 70°C.<br>AC Characteristic Table - corrected table heading temperature from -40°C to 85°C to 0°C to 70°C. Added general note to table.<br>Updated *Wiring the Differential Input to Accept Single-ended Levels* application note.<br>Ordering Information Table - deleted non lead-free parts. Deleted Tape & Reel quantity from Shipping Packaging column. | 12/19/12 |
| E | | | Updated Header and Footer format. | 12/2/15 |

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