# 阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任
 何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无
 法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获
 得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描
 叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有"数据手册"字样。

# Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets".

## General Description

The ICS8543 is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8543 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8543 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8543 ideal for those applications demanding well defined performance and repeatability.

## Features

- Four differential LVDS output pairs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequency: 800MHz
- Translates any single-ended input signals to LVDS levels with resistor bias on nCLK input
- Additive phase jitter, RMS: 0.164ps (typical)
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 2.6ns (maximum)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram
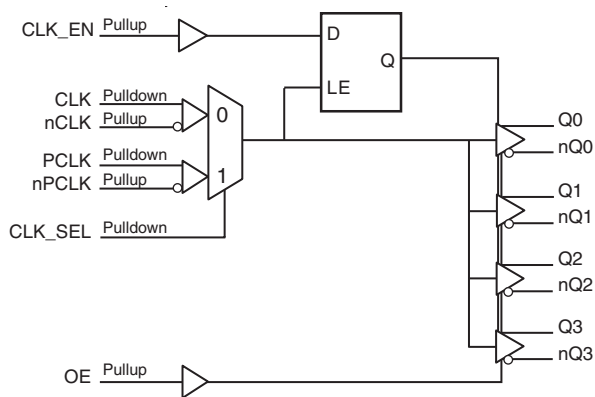


## Pin Assignment



**ICS8543**

**20-Lead TSSOP**

**6.5mm x 4.4mm x 0.925mm package body**

**G Package**

**Top View**

# Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 9, 13 | GND | Power | | Power supply ground. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS / LVTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels. |
| 4 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 5 | nCLK | Input | Pullup | Inverting differential clock input. |
| 6 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 7 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 8 | OE | Input | Pullup | Output enable. Controls enabling and disabling of outputs Q[0:3], nQ[0:3]. LVCMOS/LVTTL interface levels. |
| 10, 18 | $V_{DD}$ | Power | | Positive supply pins. |
| 11, 12 | nQ3, Q3 | Output | | Differential output pair. LVDS interface levels. |
| 14, 15 | nQ2, Q2 | Output | | Differential output pair. LVDS interface levels. |
| 16, 17 | nQ1, Q1 | Output | | Differential output pair. LVDS interface levels. |
| 19, 20 | nQ0, Q0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

# Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | k$\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k$\Omega$ |

# Function Tables

**Table 3A. Control Input Function Table**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| **OE** | **CLK_EN** | **CLK_SEL** | **Selected Source** | **Q[0:3]** | **nQ[0:3]** |
| 0 | X | X | | Hi-Z | Hi-Z |
| 1 | 0 | 0 | CLK, nCLK | Disabled; Low | Disabled; High |
| 1 | 0 | 1 | PCLK, nPCLK | Disabled; Low | Disabled; High |
| 1 | 1 | 0 | CLK, nCLK | Enabled | Enabled |
| 1 | 1 | 1 | PCLK, nPCLK | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK/nCLK and PCLK/nPCLK inputs as described in Table 3B.
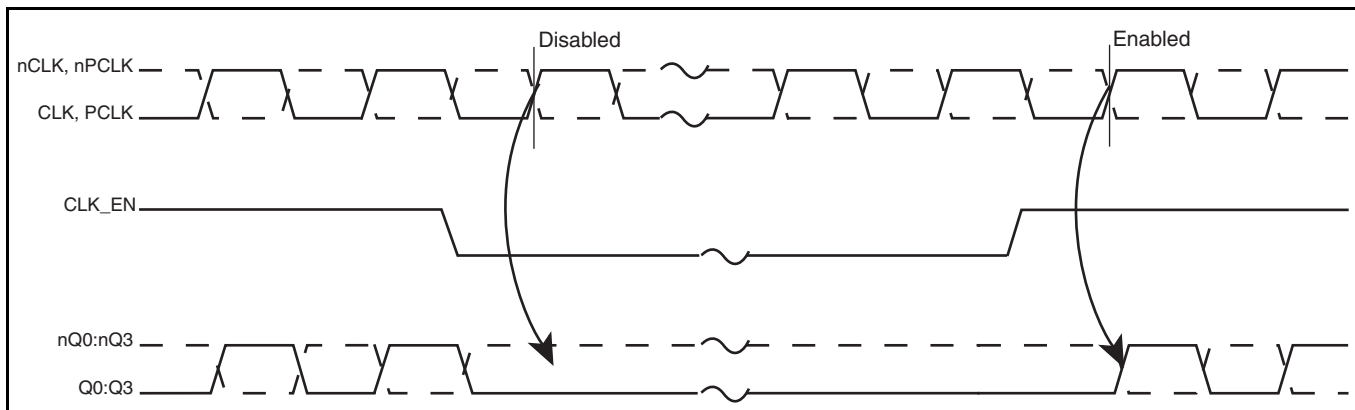


**Figure 1. CLK_EN Timing Diagram**

**Table 3B. Clock Input Function Table**

| Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| **CLK or PCLK** | **nCLK or nPCLK** | **Q[0:3]** | **nQ[0:3]** | **Input to Output Mode** | **Polarity** |
| 0 | 1 | LOW | HIGH | Differential to Differential | Non-Inverting |
| 1 | 0 | HIGH | LOW | Differential to Differential | Non-Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | Single-Ended to Differential | Non-Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | Single-Ended to Differential | Non-Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | Single-Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | Single-Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information section, *Wiring the Differential Input to Accept Single-Ended Levels.*

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.
These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond
those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$<br>Continuos Current<br>Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 50 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | 3.765 | V |
| $V_{IL}$ | Input Low Voltage | | | | | 0.8 | V |
| $I_{IH}$ | Input High Current | OE, CLK_EN | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| | | CLK_SEL | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | OE, CLK_EN | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | CLK_SEL | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | nCLK | $V_{DD} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | | µA |
| | | nCLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as $V_{IH}$.

**Table 4D. LVPECL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | nPCLK | $V_{DD} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | | µA |
| | | nPCLK | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage | | | 0.3 | | 1.0 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1 | | | 1.5 | | $V_{DD}$ | V |

NOTE 1: Common mode input voltage is defined as $V_{IH}$.

**Table 4E. LVDS DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 200 | 280 | 360 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | 0 | 40 | mV |
| $V_{OS}$ | Offset Voltage | | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | 5 | 25 | mV |
| $I_{Oz}$ | High Impedance Leakage | | -10 | | +10 | µA |
| $I_{OFF}$ | Power Off Leakage | | -20 | ±1 | +20 | µA |
| $I_{OSD}$ | Differential Output Short Circuit Current | | | -3.5 | -5 | mA |
| $I_{OS}$ | Output Short Circuit Current | | | -3.5 | -5 | mA |
| $V_{OH}$ | Output Voltage High | | | 1.34 | 1.6 | V |
| $V_{OL}$ | Output Voltage Low | | 0.9 | 1.06 | | V |

# AC Electrical Characteristics

**Table 5. AC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Output Frequency | | | | | 800 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | | $f \leq$ 800MHz | 1.7 | | 2.6 | ns |
| $t$jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | | 153.6MHz, Integration Range: 12kHz – 20MHz | | 0.164 | | ps |
| $t$sk(o) | Output Skew; NOTE 2, 4 | | | | | 40 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | | 500 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% to 80% @ 50MHz | 150 | | 350 | ps |
| odc | Output Duty Cycle | odc | | 45 | 50 | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential output cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

# Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.
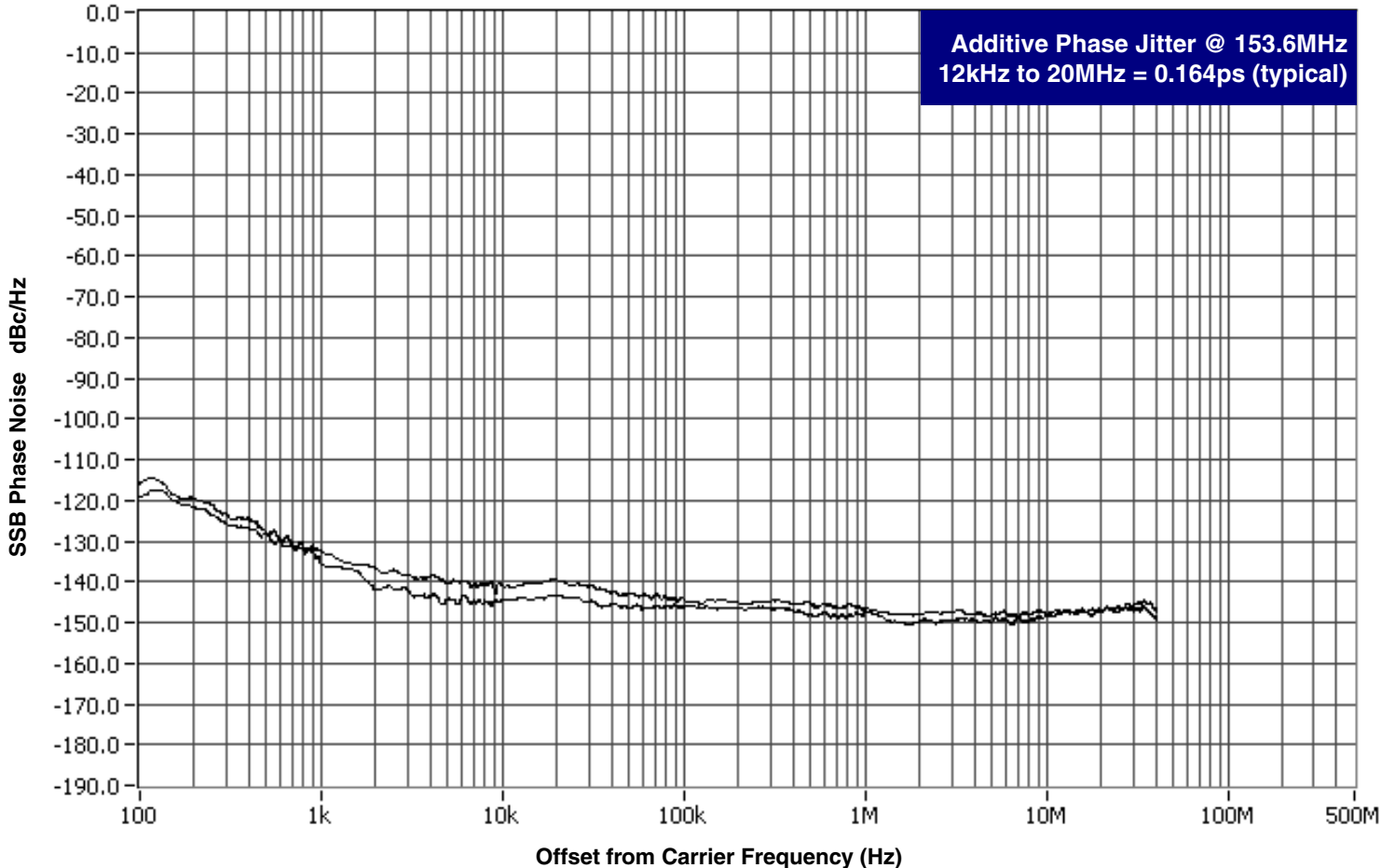


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This

is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

# Parameter Measurement Information
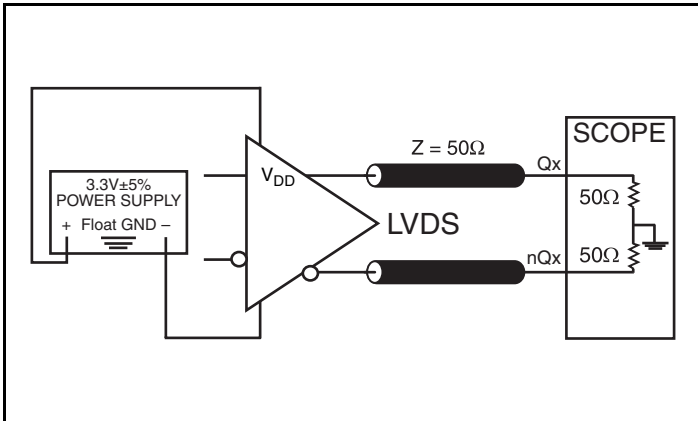


**3.3V LVDS Output Load AC Test Circuit**
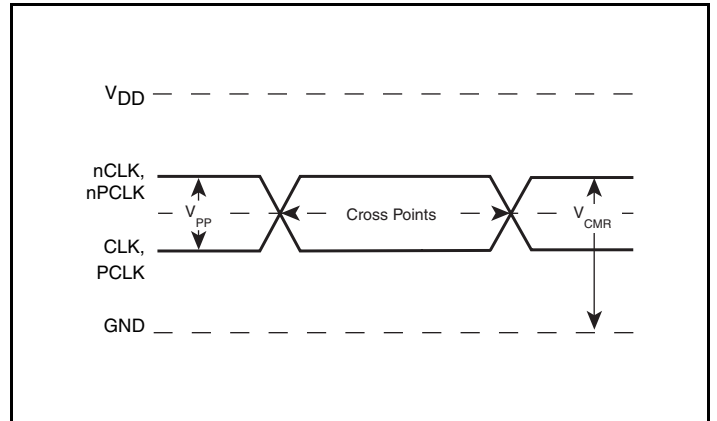


**Differential Input Level**
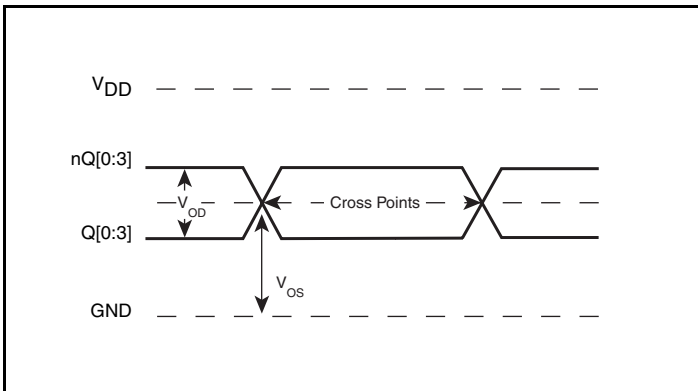


**Differential Output Level**
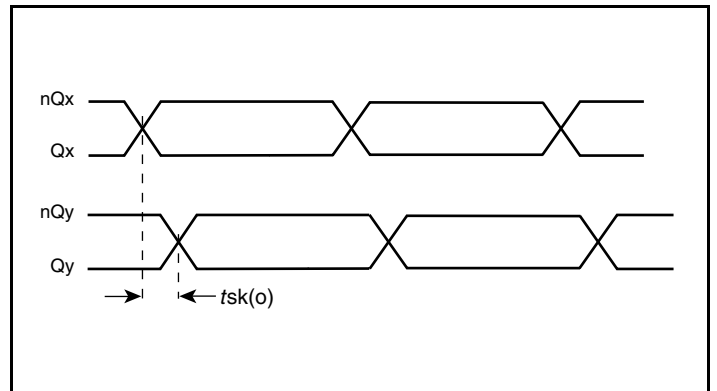


**Output Skew**
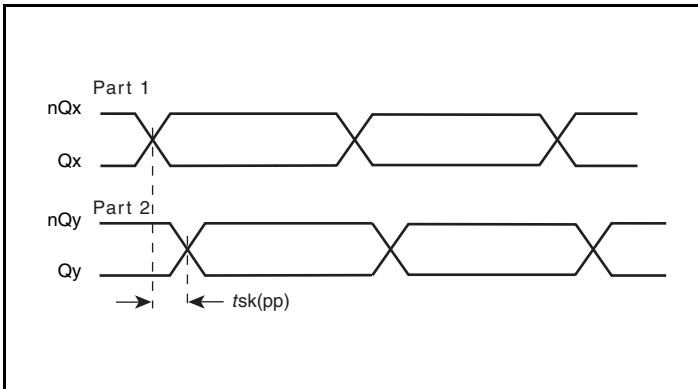


**Part-to-Part Skew**
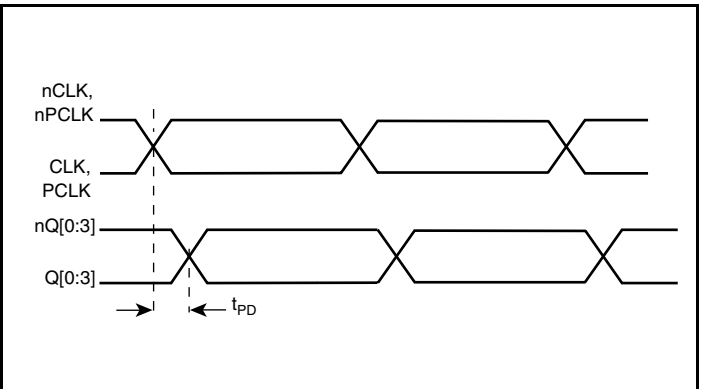


**Propagation Delay**

# Parameter Measurement Information, continued
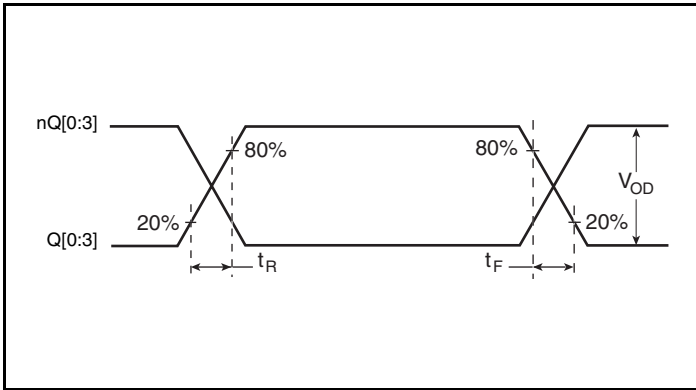


**Output Rise/Fall Time**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
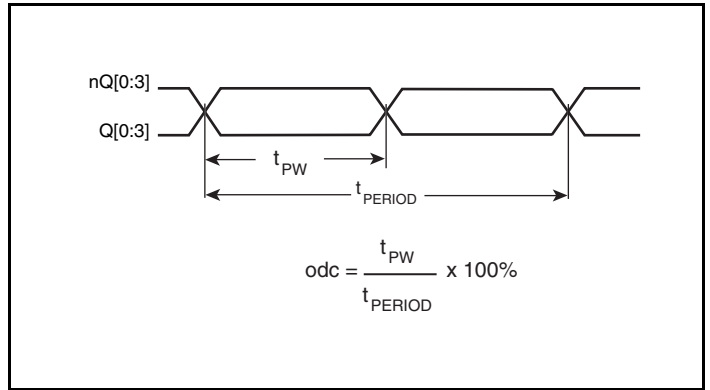
**Output Duty Cycle/Pulse Width/Period**
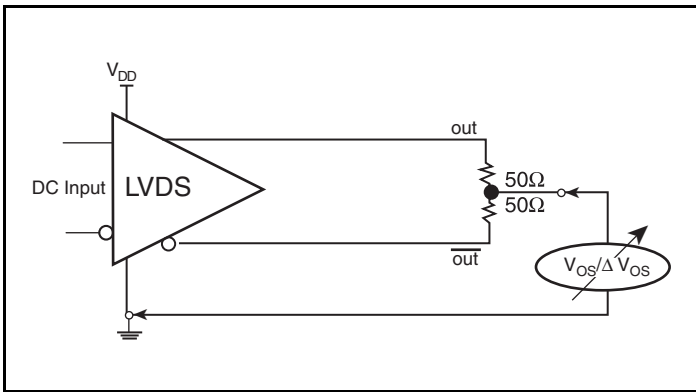


**Offset Voltage Setup**
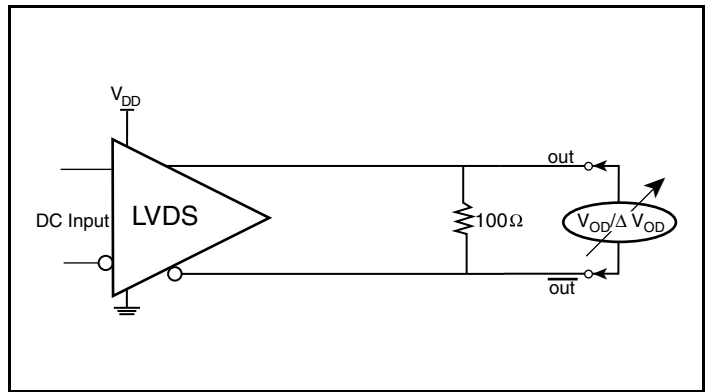


**Differential Output Voltage Setup**
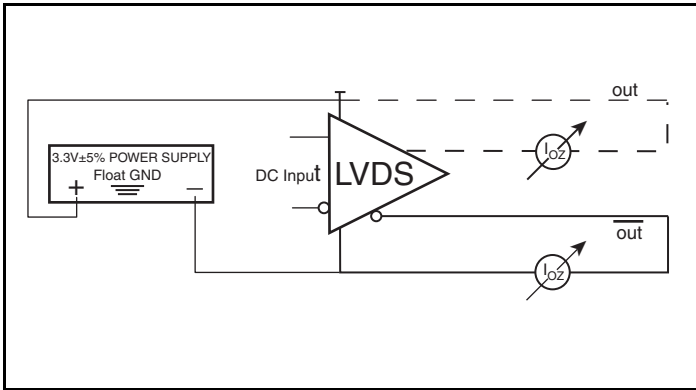


**High Impedance Leakage Current Setup**
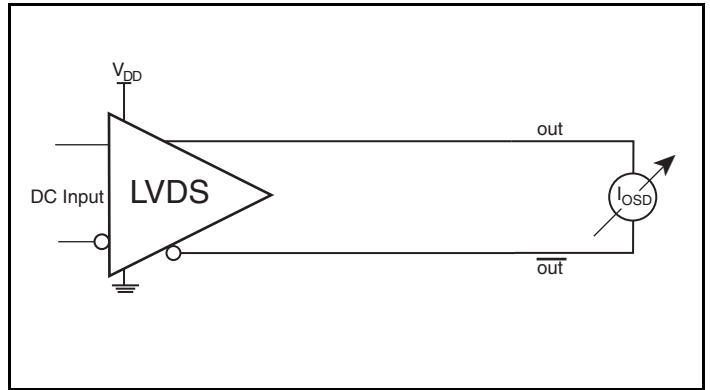


**Differential Output Short Circuit Setup**

9

## Parameter Measurement Information, continued
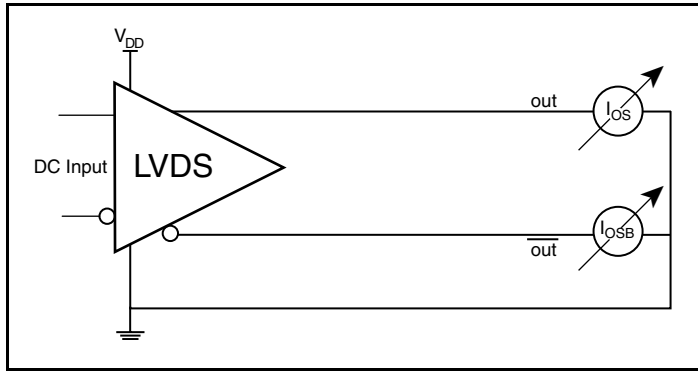


**Output Short Circuit Current Setup**
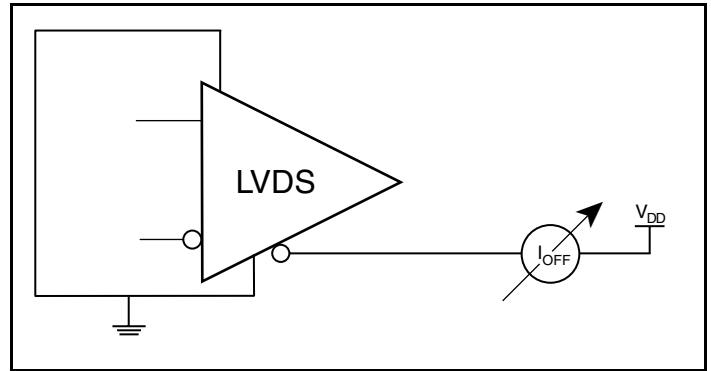


**Power Off Leakage Setup**

## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

*Figure 2* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_{REF}$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD}$ = 3.3V, R1 and R2 value should be adjusted to set $V_{REF}$ at 1.25V. The values below are for when both the single ended swing and $V_{DD}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50$\Omega$ applications, R3 and R4 can be 100$\Omega$. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{DD}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.
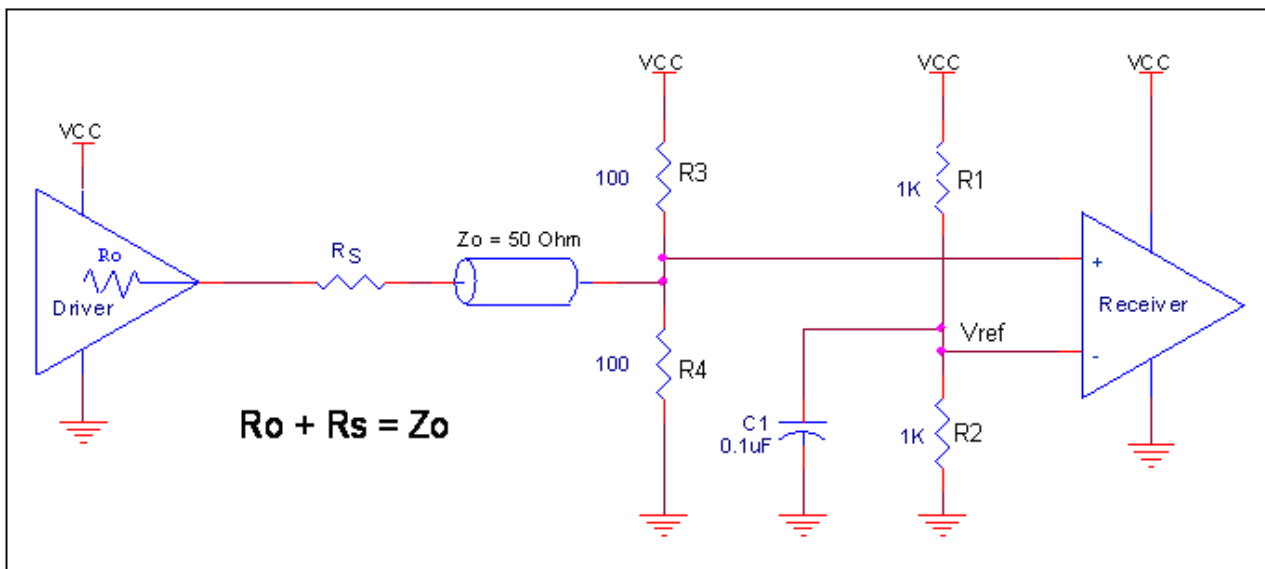


**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.
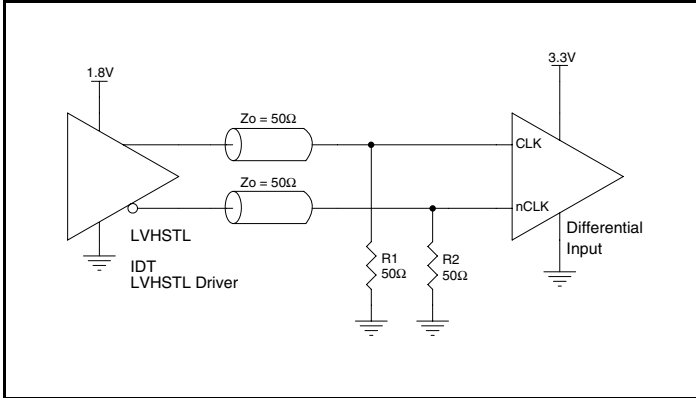


**Figure 3A.  CLK/nCLK Input Driven by an
IDT Open Emitter LVHSTL Driver**
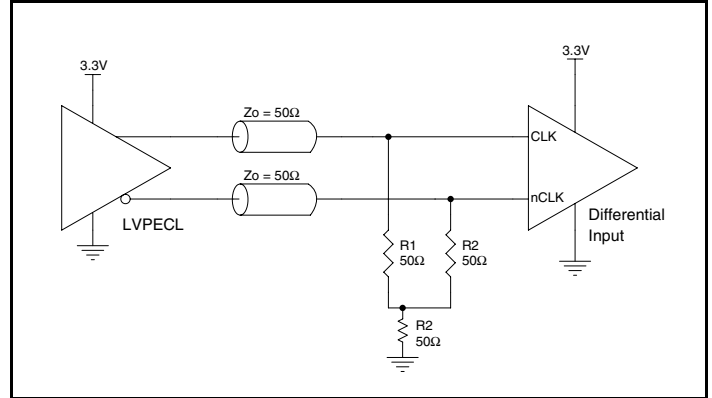


**Figure 3B.  CLK/nCLK Input Driven by a
3.3V LVPECL Driver**
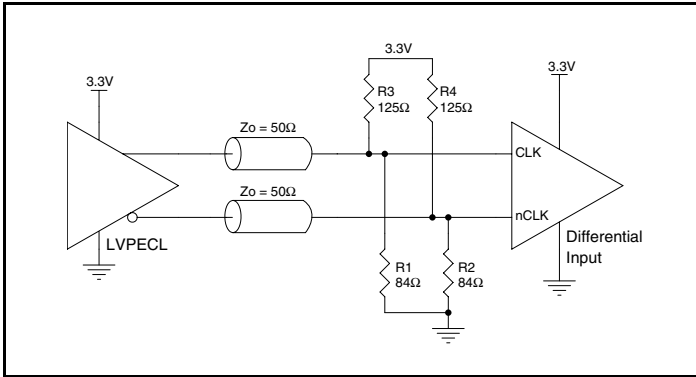


**Figure 3C.  CLK/nCLK Input Driven by a
3.3V LVPECL Driver**
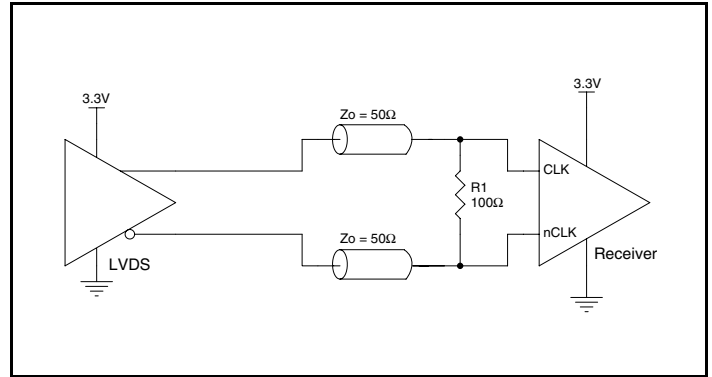


**Figure 3D.  CLK/nCLK Input Driven by a 3.3V LVDS Driver**
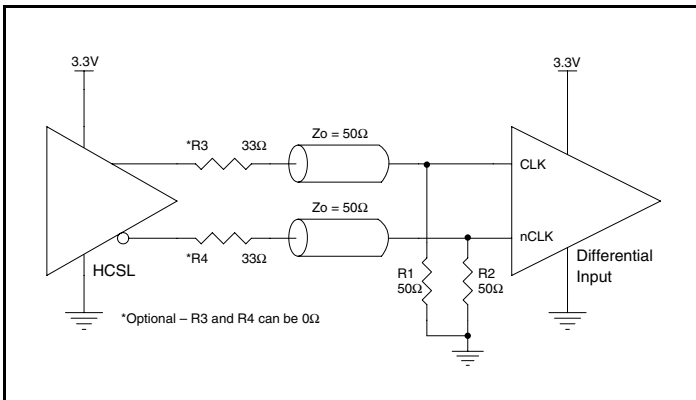


**Figure 3E.  CLK/nCLK Input Driven by a
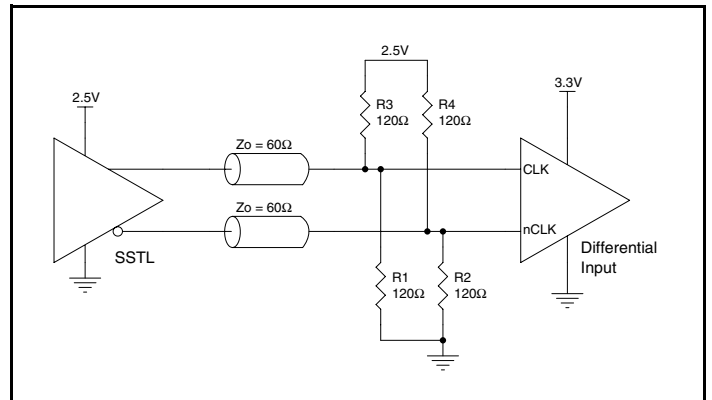3.3V HCSL Driver**



**Figure 3F.  CLK/nCLK Input Driven by a 2.5V SSTL Driver**

11

## 3.3V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 4A to 4E* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.
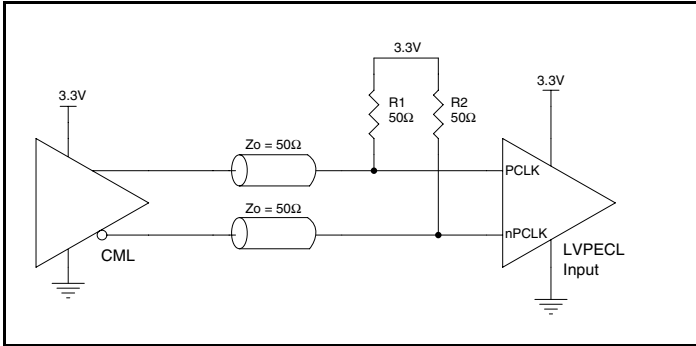


**Figure 4A.  PCLK/nPCLK Input Driven by a CML Driver**
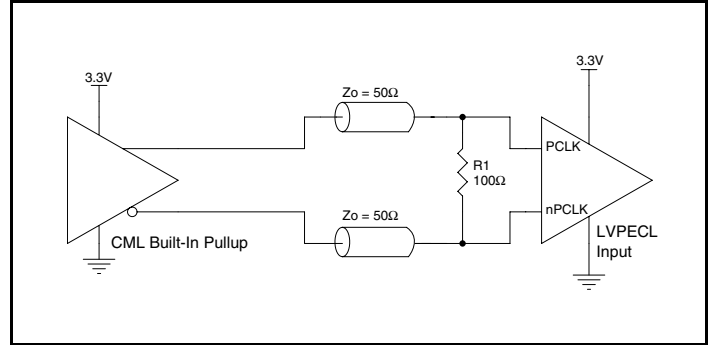


**Figure 4B.  PCLK/nPCLK Input Driven by a
Built-In Pullup CML Driver**
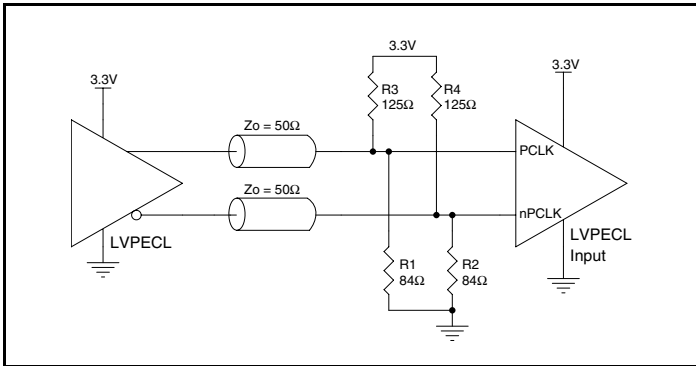


**Figure 4C.  PCLK/nPCLK Input Driven by a
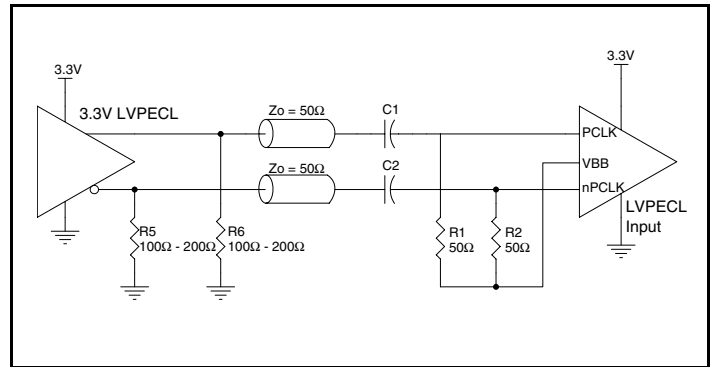3.3V LVPECL Driver**



**Figure 4D.  PCLK/nPCLK Input Driven by a
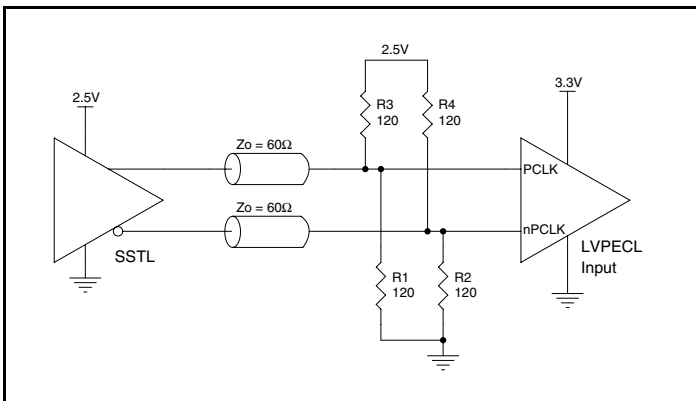3.3V LVPECL Driver with AC Couple**



**Figure 4E.  PCLK/nPCLK Input Driven by a
2.5V SSTL Driver**

# Recommendations for Unused Input and Output Pins

## Inputs:

### CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

### PCLK/nPCLK INPUTS

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

## Outputs:

### LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

# LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 5 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.
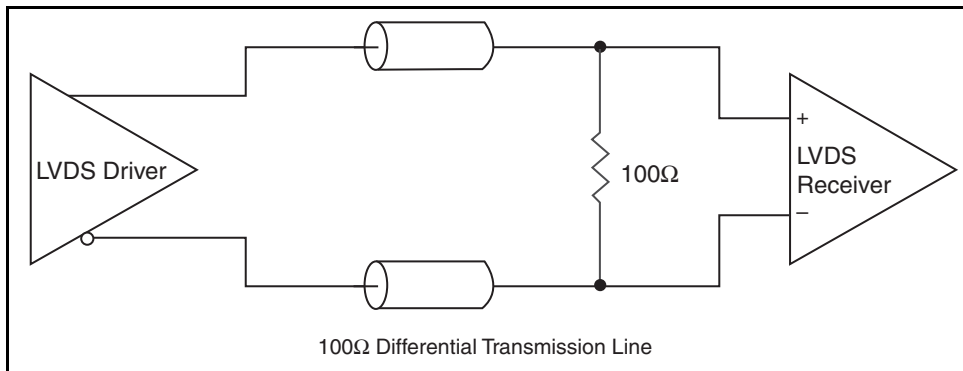


**Figure 5. Typical LVDS Driver Termination**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8543.
Equations and example calculations are also provided.

1. **Power Dissipation.**

The total power dissipation for the ICS8543 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX}$ = $V_{DD\_MAX}$ * $I_{DD\_MAX}$ = 3.465V * 50mA = **173.25mW**

2. **Junction Temperature.**

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 73.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.173W * 73.2°C/W = 82.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resitance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP**

| $\theta_{JA}$ **by Velocity** | | | |
|---|---|---|---|
| Linear Feet per Minute | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

# Transistor Count

The transistor count for ICS8543 is: 636

# Package Outline and Package Dimensions

**Package Outline - G Suffix for 20 Lead TSSOP**
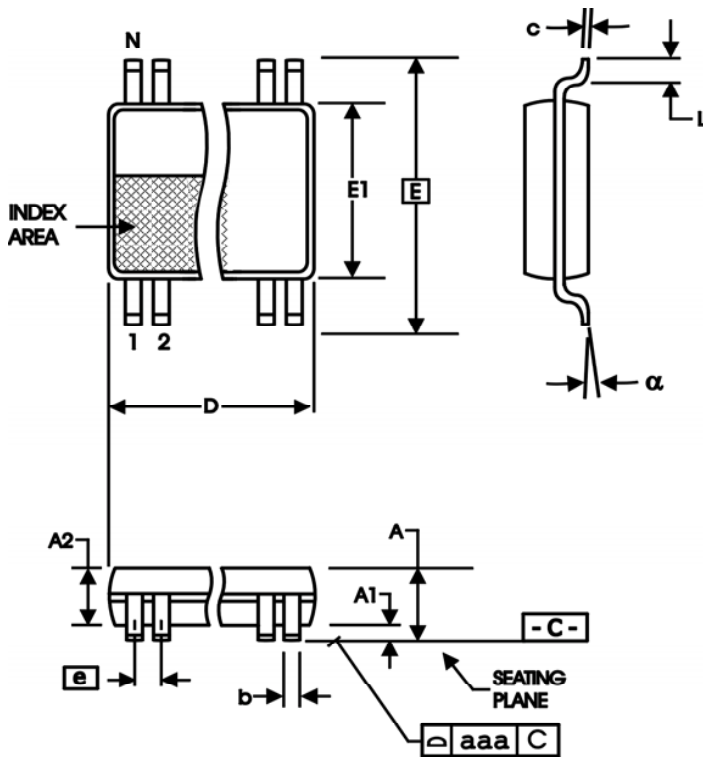


**Table 8. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| $\alpha$ | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8543BG | ICS8543BG | 20 Lead TSSOP | Tube | 0°C to 70°C |
| 8543BGT | ICS8543BG | 20 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |
| 8543BGLF | ICS8543BGLF | "Lead-Free" 20 Lead TSSOP | Tube | 0°C to 70°C |
| 8543BGLFT | ICS8543BGLF | "Lead-Free" 20 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | T4E | 5 | In the $V_{OL}$ row, 1.06 has been moved to the Typical column from the maximum column. | 9/18/01 |
| A | | 3 | Updated Figure 1, CLK_EN Timing Diagram. | 10/17/01 |
| A | | 3 | Updated Figure 1, CLK_EN Timing Diagram. | 11/2/01 |
| A | | 1<br>6 - 10 | Features section, Bullet 6 to read 3.3V LVDS levels instead of LVPECL.<br>Updated Parameter Measurement Information figures. | 5/6/02 |
| B | T5 | 5 | AC Characteristics table - revised Output Frequency from 650MHz to 800MHz. | 6/5/02 |
| C | <br>4E | 1<br><br>5 | Features - deleted bullet "Designed to meet or exceed the requirements of ANSI TIA/EIA-644".<br>LVDS Table - changed $V_{OD}$ typical value from 350mV to 280mV. | 9/19/02 |
| D | T2 | 2<br>4<br>9<br>10<br>11 | Pin Characteristics - changed $C_{IN}$ 4pF max. to 4pF typical.<br>Absolute Maximum Ratings - changed Output rating.<br>Added Differential Clock Input Interface section.<br>Added *LVPECL Clock Input Interface* section.<br>Added *LVDS Driver Termination* section.<br>Updated format throughout data sheet. | 12/31/03 |
| D | T1 | 2 | Pin Description table - added function description to the OE pin. | 4/7/04 |
| D | T8 | 10<br>13 | Updated *LVPECL Clock Input Interface* section.<br>Added Lead Free part number to Ordering Information table. | 6/16/04 |
| D | | 3<br>10<br>11<br>12<br>13 | Updated Figure 1, CLK_EN Timing Diagram.<br>Updated *Differential Clock Input Interface* section.<br>Updated *LVPECL Clock Input Interface* section.<br>Added *Recommendation for Unused Input and Output Pins* section.<br>Added *Power Considerations* section.<br>Updated format throughout the datasheet. | 2/27/08 |
| E | <br>T5<br><br><br><br><br><br><br>T9 | 1<br>6<br>7<br>10<br>11<br>12<br>13<br>16 | Features section - added Additive Phase Jitter bullet.<br>AC Characteristics Table - added Added Phase Jitter spec and thermal note.<br>Added Additive Phase Jitter plot.<br>Updated *Wiring the Differential Input to Accept Single-ended Levels* section.<br>Updated *3.3V Differential Clock Input Interface* section.<br>Updated *3.3V LVPECL Clock Input Interface* section.<br>Updated *LVDS Driver Termination* section.<br>Ordering Information Table - deleted "ICS" prefix from Part/Order Number column.<br>Updated datasheet header/footer style. | 11/12/10 |
| E | | 1<br>14 | Page 1, corrected Header Title.<br>Power Considerations - corrected typo for junction temperature from 827.7°C to 82.7°C. | 12/17/10 |

# We've Got Your Timing Solution

**IDT**
www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

**Technical Support**
netcom@idt.com
+480-763-2056