

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

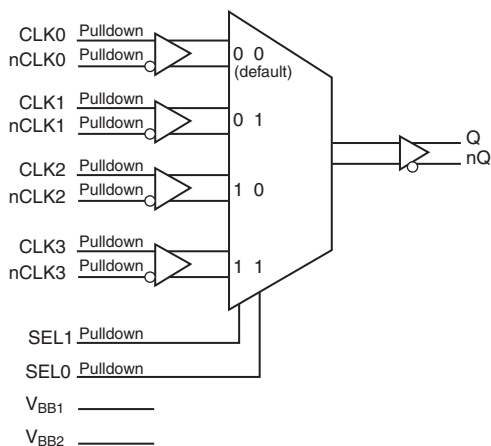
### General Description

The ICS853S0571 is a 4:1 Differential-to-3.3V or 2.5V LVPECL/ECL Clock/Data Multiplexer which can operate up to 3GHz. The ICS853S0571 has 4 differential selectable clock input pairs. The CLK, nCLK input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The multiplexer select control inputs have ECL/LVPECL interface levels. The select pins have internal pulldown resistors.

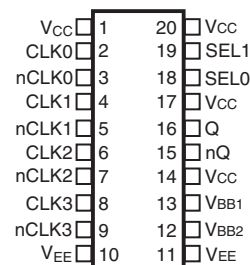
### Features

- High speed 4:1 differential multiplexer
- One differential 3.3V, 2.5V LVPECL/ECL output
- Four differential CLKx, nCLKx input pairs
- Differential CLKx, nCLKx pairs can accept the following interface levels: LVPECL, LVDS, CML, SSTL
- Maximum input/output frequency: 3GHz
- Additive phase jitter, RMS @ 622.08MHz: 0.073ps (typical)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 615ps (maximum)
- LVPECL mode operating voltage supply range:  $V_{CC} = 2.375V$  to  $3.465V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  $V_{CC} = 0V$ ,  $V_{EE} = -3.465V$  to  $-2.375V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Available in lead-free (RoHS 6) packages

### Block Diagram



### Pin Assignment



**ICS853S0571**  
**20-Lead TSSOP**  
**6.5mm x 4.4mm x 0.925mm**  
**package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 14, 17, 20	V <sub>CC</sub>	Power		Positive supply pins.
2	CLK0	Input	Pulldown	Non-inverting differential clock input.
3	nCLK0	Input	Pulldown	Inverting differential clock input.
4	CLK1	Input	Pulldown	Non-inverting differential clock input.
5	nCLK1	Input	Pulldown	Inverting differential clock input.
6	CLK2	Input	Pulldown	Non-inverting differential clock input.
7	nCLK2	Input	Pulldown	Inverting differential clock input.
8	CLK3	Input	Pulldown	Non-inverting differential clock input.
9	nCLK3	Input	Pulldown	Inverting differential clock input.
10, 11	V <sub>EE</sub>	Power		Negative supply pins.
12, 13	V <sub>BB2</sub> , V <sub>BB1</sub>	Output		ECL reference outputs.
15, 16	nQ, Q	Output		Differential output pair. ECL/LVPECL interface levels.
18, 19	SEL0, SEL1	Input	Pulldown	Clock select inputs. ECL/LVPECL or LVCMOS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**Function Tables****Table 3. Control Input Function Table**

Control Inputs		Clock Out
SEL1	SEL0	Q, nQ
0	0 (default)	CLK0, nCLK0
0	1	CLK1, nCLK1
1	0	CLK2, nCLK2
1	1	CLK3, nCLK3

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	87.2°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 2.375V$  to  $3.465V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	3.3	3.465	V
$I_{EE}$	Power Supply Current				25	mA

**Table 4B. DC Characteristics,  $V_{CC} = 2.375V$  to  $3.465V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{PP}$	Input Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Range; NOTE 1, 2		0.5		$V_{CC} - 0.85$	V
$I_{IH}$	Input High Current	CLK[0:3], nCLK[0:3] $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK[0:3], nCLK[0:3] $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-10			$\mu A$

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**Table 4C. LVPECL DC Characteristics,  $V_{CC} = 2.375V$  to  $3.465V$ ;  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{swing}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 4D. ECL DC Characteristics,  $V_{CC} = 0V$ ;  $V_{EE} = 2.375V$  to  $3.465V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		-1.125		-0.935	V
$V_{OL}$	Output Low Voltage; NOTE 1		-1.895		-1.67	V
$V_{BB1}, V_{BB2}$	Output Voltage Reference; NOTE 2			-1.3		V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Single-ended input operation is limited.  $V_{CC} \geq 3V$  in LVPECL mode.

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{CC} = 2.375V$  to  $3.465V$ ;  $V_{EE} = 0V$  or  $V_{CC} = 0V$ ;  $V_{EE} = -3.8V$  to  $-2.375V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				3	GHz
$f_{jit}$	Additive Phase Jitter, RMS; refer to Additive Phase Jitter section	622.08MHz, 12kHz – 20MHz		0.073		ps
$t_{PD}$	Propagation Delay; NOTE 1		300		615	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				250	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	70		220	ps
$MUX_{ISOLATION}$	MUX Isolation	622.08MHz, $V_{IN}$ 1.6V to 2.4V		-59		dB

All parameters measured up to 1.5GHz, unless otherwise noted.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

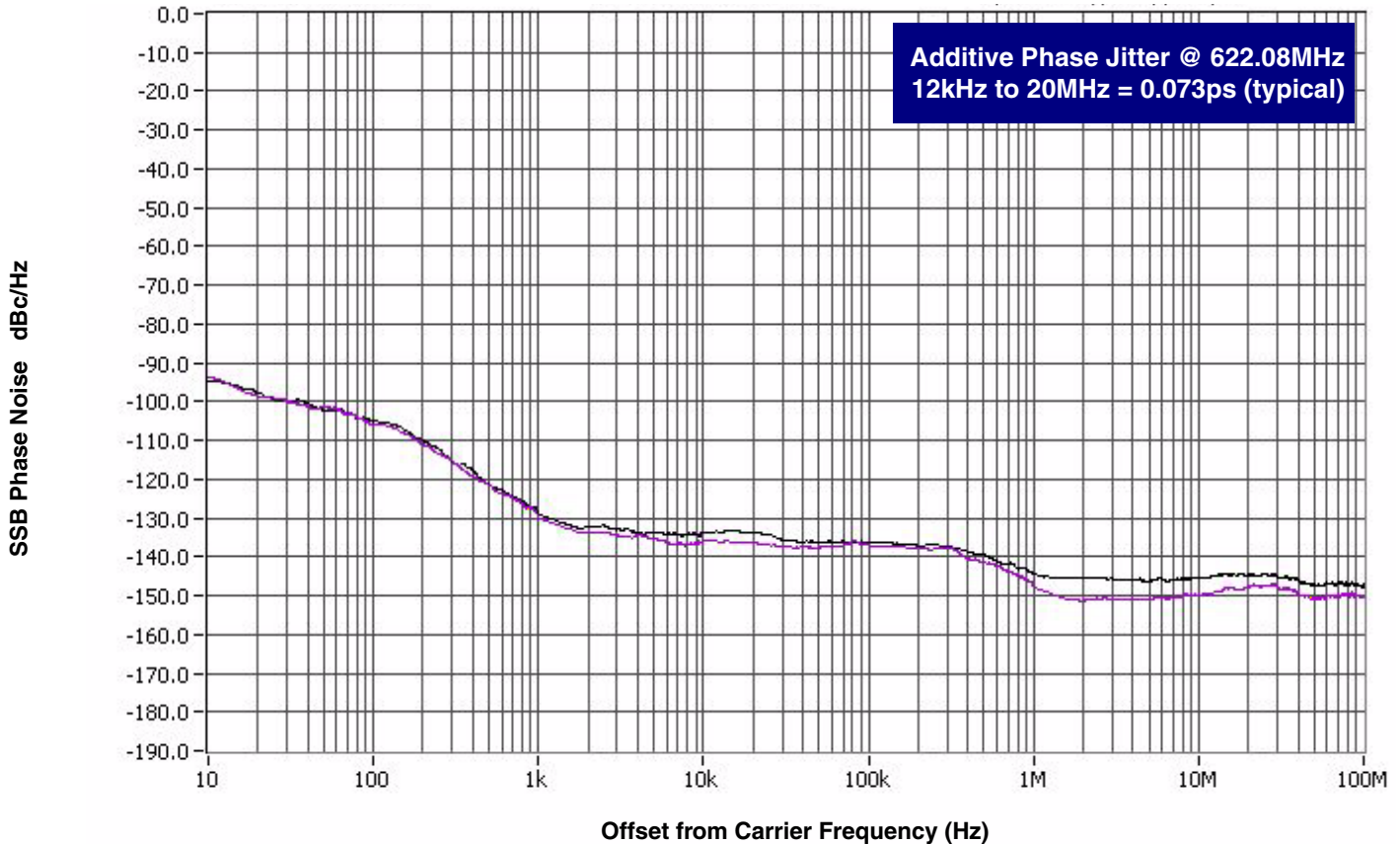
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined according with JEDEC Standard 65.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

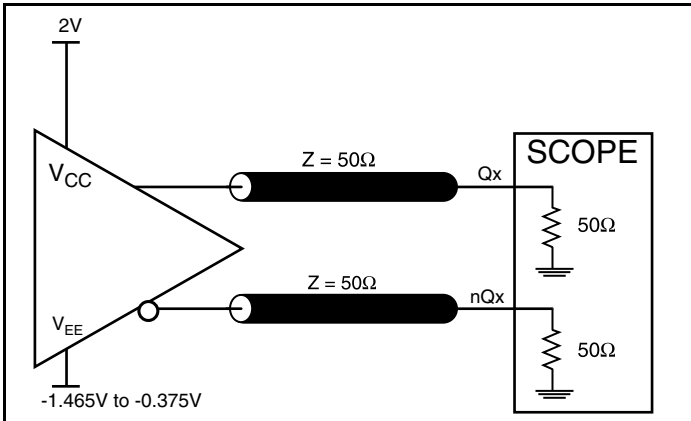
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



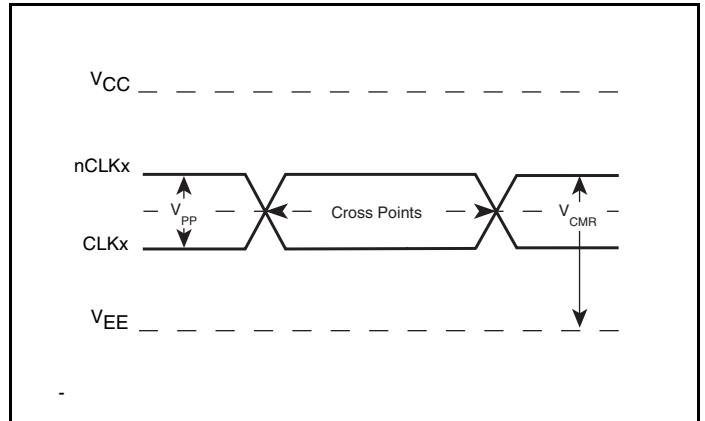
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This

is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

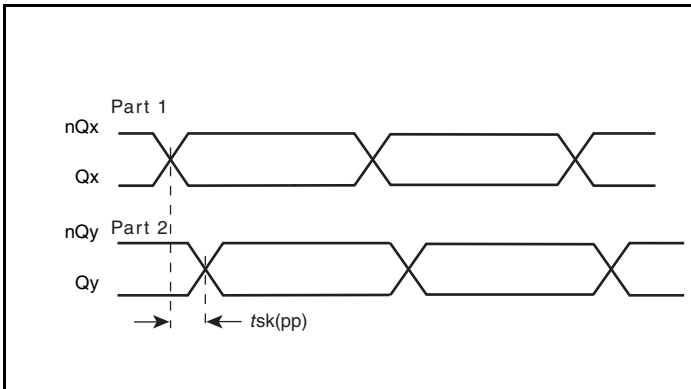
### Parameter Measurement Information



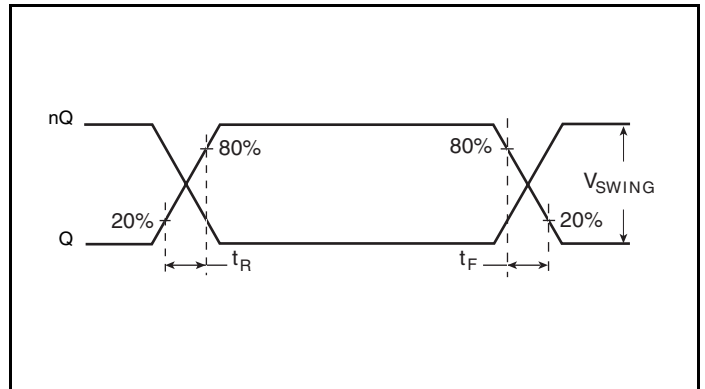
LVPECL Output Load AC Test Circuit



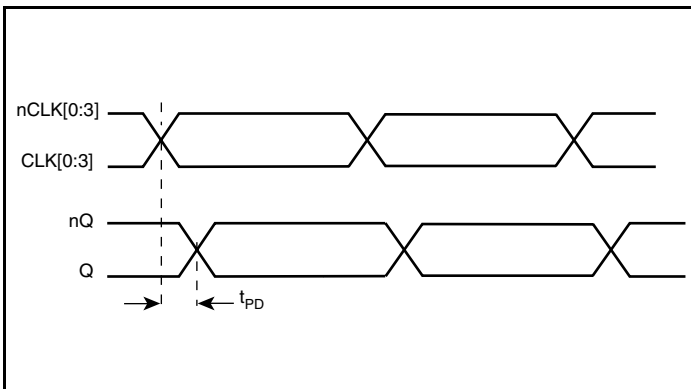
Differential Input Level



Part-to-Part Skew



Output Rise/Fall Time



Propagation Delay

## Application Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

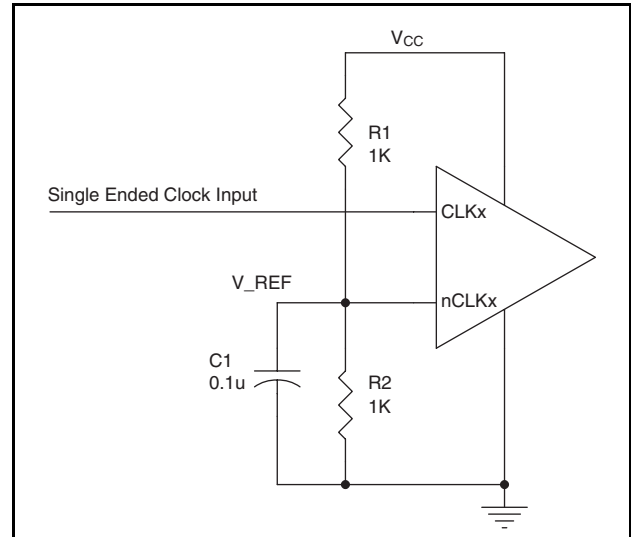


Figure 1. Single-Ended Signal Driving Differential Input

## Recommendations for Unused Input Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, a 1k $\Omega$  resistor should be tied from nCLK to  $V_{CC}$ .

#### Single-ended LVPECL Control Pins

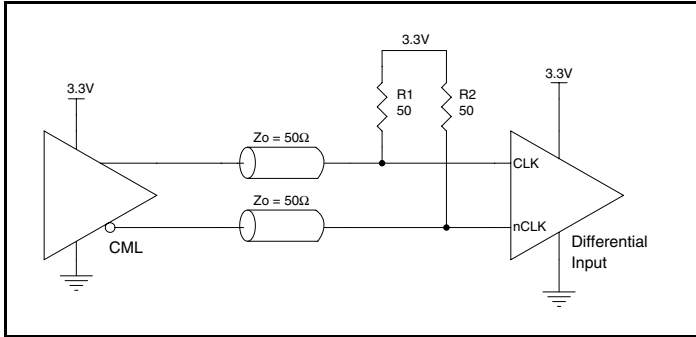
All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.



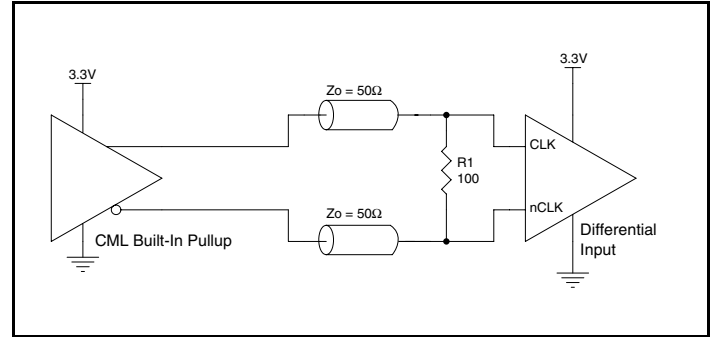
## Clock Input Interface

The CLK/nCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS CLK /nCLK input driven by the most common

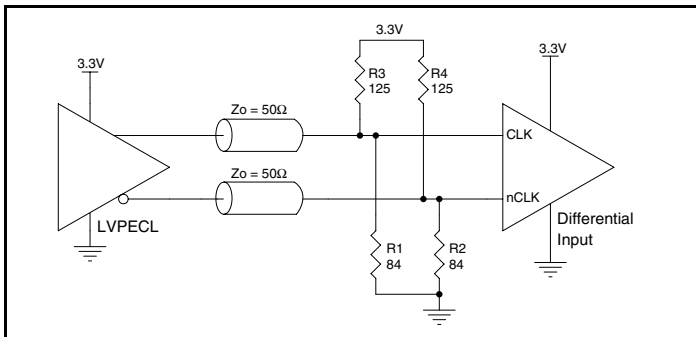
driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



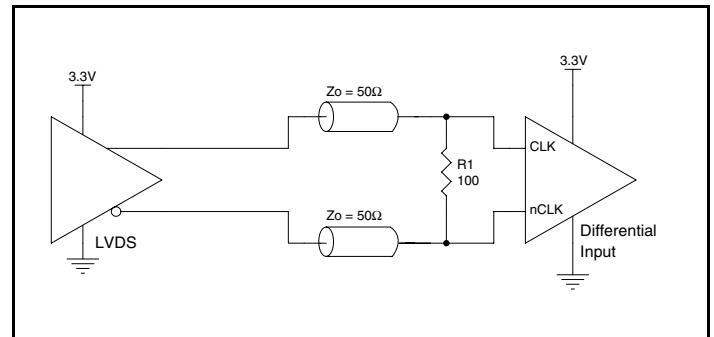
**Figure 2A. HiPerClockS CLK/nCLK Input Driven by a CML Driver**



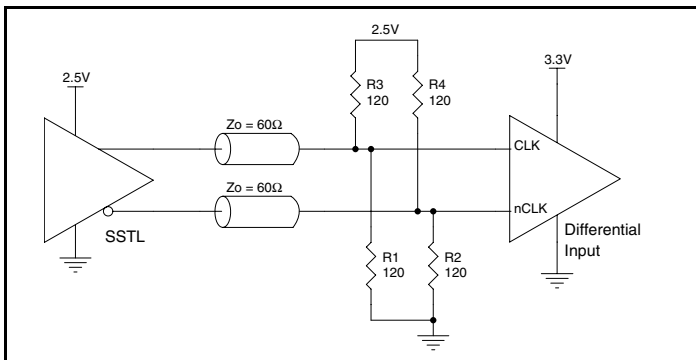
**Figure 2B. HiPerClockS CLK/nCLK Input Driven by a Built-In Pullup CML Driver**



**Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 2E. HiPerClockS CLK/nCLK Input Driven by an SSTL Driver**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

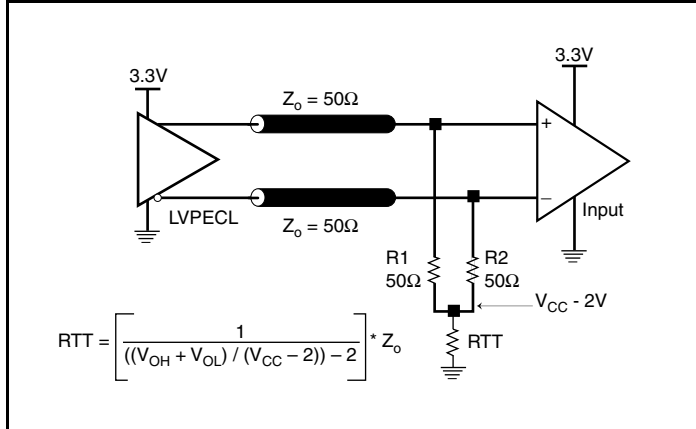


Figure 3A. 3.3V LVPECL Output Termination

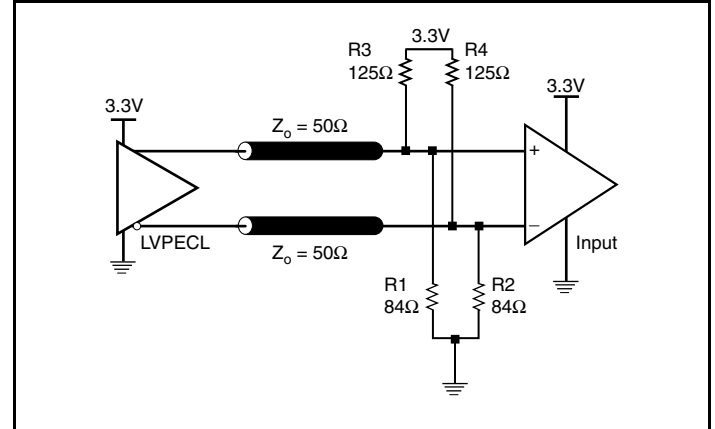


Figure 3B. 3.3V LVPECL Output Termination

### Termination for 2.5V LVPECL Outputs

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.



Figure 4A. 2.5V LVPECL Driver Termination Example

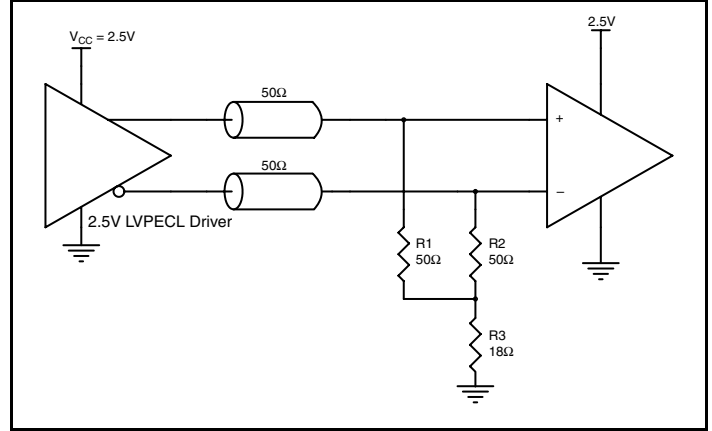


Figure 4B. 2.5V LVPECL Driver Termination Example

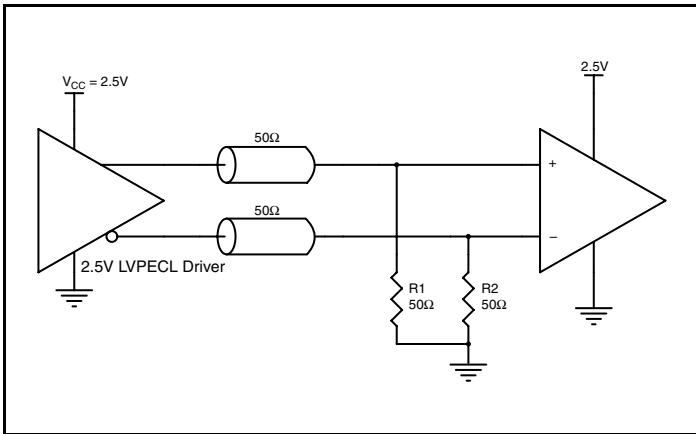


Figure 4C. 2.5V LVPECL Driver Termination Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS53S0571. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS53S0571 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 25mA = \mathbf{86.625mW}$
- Power (outputs)<sub>MAX</sub> = **31.1mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.3V, with all outputs switching) =  $86.625mW + 31.1mW = \mathbf{117.725mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 87.2°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.118\text{W} * 87.2^\circ\text{C/W} = 95.3^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

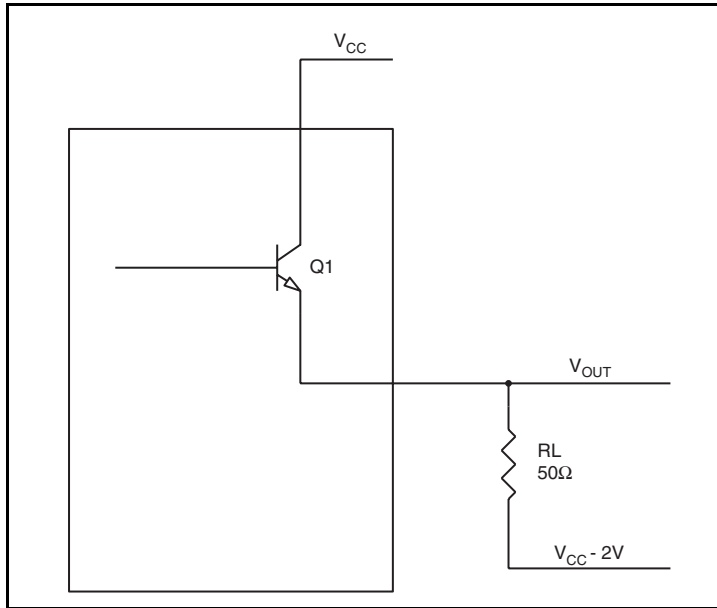
**Table 6. Thermal Resistance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection**

Meters per Second	$\theta_{JA}$ by Velocity		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.



**Figure 5. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.935V$   
( $V_{CC\_MAX} - V_{OH\_MAX}$ ) = **0.935V**
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.67V$   
( $V_{CC\_MAX} - V_{OL\_MAX}$ ) = **1.67V**

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = \mathbf{19.9mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = \mathbf{11.2mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{31.1mW}$

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

## Transistor Count

The transistor count for ICS853S0571 is: 251

## Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

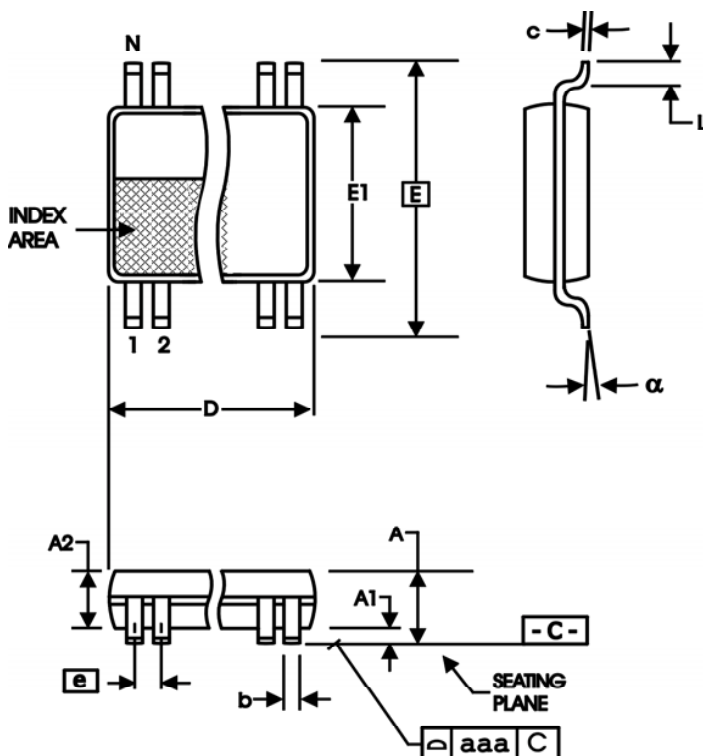


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa	0.10	

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S057AGILF	ICS53S057AIL	"Lead-Free" 20 Lead TSSOP	Tube	-40°C to 85°C
853S057AGILFT	ICS53S057AIL	"Lead-Free" 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications, such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T5	4 7	AC Characteristics Table - added Thermal Note. Recommendations for Unused Input Pins - modified CLK/nCLK Input paragraph. Changed datasheet Header/Footer.	7/30/09
A	T1	2	Pin Description Table - Pins 18 and 19 (SELx description) added LVCMOS levels.	5/16/2012



## We've Got Your Timing Solution



6024 Silver Creek Valley Road  
San Jose, California 95138

**Sales**  
800-345-7015 (inside USA)  
+408-284-8200 (outside USA)  
Fax: 408-284-2775  
[www.IDT.com/go/contactIDT](http://www.IDT.com/go/contactIDT)

**Technical Support**  
[netcom@idt.com](mailto:netcom@idt.com)  
+480-763-2056

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2012. All rights reserved.