阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网,版权归原作者所有。如读者和版权方有任何异议请及时告之,我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译,其目的是协助用户阅读,该译文无法自动跟随原稿更新,同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料,来自厂商的技术支持或者使用者的心得体会等,其内容可能存在描 叙上的差异,建议读者做出适当判断。
- 4.如需与我们联系,请发邮件到marketing@iczoom.com,主题请标有"数据手册"字样。

Read Statement

- 1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
- 2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
- 3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
- 4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .





Not Recommended for New Designs

Low Jitter and Skew DC to 140MHz Clock Buffer

Key Features

- DC to 140 MHz operating frequency range
- · Low output clock skew: 50ps-typ
- Low part-to-part output skew: 100 ps-typ
- Low output propagation delay: 2.5ns-typ
- 3.3V +/-10% operation supply voltage
- Low power dissipation:
 - 7 mA-typ at 33MHz
 - 9 mA-typ at 66MHz
 - 12 mA-typ at 133MHz
- One input to four output fanout buffer drivers
- Output Enable (OE) control function
- Available in 8-pin TSSOP package
- · Available in Commercial and Industrial grades
- Available in Lead (Pb) free package

Applications

- General Purpose PCI/PCI-X Clock Buffer
- Printers, MFPs and Digital Copiers
- PCs and Work Stations
- Routers, Switches and Servers
- Datacom and Telecom
- High-Speed Digital Embedded Systems

Description

The SL2304NZ is a low skew, jitter and power fanout Buffer designed to produce up to four (4) clock outputs from one (1) reference input clock, for high speed clock distribution, including PCI/PCI-X applications.

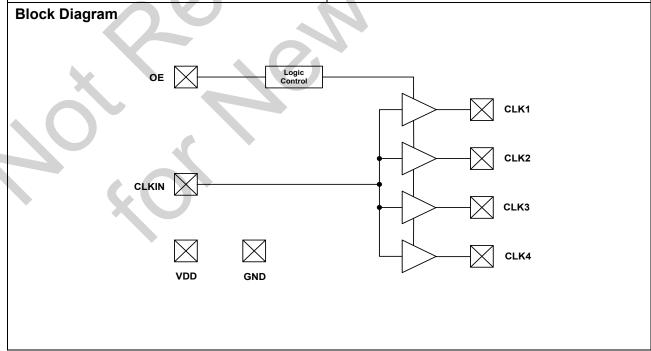
The SL2304NZ products operate from DC to 140MHz.

The only difference between SL2304NZ-1 and SL2304NZ-1Z is the OE logic implementation. Refer to the Available OE Logic Configuration Table. 1

Refer to SL23EP04NZ products for DC to 220MHz-max frequency range and 2.5V to 3.3V power supply operation, improved skew, jitter and higher drive options.

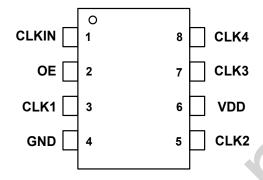
Benefits

- Up to four (4) distribution of input clock
- Low propogation delay
- Low output-to-output skew
- Low output clock Jitter
- · Low power dissipation





Pin Configuration



8-Pin TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Clock Input
2	OE	Output	Output Enable. Refer to the Table. 1 for Logic Table
3	CLK1	Output	Buffered Clock Output 1
4	GND	Power	Power Ground.
5	CLK2	Output	Buffered Clock Output 2
6	VDD	Output	3.3V Power Supply
7	CLK3	Power	Buffered Clock Output 3
8	CLK4	Input	Buffered Clock Output 4

Rev 2.1, May 6, 2008 Page 2 of 9



General Description

The SL2304NZ is a low skew, jitter and power fanout Buffer designed to produce up to four (4) clock outputs from one (1) reference input clock, for high speed clock distribution, including PCI/PCI-X applications.

Input and output Frequency Range

The input and output frequency is the same (1x) for SL2304NZ-1 and SL2304NZ-1Z and operates from DC to 140MHz clock range with up to 25pF output load.

OE (Output Enable) Function

The only difference between SL2304-1 and SL2304NZ-1Z is the OE logic implementation. When OE=0, SL2404NZ-1 outputs are disabled and outputs are at Logic Low. In the case of SL2304NZ-1Z the outputs are at High-Z. Refer to the Available OE Logic Configuration Table. 1 below.

Output Clock Skew

All outputs should drive the similar load to achieve outputto-output skew and input-to-output delay specifications as given in the switching electrical tables.

Power Supply Range (VDD)

The SL2304NZ is designed to operate 3.3V+/-10% (3.63V-max to 2.97V-min) VDD power supply range. An internal on-chip voltage regulator is used to provide to constant power supply of 1.8V, leading to a consistent and stable electrical performance in terms of skew and jitter. The SL2304NZ I/O is powered by using VDD.

Refer to SL23EP04NZ products for DC to 220MHz-max frequency range, 2.5V to 3.3V power supply operation, improved skew, jitter and higher drive options.

Contact SLI for 1.8V power supply Fan-Out Buffer and ZDB products.

CLKIN (Pin-1)	OE (Pin-2)	SL2304NZ-1 CLKOUT [1:4]	SL2304NZ-1Z CLKOUT [1:4]
Low	Low	Low	High-Z
High	Low	Low	High-Z
Low	High	Low	Low
High	High	High	High

Table 1. Available SL2304 CLKIN and OE Logic Configurations

Rev 2.1, May 6, 2008 Page 3 of 9



Absolute Maximum Ratings (All Products)

Description	Condition	Min	Max	Unit
Supply voltage, VDD		-0.5	4.6	V
All Inputs and Outputs		-0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	-40	85	°C
Storage Temperature	No power is applied	-65	150	°C
Junction Temperature	In operation, power is applied	(-)	125	°C
Soldering Temperature			260	°C
ESD Rating (Human Body Model)	JEDEC22-A114D	-4,000	4,000	V
ESD Rating (Charge Device Model)	JEDEC22-C101C	-1,500	1,500	٧
ESD Rating (Machine Model)	JEDEC22-A115D	-200	200	V

Operating Conditions (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

	•		-			
Description	Symbol	Condition	Min	Тур	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Operating Temperature	TA	Ambient Temperature	0	-	70	°C
Input Capacitance	VIH	Pins 1 and 2	_	3	5	pF
Output Canacitanas	CL1	All outputs≤100MHz	_	-	30	pF
Output Capacitance	CL2	All outputs≤140MHz	_	-	15	pF
Input Operating Frequency CLKIN Input Clock R		Input Clock Range	DC	_	140	MHz
Input Operating Frequency	CLKN2	Input Clock Range, CL=30pF	DC	_	100	MHz

Rev 2.1, May 6, 2008 Page 4 of 9



DC Electrical Characteristics (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Тур	Max	Unit
Input Low Voltage	VINL	CLKIN and OE	-	_	0.8	V
Input High Voltage	VINH	CLKIN and OE	2.0	_	VDD+0.3	V
Input Low Current	IINL	0 < VIN < 0.8V	-5	+/-2	5	μΑ
Input High Current	IINH	2.4V < VIN < VDD	-5	+/-2	5	μΑ
Output Low Voltage	VOL1	IOL=24mA	-		0.80	V
Output Low Voltage	VOL2	IoL=12mA			0.55	V
Output High Voltage	VOH1	IOH=-24mA	2.0	_	- (V
Output High Voltage	VOH1	IOH=-12mA	2.4	-		>
Power Supply Current	IDD1	CLKIN=33MHz CL=0 (No load at outputs)) -	7	11	mA
Power Supply Current	IDD2	CLKIN=66MHz CL=0 (No load at outputs)	-	9	14	mA
Power Supply Current	IDD3	CLKIN=133MHz CL=0 (No load at outputs)	_C	12	18	mA

Switching Electrical Characteristics (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Тур	Max	Unit
Output Fraguency Dange	FOUT1	CL=15pF	DC	-	140	MHz
Output Frequency Range	FOUT1	CL=30pF	DC	_	100	MHz
Output Rise/Fall Time	tr/f-1	Measured at 0.8V to 2.0V CL=15pF	I	-	2.0	ns
Output Rise/Fall Time	tr/f-2	Measured at 0.8V to 2.0V CL=30pF	I	_	2.4	ns
Input Duty Cycle	DC1	Measured at VDD/2	20	50	80	%
Output Duty Cycle	DC2	CL=15pF, Fout=140MHz Measured at VDD/2	45	-	55	%
Output Duty Cycle	DC3	CL=30pF, Fout=100MHz Measured at VDD/2	40	_	60	%
Output to Output Skew	SKW1 Measured at VDD/2 and – Outputs are equally loaded		-	50	100	ps
Part to Part Skew	SKW2	Measured at VDD/2 and Outputs are equally loaded	ı	100	200	ps
Propagation Delay Time	PDT	Measured at VDD/2 from CLKIN to Output Clock rising edge 1.5		2.5	3.5	ns
Cycle-to-Cycle Jitter	CCJ1	CLKIN=66MHz and CL=15	_	75	150	ps
Cycle-to-Cycle Jitter	CCJ2	CLKIN=133MHz and CL=15	_	50	100	ps

Rev 2.1, May 6, 2008 Page 5 of 9



Operating Conditions (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Тур	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	٧
Operating Temperature	TA	Ambient Temperature	-40	_	85	°C
Input Capacitance	VIH	Pins 1 and 2	-	3	6	pF
Output Canacitanes	CL1	All outputs≤100MHz	-		30	pF
Output Capacitance	CL2	All outputs≤140MHz	-	-	15	pF
Input Operating Frequency	CLKN1	Input Clock Range, CL=15pF	DC	<u> </u>	140	MHz
Input Operating Frequency	CLKN2	Input Clock Range, CL=30pF	DC	. –	100	MHz

DC Electrical Characteristics (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Тур	Max	Unit
Input LOW Voltage	VINL	CLKIN and OE			0.8	V
Input HIGH Voltage	VINH	CLKIN and OE	2.0) -	VDD+0.3	V
Input LOW Current	IINL	0 < VIN < 0.8V	-6	+/-3	6	μΑ
Input HIGH Current	IINH	2.4V < VIN < VDD	-6	+/-3	6	μΑ
Output Law Valtage	VOI	IoL=24mA	_	_	0.80	V
Output Low Voltage	VOL	IOL=12mA	_	_	0.55	V
Output High Voltage	VOH	IOH=-24mA	2.0	_	_	V
Output High Voltage	VOH	IOH=-12mA	2.4	_	_	V
Power Supply Current	IDD1	CLKIN=33MHz CL=0 (No load at outputs)	_	8	12	mA
Power Supply Current	IDD2	CLKIN=66MHz CL=0 (No load at outputs)	_	10	15	mA
Power Supply Current	IDD3	CLKIN=133MHz CL=0 (No load at outputs)	_	14	20	mA

Rev 2.1, May 6, 2008 Page 6 of 9



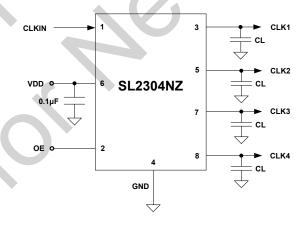
Switching Electrical Characteristics (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Тур	Max	Unit
Output Fraguency Bongs	FOUT1	CL=15pF	DC	-	140	MHz
Output Frequency Range	FOUT2	CL=30pF	DC	-	100	MHz
Output Rise/fall Time	tr/f-1	CL=15pF, measured at 0.8V to 2.0V	-		2.2	ns
Output Rise/Fall Time	tr/f-2	CL=30pF, measured at 0.8V to 2.0V	1		2.6	ns
Input Duty Cycle	DC1	Measured at VDD/2	20		80	%
Output Duty Cycle	DC2	CL=15pF, Fout=140MHz Measured at VDD/2	45		55	%
Output Duty Cycle	DC3	CL=30pF, Fout=100MHz Measured at VDD/2	40	-	60	%
Output to Output Skew	SKW1	Measured at VDD/2 and Outputs are equally loaded	-	60	120	ps
Part to Part Skew	SKW2	Measured at VDD/2 and Outputs are equally loaded	-	120	240	ps
Propagation Delay Time	PDT	Measured at VDD/2 from CLKIN to Output Clock rising edge and Outputs are equally loaded	1.2	2.5	3.8	ns
Cycle-to-Cycle Jitter	CCJ1	CLKIN=66MHz and CL=15		80	160	ps
Cycle-to-Cycle Jitter	CCJ2	CLKIN=133MHz and CL=15	_	60	120	ps

External Components & Design Considerations

Typical Application Schematic



Recommendations

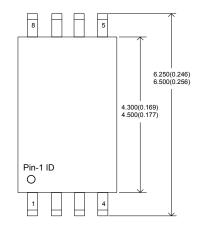
Decoupling Capacitor: A decoupling capacitor of $0.1\mu F$ must be used between VDD and VSS pins. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Rev 2.1, May 6, 2008 Page 7 of 9

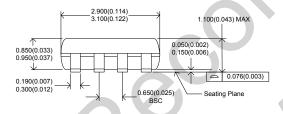


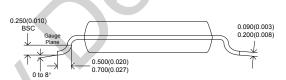
Package Outline and Package Dimensions

8-Pin TSSOP (4.4 mm)



Dimensions are in milimeters(inches). Top line: (MIN) and Bottom line: (Max)





Thermal Characteristics

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Thermal Resistance Junction to Ambient	θЈА	Still air	-	110	-	°C/W
	θJA	1m/s air flow	-	100	-	°C/W
	θЈΑ	3m/s air flow	-	80	1	°C/W
Thermal Resistance Junction to Case	θЈС	Independent of air flow	-	35	-	°C/W

Rev 2.1, May 6, 2008 Page 8 of 9



Ordering Information [1]

Ordering Number	Marking	Shipping Package	Package	Temperature
SL2304NZZC-1	SL2304NZC-1	Tube	8-pin TSSOP	0 to 70°C
SL2304NZZC-1T	SL2304NZC-1	Tape and Reel	8-pin TSSOP	0 to 70°C
SL2304NZZI-1	SL2304NZI-1	Tube	8-pin TSSOP	-40 to 85°C
SL2304NZZI-1T	SL2304NZI-1	Tape and Reel	8-pin TSSOP	-40 to 85°C
SL2304NZZC-1Z	SL2304NZC-1Z	Tube	8-pin TSSOP	0 to 70°C
SL2304NZZC-1ZT	SL2304NZC-1Z	Tape and Reel	8-pin TSSOP	0 to 70°C
SL2304NZZI-1Z	SL2304NZI-1Z	Tube	8-pin TSSOP	-40 to 85°C
SL2304NZZI-1ZT	SL2304NZI-1Z	Tape and Reel	8-pin TSSOP	-40 to 85°C

Notes:

1. The SL2304NZ products are RoHS compliant.

Rev 2.1, May 6, 2008 Page 9 of 9





Timing Portfolio www.silabs.com/timina



SW/HW www.silabs.com/CBPro



Quality www.silabs.com/quality



Support and Community community.silabs.com

Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are not designed or authorized for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, Silabs® and the Silicon Labs logo®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISOmodem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc. 400 West Cesar Chavez Austin, TX 78701