

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

## General Description

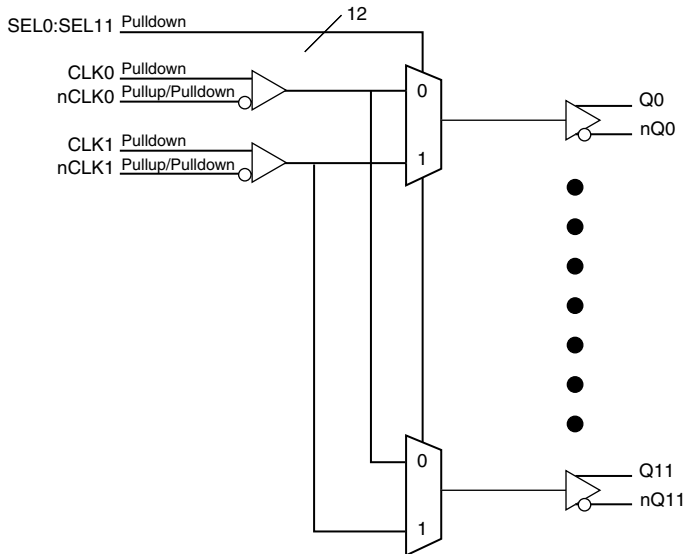
The 85352 is a 12 bit, 2-to-1 LVPECL Clock Buffer. Individual input select controls support independent multiplexer operation from a common clock input source. Clock inputs accept most standard differential levels.

The 85352 is characterized at full 3.3V or mixed 3.3V core/2.5V output operating supply modes.

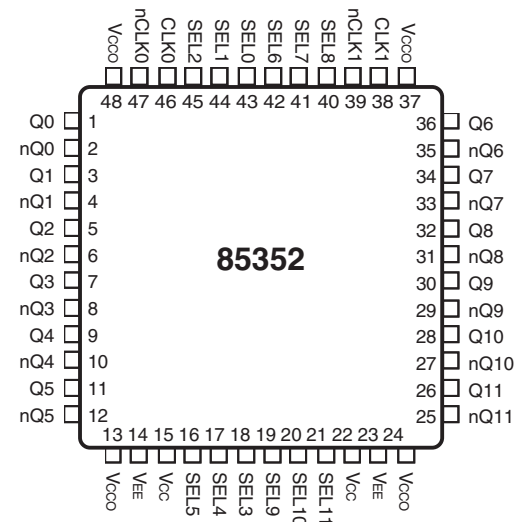
## Features

- Twelve, 2-to-1 multiplexers with LVPECL outputs
- Selectable differential CLKx, nCLKx input pairs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Individual select control for each multiplexer
- Select inputs accept LVCMOS / LVTTTL levels
- Propagation delay: 2ns (maximum)
- Additive Phase Jitter, RMS: 0.21ps (typical), 3.3V
- Full 3.3V or mixed 3.3V core/2.5V output supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment



### 85352

**48-Lead TQFP, E-Pad**  
**7mm x 7mm x 1.0mm package body**  
**Y Package**  
**Top View**

## Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2 3, 4 5, 6 7, 8 9, 10 11, 12 25, 26 27, 28 29, 30 31, 32 33, 34 35, 36	Q0, nQ0 Q1, nQ1 Q2, nQ2 Q3, nQ3 Q4, nQ4 Q5, nQ5 nQ11, Q11 nQ10, Q10 nQ9, Q9 nQ8, Q8 nQ7, Q7 nQ6, Q6	Output		Differential output pairs. LVPECL interface levels.
13, 24, 37, 48	V <sub>CC0</sub>	Power		Output power supply pins.
14, 23	V <sub>EE</sub>	Power		Negative power supply pins.
15, 22	V <sub>CC</sub>	Power		Positive power supply pins.
16, 17, 18, 19, 20, 21, 40, 41, 42, 43, 44, 45	SEL5, SEL4, SEL3, SEL9, SEL10, SEL11, SEL8, SEL7, SEL6, SEL0, SEL1, SEL2	Input	Pulldown	Clock select inputs. LVCMOS / LVTTTL interface levels. See Table 3.
38	CLK1	Input	Pulldown	Non-inverting differential clock input.
39	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating.
46	CLK0	Input	Pulldown	Non-inverting differential clock input.
47	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Table

**Table 3. Control Input Function Table**

SELx	Selected Clock inputs
0	CLK0, nCLK0
1	CLK1, nCLK1

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	27.6°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V$  to  $3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		2.375	3.3	3.465	V
$I_{EE}$	Power Supply Current				170	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V$  to  $3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	SEL[0:11] $V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	SEL[0:11] $V_{CC} = 3.465V, V_{IN} = 0V$	-5			$\mu A$

**Table 4C. Differential Input DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V$  to  $3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK0, CLK1			150	$\mu A$
		nCLK0, nCLK1			150	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1	-5			$\mu A$
		nCLK0, nCLK1	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.0	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

**Table 4D. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V$  to  $3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

## AC Electrical Characteristics

**Table 5A. AC Electrical Characteristics,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1		1.0	1.5	2.0	ns
$f_{jit}$	Buffer Additive Phase Jitter, RMS: refer to additive Phase Jitter Section	156.25MHz Integration Range: (12kHz – 20MHz)		0.21		ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				180	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 4				750	ps
$t_R / t_F$	Output Rise/ Fall Time	20% to 80%	150		700	ps
odc	Output Duty Cycle	$f \leq 622MHz$	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

**Table 5B. AC Electrical Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1		1.0	1.5	2.0	ns
$f_{jit}$	Buffer Additive Phase Jitter, RMS	156.25MHz Integration Range: (12kHz – 20MHz)		0.23		ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				180	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 4				750	ps
$t_R / t_F$	Output Rise/ Fall Time	20% to 80%	150		700	ps
odc	Output Duty Cycle	$f \leq 622MHz$	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

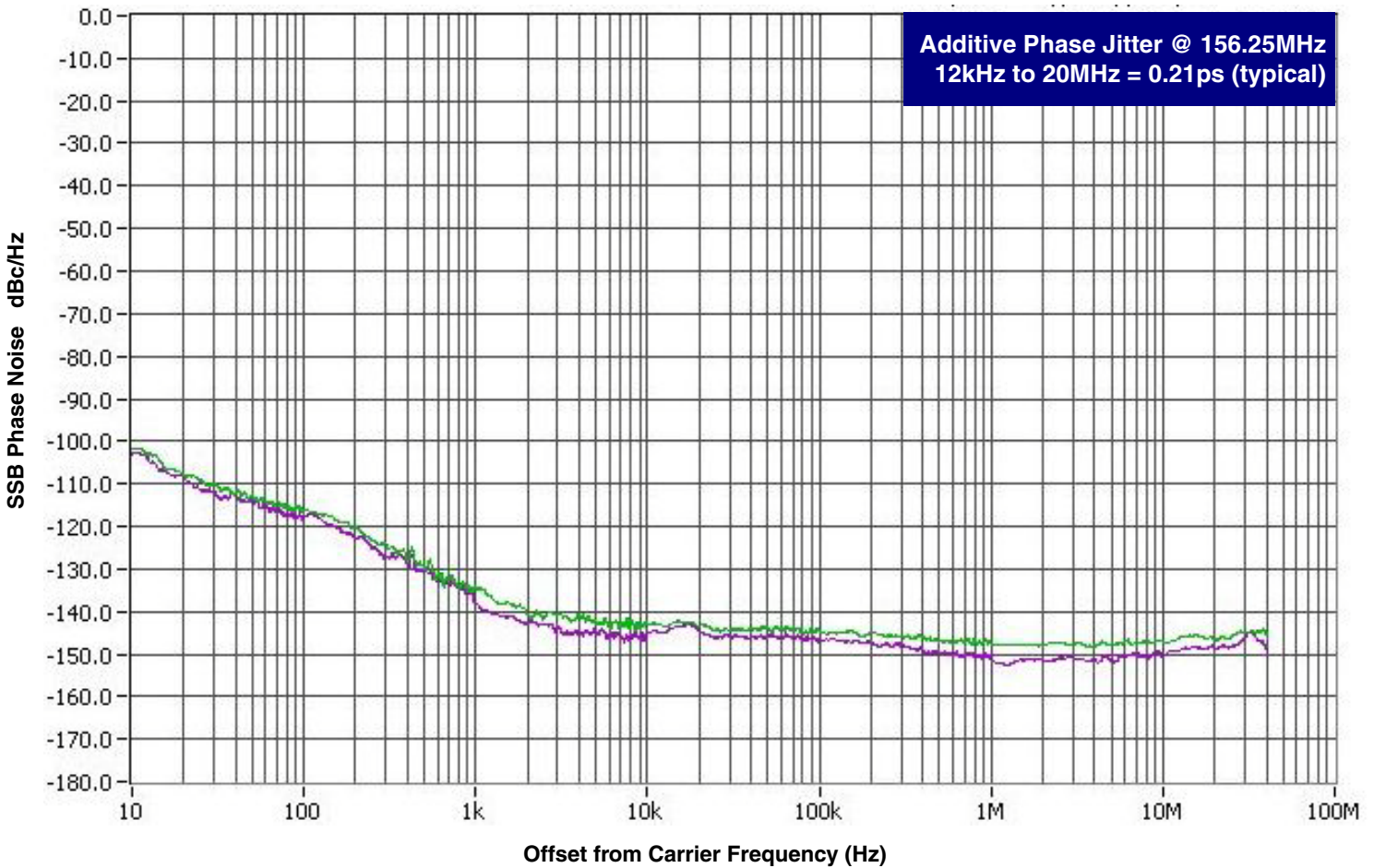
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

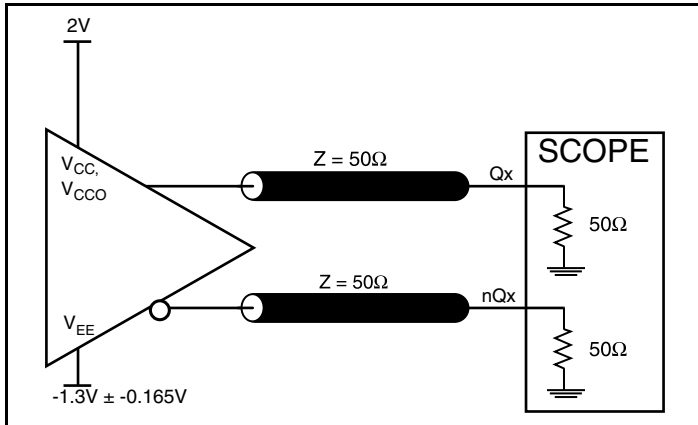
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



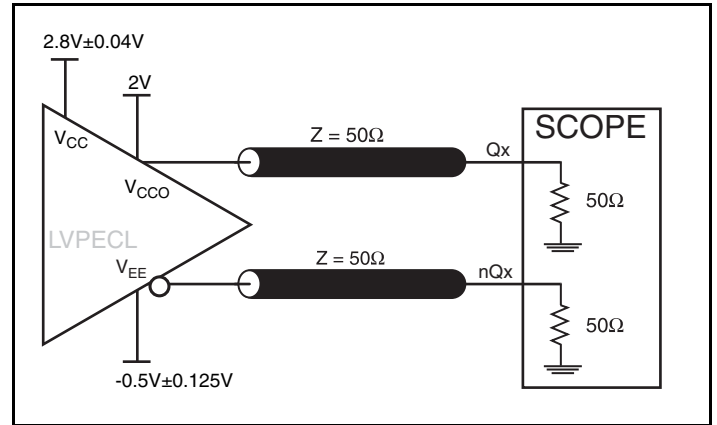
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "Rohde & Schwarz Signal Generator SMA100A 9kHz – 6GHz as external input to a Hewlett Packard 8133A 3GHz Pulse Generator".

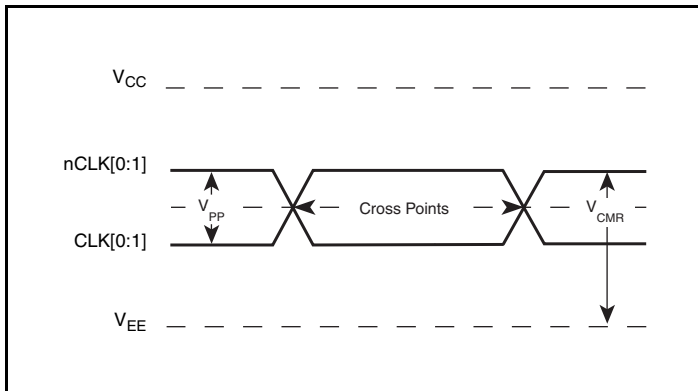
### Parameter Measurement Information



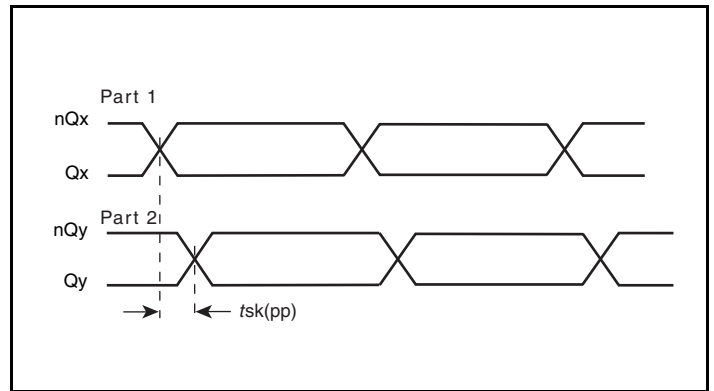
3.3V Core / 3.3V LVPECL Output Load AC Test Circuit



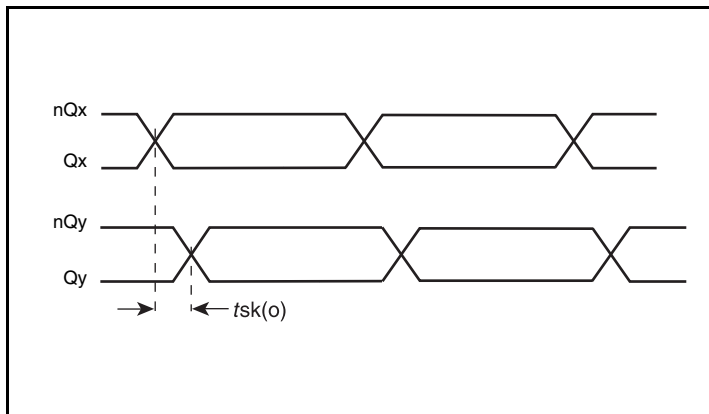
3.3V Core / 2.5V LVPECL Output Load AC Test Circuit



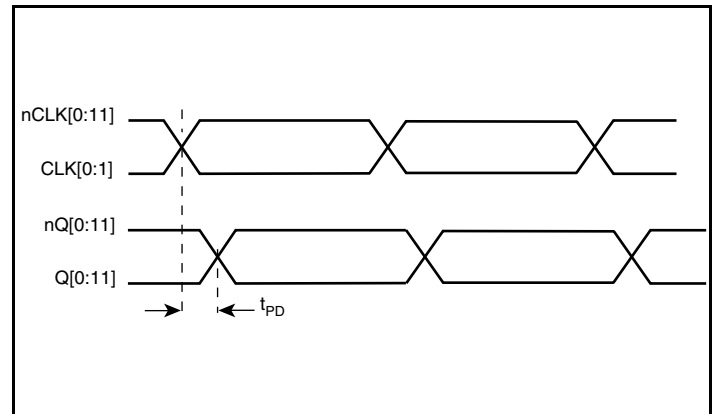
Differential Input Level



Part-to-Part Skew

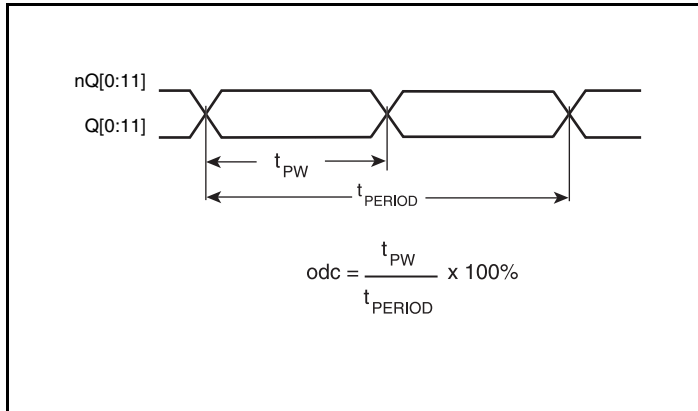


Output Skew

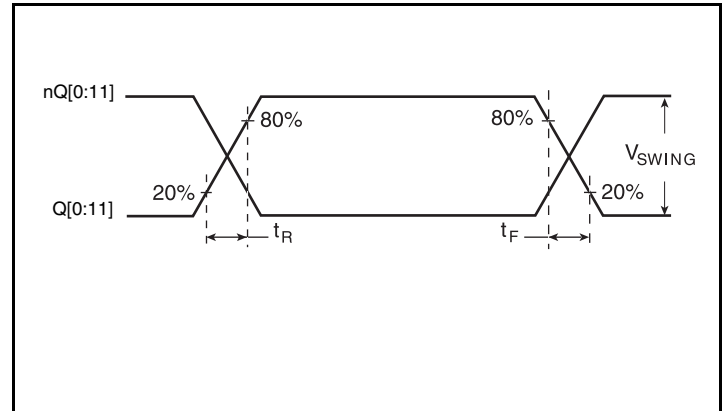


Propagation Delay

## Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

##### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

#### Outputs:

##### LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



## Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most  $50\Omega$  applications, R3 and R4 can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

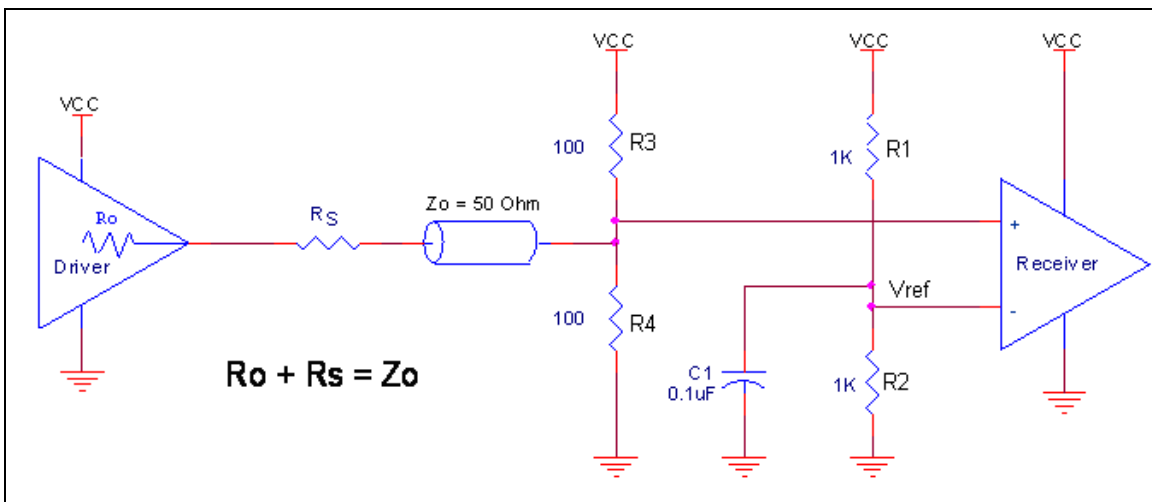


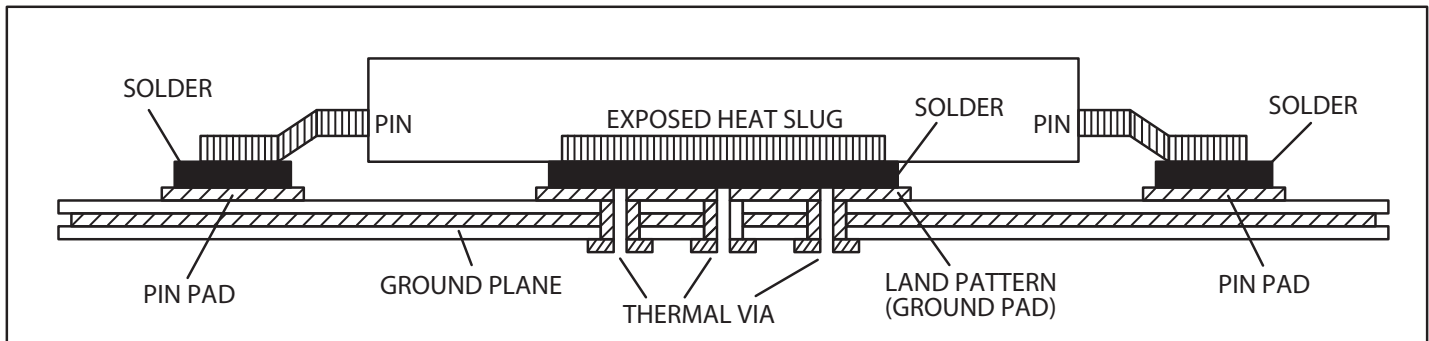
Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

## EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

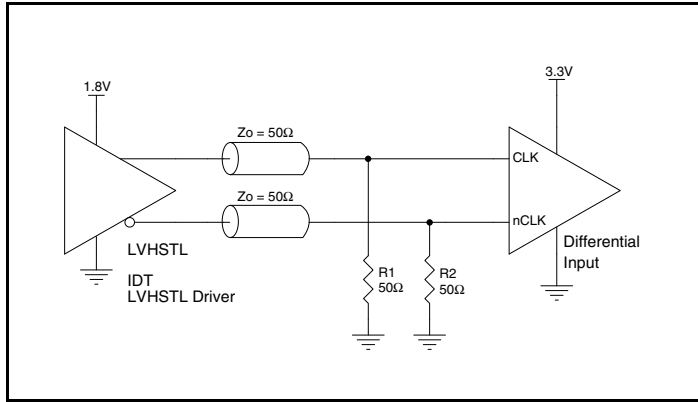


**Figure 2. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)**

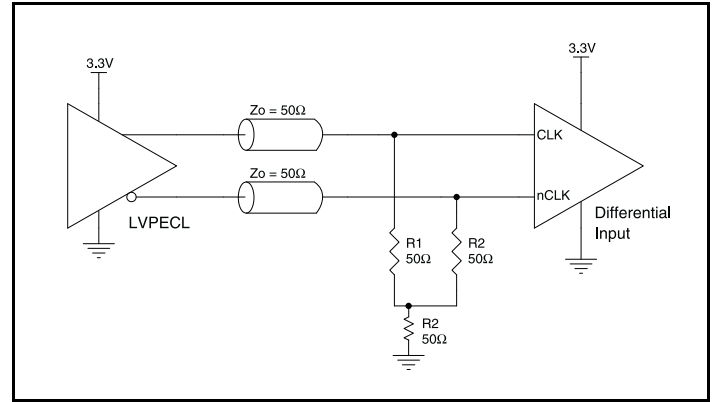
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

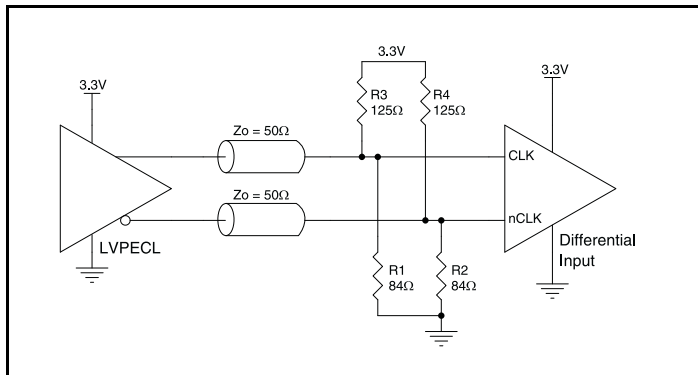
with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for IDT LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



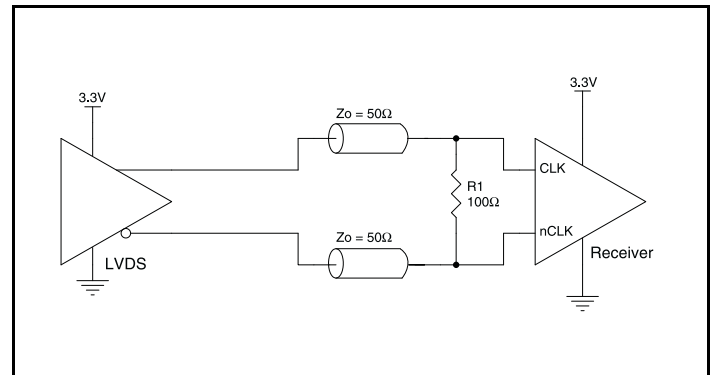
**Figure 3A. CLK/nCLK Input Driven by an IDT LVHSTL Driver**



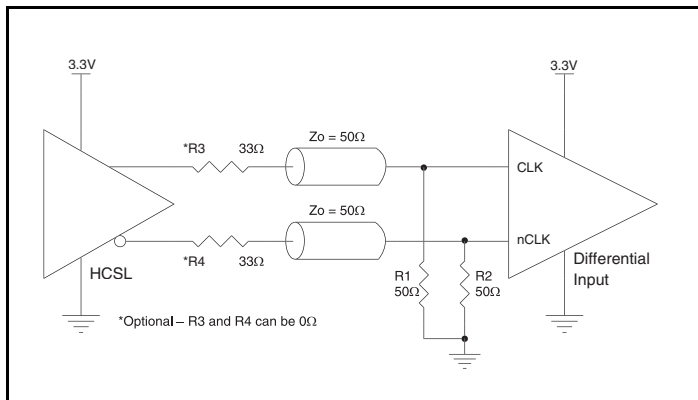
**Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



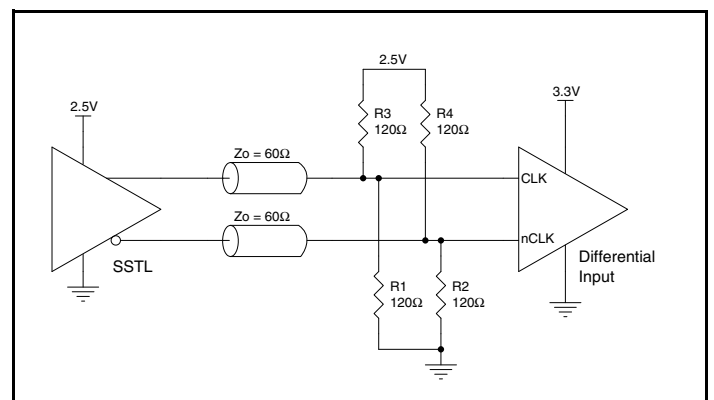
**Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

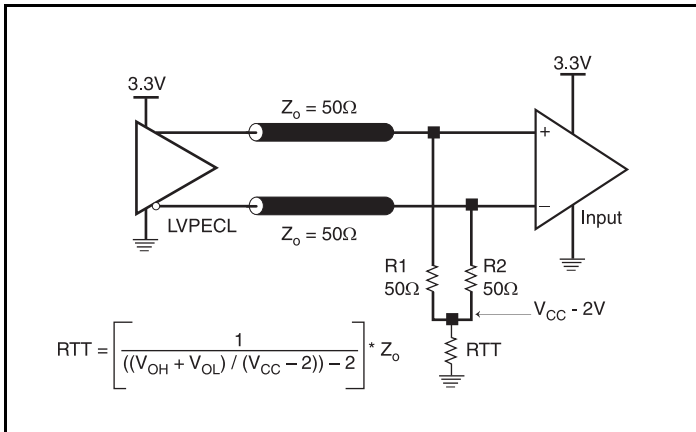


Figure 4A. 3.3V LVPECL Output Termination

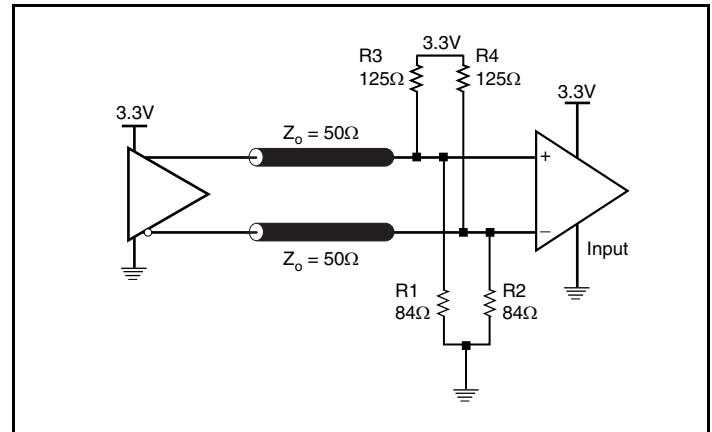


Figure 4B. 3.3V LVPECL Output Termination

### Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC} - 2V$ . For  $V_{CC0} = 2.5V$ , the  $V_{CC0} - 2V$  is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

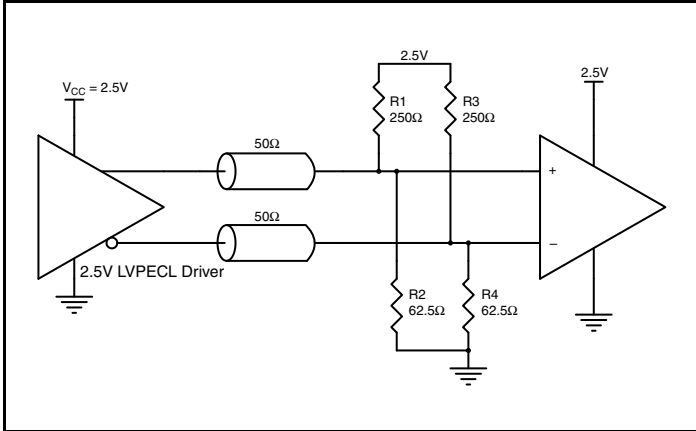


Figure 5A. 2.5V LVPECL Driver Termination Example

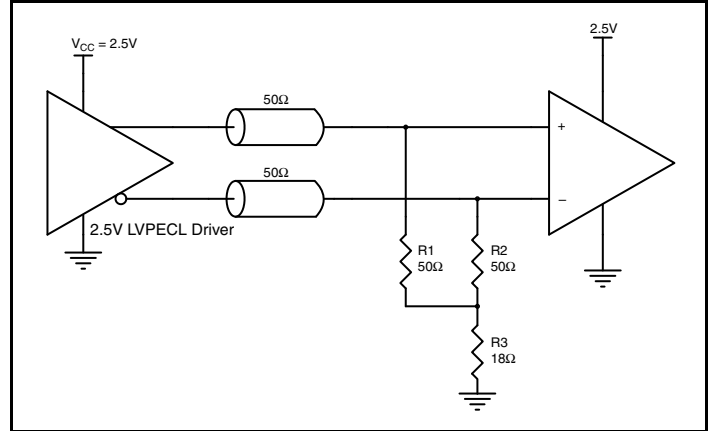


Figure 5B. 2.5V LVPECL Driver Termination Example

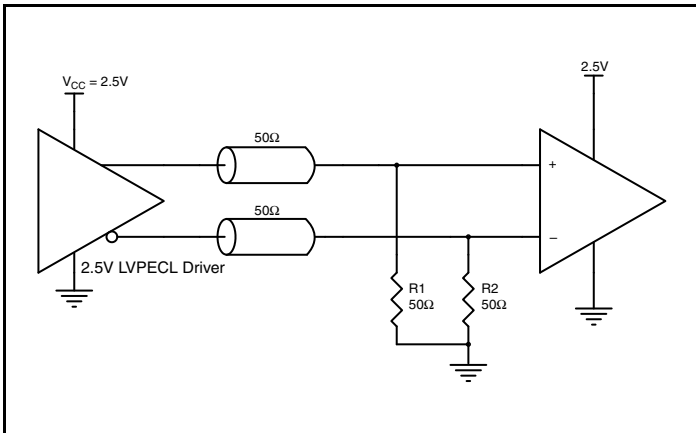


Figure 5C. 2.5V LVPECL Driver Termination Example

## Application Schematic Example

Figure 6 shows an example of 85352 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . The decoupling capacitor should be located as close as possible to the power pin. For

the LVPECL output drivers, only two terminations examples are shown in this schematic. Additional termination approaches can be found in the LVPECL Termination Application Note.

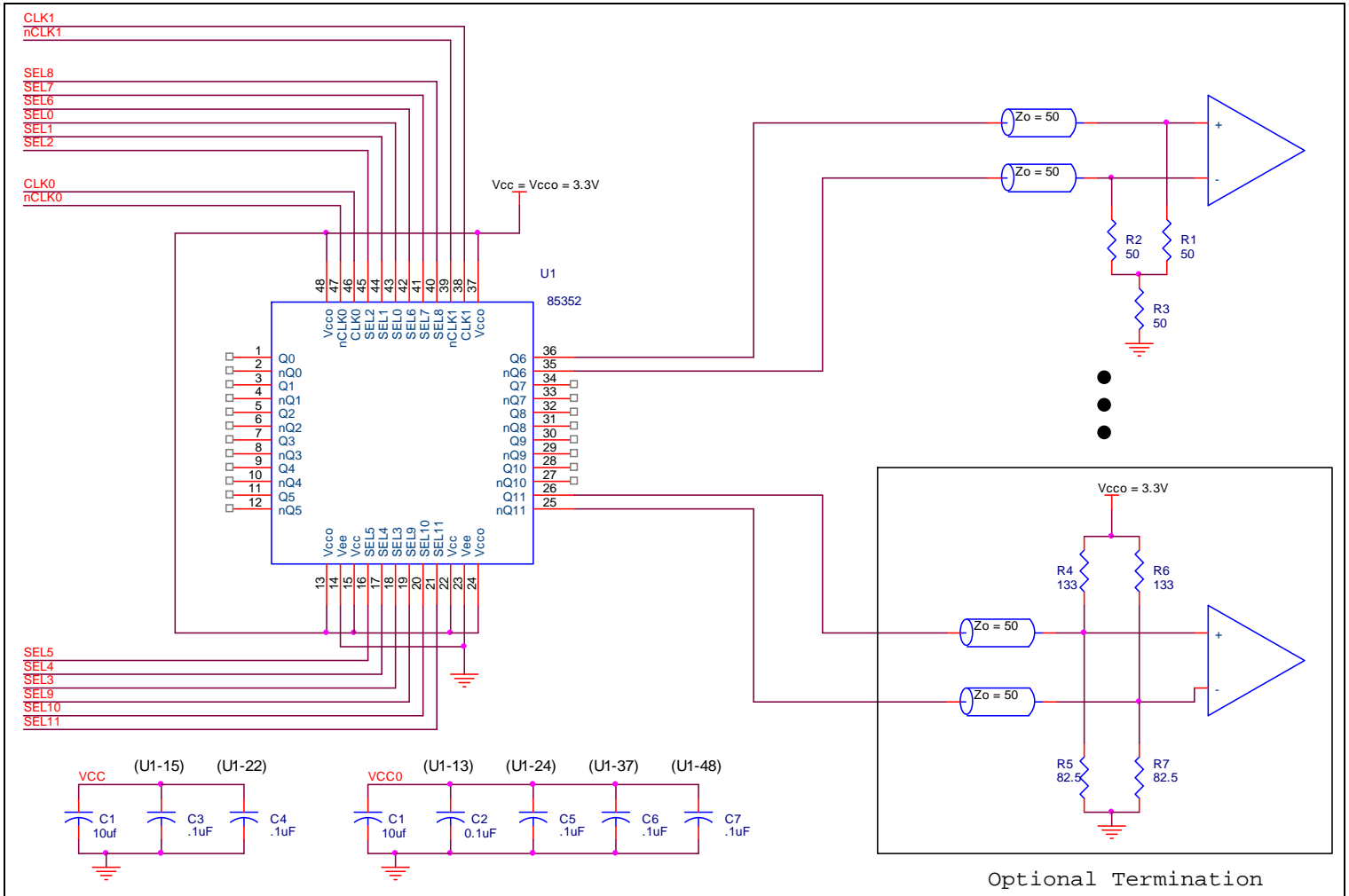


Figure 6. 85352 Application Schematic

## Power Considerations

This section provides information on power dissipation and junction temperature for the 85352. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 85352 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 170mA = \mathbf{589.05mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $12 * 30mW = \mathbf{360mW}$

**Total Power<sub>MAX</sub>** (3.3V, with all outputs switching) =  $589.05mW + 360mW = \mathbf{949.05mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ C$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ C$  ensures that the bond wire and bond pad temperature remains below  $125^\circ C$ .

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is  $22.6^\circ C/W$  per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ C$  with all outputs switching is:

$$85^\circ C + 0.949W * 22.6^\circ C/W = 106.4^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

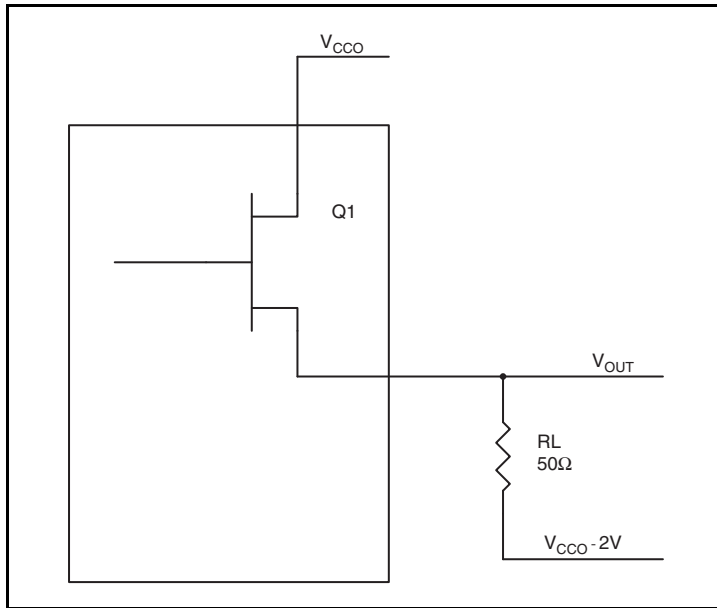
**Table 6. Thermal Resistance  $\theta_{JA}$  for 48 Lead TQFP, Forced Convection**

$\theta_{JA}$ by Velocity			
Linear Feet per Minute	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	$27.6^\circ C/W$	$22.6^\circ C/W$	$20.78^\circ C/W$

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 5*.



**Figure 5. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$   
 $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$   
 $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{30mW}$



## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 48 Lead TQFP, E-Pad**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	<b>0</b>	<b>200</b>	<b>500</b>
Multi-Layer PCB, JEDEC Standard Test Boards	27.6°C/W	22.6°C/W	20.78°C/W

## Transistor Count

The transistor count for 85352 is: 2252

# Package Outline and Package Dimensions

## Package Outline - Y Suffix for 48 Lead TQFP, E-Pad

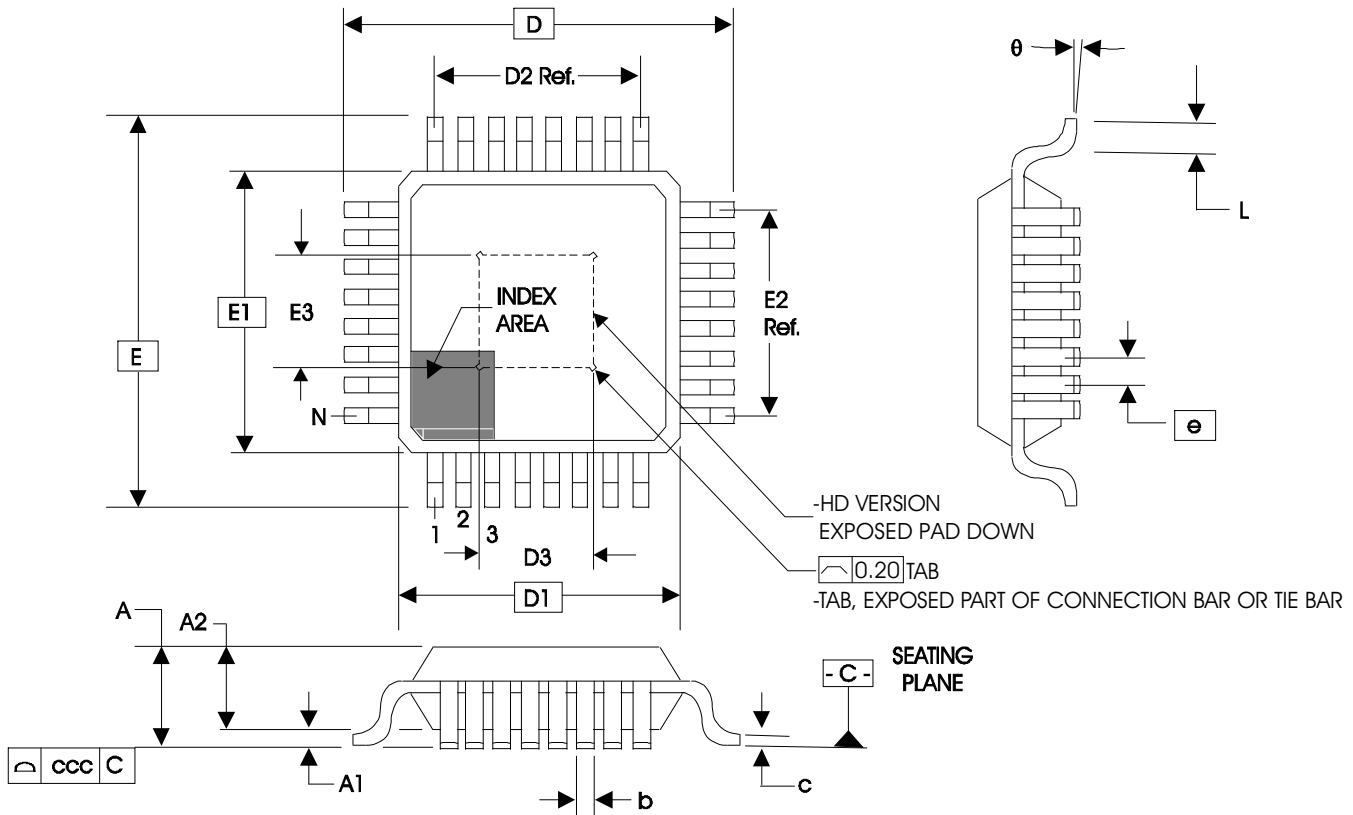


Table 8. Package Dimensions 48 Lead TQFP, E-Pad

JEDEC Variation: ABC - HD			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	48		
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.50 Ref.		
D3 & E3		3.5	
e	0.50 Basic		
L	0.45	0.60	0.75
theta	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

**Table 9. Ordering Information Table**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
85352AYILF	ICS85352AYIL	48 Lead TQFP, E-Pad, Lead-Free	Tray	-40°C to 85°C
85352AYILFT	ICS85352AYIL	48 Lead TQFP, E-Pad, Lead-Free	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	1	Features Section - added lead-free bullet.	7/6/06
		6	Added Recommendations for Unused Input and Output Pins.	
		7	Added Thermal Release Path.	
		15	Ordering Information Table - added lead-free part number, marking and note.	
B	T4A	3	Power Supply DC Characteristics Table - corrected $V_{CC}$ min. from 3.475V to 3.135V.	9/27/06
B	T4C T5A - T5B	3	Differential DC Characteristics Table - updates notes.	2/12/10
		4	AC Characteristics Tables - added thermal note.	
		7	Updated Wiring the Differential Input to Accept Single-ended Levels.	
	8	Updated EPAD Thermal Release Path.		
	9	Differential Clock input Interface - added Figure 3F.		
	12	Termination for 3.3V LVPECL Outputs - updated Figures 4A & 4B.		
T8 T9	15	Power Considerations - re-calculated ambient temperature using 0 air flow.		
	16	Updated Package Dimensions Table. Ordering Information Table - deleted "ICS" prefix from Part/Order Number		
B		16	Updated Package Outline.	3/9/10
B			Corrected title of datasheet from clock generator to clock buffer.	7/6/10
C	T5A - T5B	1	Features, corrected Propagation Delay bullet from 1.8ns to 2ns maximum.	8/3/10
		4	AC Characteristics Tables - added Additive Phase Jitter spec.	
	5	Added Additive Phase Jitter Plot.		
T8	17	Package Dimensions, corrected D3/E3 dimensions.		
D	T9	1	Features section - updated package bullet.	12/1/15
		18	Ordering Information Table - deleted leaded part rows and note. Deleted "ICS" prefix & "I" suffix from part number. Updated header/footer to new format.	



Corporate Headquarters  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

Sales  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
[www.IDT.com/go/sales](http://www.IDT.com/go/sales)

Tech Support  
[www.idt.com/go/support](http://www.idt.com/go/support)

DISCLAIMER Integrated Device Technology, Inc. (IDT) reserves the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners.

For datasheet type definitions and a glossary of common terms, visit [www.idt.com/go/glossary](http://www.idt.com/go/glossary).

Copyright ©2015 Integrated Device Technology, Inc. All rights reserved.