

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



# FAST CMOS BUFFER/CLOCK DRIVER

**IDT49FCT805BT/CT**

## FEATURES:

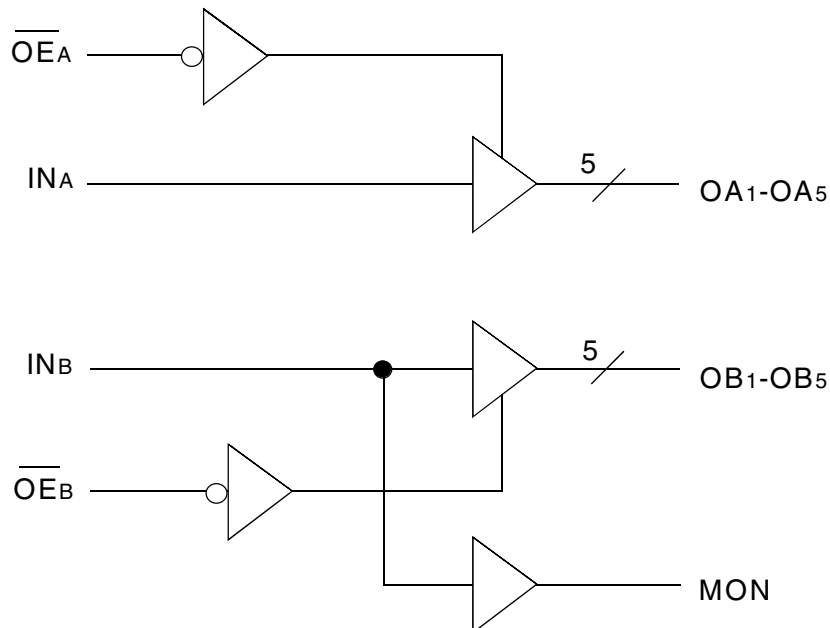
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 600ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: -32mA  $I_{OH}$ , +48mA  $I_{OL}$
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in the following packages:
  - Commercial: QSOP, SOIC, SSOP
  - Military: CERDIP, LCC

## DESCRIPTION:

This buffer/clock driver is built using advanced dual metal CMOS technology. The FCT805T is a non-inverting clock driver consisting of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. This part has extremely low output skew, pulse skew, and package skew. The device has a "heart-beat" monitor for diagnostics and PLL driving. The monitor output is identical to all other outputs and complies with the output specifications in this document.

The FCT805T is designed for fast, clean edge rates to provide accurate clock distribution in high speed systems.

## FUNCTIONAL BLOCK DIAGRAM

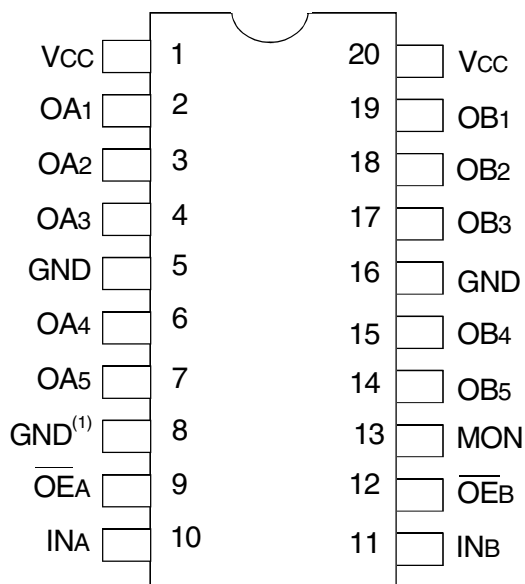


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

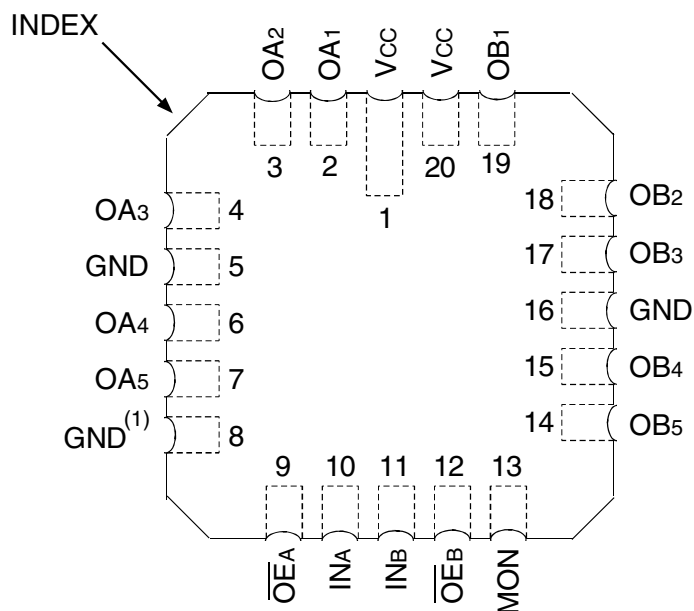
MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 2010

## PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ CERDIP  
TOP VIEW



LCC  
TOP VIEW

**NOTE:**

1. Pin 8 is internally connected to GND. To insure compatibility with all products, pin 8 should be connected to GND at the board level.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
COUT	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF

**NOTE:**

1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
OEA, OEB	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAx, OBx	Clock Outputs
MON	Monitor Output

## FUNCTION TABLE (1)

Inputs		Outputs	
OEA, OEB	INA, INB	OAx, OBx	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

**NOTE:**

1. H = HIGH  
L = LOW  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ , Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (3-State Output Pins)	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$I_I$	Input HIGH Current	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-255	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA COM'L}$	2.4	3.3	—	V
			$I_{OH} = -24\text{mA MIL}$ $I_{OH} = -32\text{mA COM'L}^{(4)}$	2	3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA COM'L}$	—	0.3	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$
$V_H$	Input Hysteresis for all inputs	—		—	150	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or $V_{CC}$		—	5	500	$\mu\text{A}$

### NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5\text{V}$ ,  $+25^\circ\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition should not exceed one second.
5. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	1	2	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open OEA = OEB = GND 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	60	100	μA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>o</sub> = 25MHz 50% Duty Cycle OEA = OEB = V <sub>CC</sub> Mon. Output Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	1.5	3	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	1.8	4	
		V <sub>CC</sub> = Max. Outputs Open f <sub>o</sub> = 50MHz 50% Duty Cycle OEA = OEB = GND Eleven Outputs Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	33	55.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	33.5	57.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>C</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$   
 I<sub>CC</sub> = Quiescent Current (I<sub>CC1</sub>, I<sub>CC2</sub> and I<sub>CC3</sub>)  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>o</sub> = Output Frequency  
 N<sub>o</sub> = Number of Outputs at f<sub>o</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY<sup>(1,2)</sup>

Symbol	Parameter	Conditions <sup>(3)</sup>	FCT805BT		FCT805CT		Unit
			Min. <sup>(4)</sup>	Max.	Min. <sup>(4)</sup>	Max.	
t <sub>PLH</sub>	Propagation Delay	CL = 50pF RL = 500Ω	1.5	5.7	1.5	5.2	ns
t <sub>PHL</sub>	INA to OAx, INB to OBx		—	2	—	2	ns
t <sub>r</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>f</sub>	Output Fall Time		—	0.9	—	0.7	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.9	—	0.8	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	1.5	—	1.2	ns
tsk(PP)	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		1.5	6.5	1.5	6	ns
t <sub>PZL</sub>	Output Enable Time		1.5	6.5	1.5	6	ns
t <sub>PZH</sub>	○EA to OAx, ○EB to OBx						
t <sub>PLZ</sub>	Output Disable Time						
t <sub>PHZ</sub>	○EA to OAx, ○EB to OBx						

NOTES:

1. t<sub>PLH</sub>, t<sub>PHL</sub>, and tsk(pp) are production tested. All other parameters are guaranteed but not production tested.
2. Propagation delay range indicated by Min. and Max. limit is dues to Vcc, operating temperature, and process parameters. These propagation delay limits do not imply skew.
3. See Test Circuits and Waveforms.
4. Minimum limits are guaranteed but not tested on Propagation Delays.

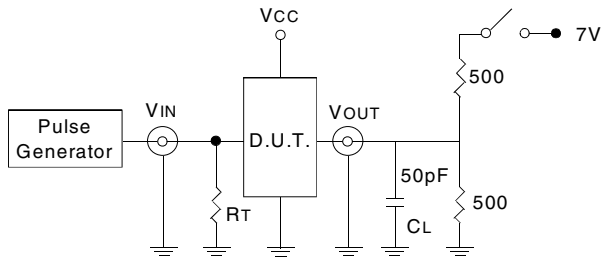
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL<sup>(1,2)</sup>

Symbol	Parameter	Conditions <sup>(3)</sup>	FCT805BT		FCT805CT		Unit
			Min. <sup>(4)</sup>	Max.	Min. <sup>(4)</sup>	Max.	
t <sub>PLH</sub>	Propagation Delay	CL = 50pF RL = 500Ω	1.5	5	1.5	4.5	ns
t <sub>PHL</sub>	INA to OAx, INB to OBx		—	1.5	—	1.5	ns
t <sub>r</sub>	Output Rise Time		—	1.5	—	1.5	ns
t <sub>f</sub>	Output Fall Time		—	0.7	—	0.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.6	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> - t <sub>PLH</sub>  )		—	1.2	—	1	ns
tsk(PP)	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		1.5	6	1.5	5	ns
t <sub>PZL</sub>	Output Enable Time		1.5	6	1.5	5	ns
t <sub>PZH</sub>	○EA to OAx, ○EB to OBx						
t <sub>PLZ</sub>	Output Disable Time						
t <sub>PHZ</sub>	○EA to OAx, ○EB to OBx						

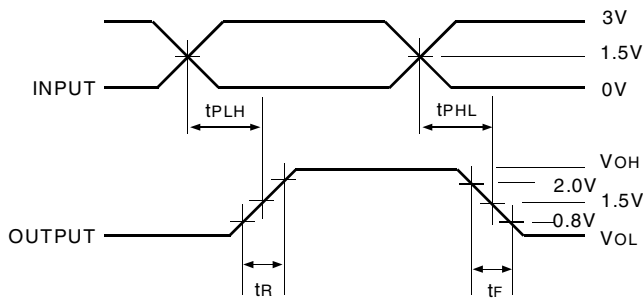
NOTES:

1. t<sub>PLH</sub>, t<sub>PHL</sub>, and tsk(pp) are production tested. All other parameters are guaranteed but not production tested.
2. Propagation delay range indicated by Min. and Max. limit is dues to Vcc, operating temperature, and process parameters. These propagation delay limits do not imply skew.
3. See Test Circuits and Waveforms.
4. Minimum limits are guaranteed but not tested on Propagation Delays.

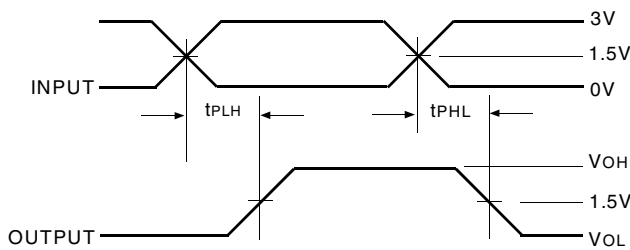
## TEST CIRCUITS AND WAVEFORMS



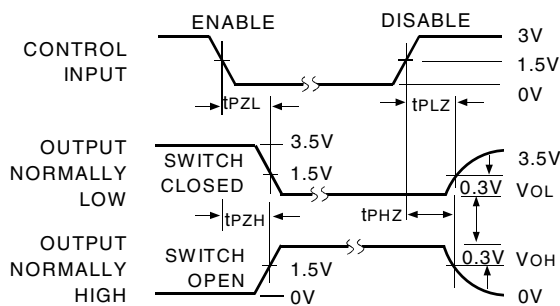
Test Circuits for All Outputs



Package Delay



$t_{SK(P)} = |t_{PHL} - t_{PLH}|$   
Pulse Skew -  $t_{SK(P)}$



Enable and Disable Times

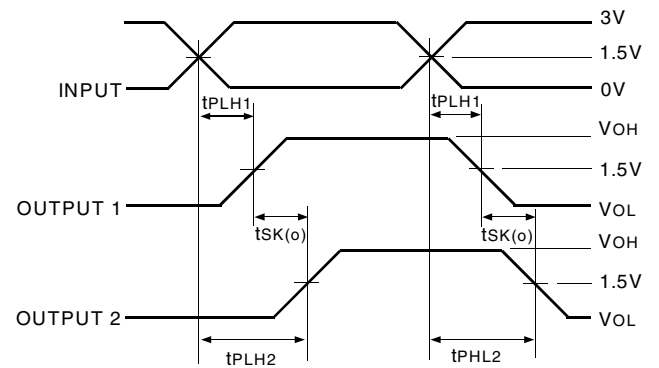
- NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
  2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$

## SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	GND

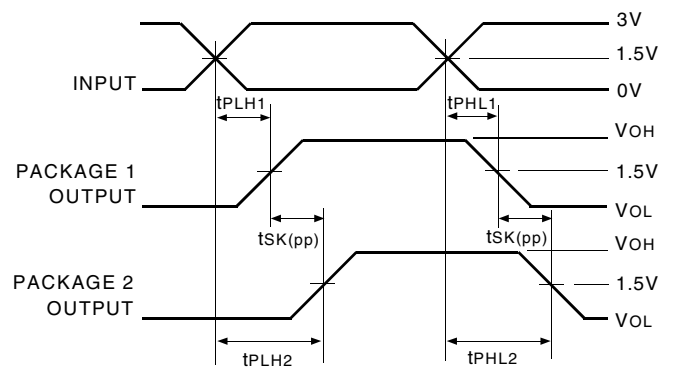
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Zout of the Pulse Generator.



$$t_{SK(o)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew



$$t_{SK(pp)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Part-to-Part Skew -  $t_{SK(PP)}$

### NOTE:

1. Package 1 and Package 2 are same device type and speed grade.

ORDERING INFORMATION

49FCT	XXXX	XX	X		
	Device Type	Package	Process		
				Blank	Commercial (0°C to +70°C)
				B	MIL-STD-883, Class B (-55°C to +125°C)
					<u>Commercial Options</u>
				SOG	SOIC - Green
				QG	QSOP - Green
				PYG	SSOP - Green
					<u>Military Options</u>
				D	CERDIP
				L	Leadless Chip Carrier
				805BT	Fast CMOS Buffer/Clock Driver
				805CT	



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
clockhelp@idt.com