

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

BUFFER/CLOCK DRIVER

ICSLV810

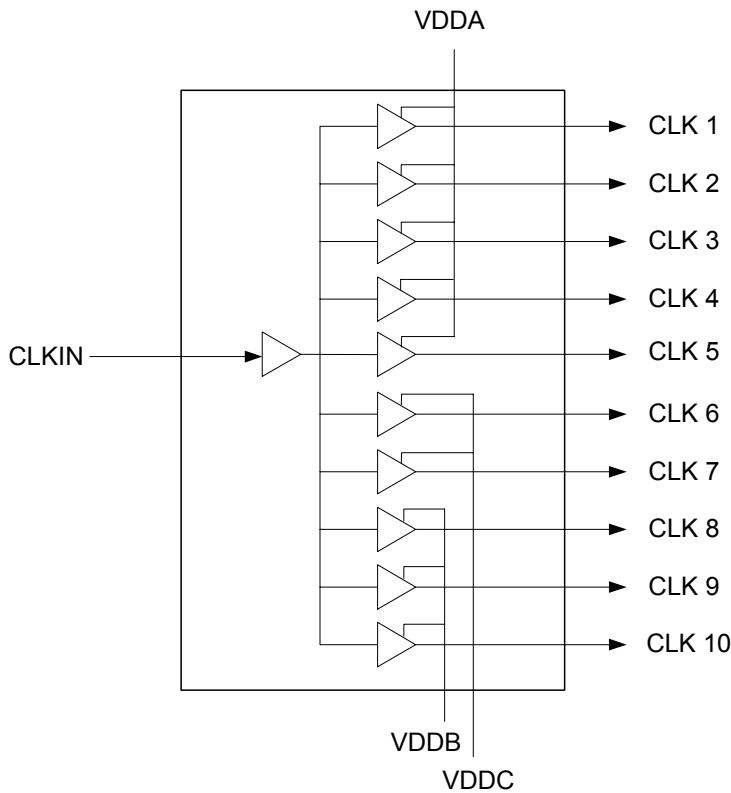
Description

The ICSLV810 is a low skew 1.5 V to 2.5 V, 1:10 fanout buffer. This device is specifically designed for data communications clock management. The large fanout from a single input line reduces loading on the input clock. The TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

Features

- Packaged in 20-pin QSOP/SSOP
- Split 1:10 fanout Buffer
- Maximum skew between outputs of different packages 0.75 ns
- Max propagation delay of 3.8 ns
- Operating voltage of 1.5 V to 2.5 V on Bank A
- Operating voltage of 1.5 V to 2.5 V on Banks B and C
- Advanced, low power, CMOS process
- Industrial temperature range -40° C to +85° C
- 3.3 V tolerant input when VDDA=2.5 V
- Pb (lead) free packaging

Block Diagram



Pin Assignment

| | | | |
|-------|----|----|--------|
| CLKIN | 1 | 20 | VDDB |
| GND | 2 | 19 | CLK 10 |
| CLK 1 | 3 | 18 | CLK 9 |
| VDDA | 4 | 17 | GND |
| CLK 2 | 5 | 16 | CLK 8 |
| GND | 6 | 15 | VDDC |
| CLK 3 | 7 | 14 | CLK 7 |
| VDDA | 8 | 13 | GND |
| CLK 4 | 9 | 12 | CLK 6 |
| GND | 10 | 11 | CLK 5 |

20 pin (150mil) SSOP

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---------------------------|
| 1 | CLKIN | Input | Clock input. |
| 2 | GND | Power | Connect to ground. |
| 3 | CLK1 | Output | Clock output. |
| 4 | VDDA | Power | Connect to +1.5 - +2.5 V. |
| 5 | CLK2 | Output | Clock output. |
| 6 | GND | Power | Connect to ground. |
| 7 | CLK3 | Output | Clock output. |
| 8 | VDDA | Power | Connect to +1.5 - +2.5 V. |
| 9 | CLK4 | Output | Clock output. |
| 10 | GND | Power | Connect to ground. |
| 11 | CLK5 | Output | Clock output. |
| 12 | CLK6 | Output | Clock output. |
| 13 | GND | Power | Connect to ground. |
| 14 | CLK7 | Output | Clock output. |
| 15 | VDDC | Power | Connect to +1.5 - 2.5 V. |
| 16 | CLK8 | Output | Clock output. |
| 17 | GND | Power | Connect to ground. |
| 18 | CLK9 | Output | Clock output. |
| 19 | CLK10 | Output | Clock output. |
| 20 | VDDB | Power | Connect to +1.5 - 2.5 V. |

External Components

The ICSLV810 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μ F must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance) place a 33 Ω resistor in series with the clock line,

as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) The 0.01 μ F decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.
- 2) To minimize EMI the 33 Ω series termination resistor, if needed, should be placed close to the clock output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICSLV810. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|------------------------|
| Supply Voltage, VDD MAX | 7 V |
| All Inputs and Outputs | -0.5 V to VDDA + 1.2 V |
| Ambient Operating Temperature | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage (measured with respect to GND), VDDA | 1.425 | | 2.625 | V |
| Power Supply Voltage (measured with respect to GND), VDDB | 1.425 | | 2.625 | V |
| Power Supply Voltage (measured with respect to GND), VDDC | 1.425 | | 2.625 | V |

DC Electrical Characteristics—CLKIN and Bank A

VDDA = 2.5 V, Ambient Temperature -40° C to +85° C

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|--------------------------------|------------------|--|-----------------------------|-------|------|-------|-------|
| Operating Voltage | VDDA | | | 1.425 | | 2.625 | V |
| Quiescent Power Supply Current | IDDA | No Load F = 40 MHz | | | 15 | | mA |
| Short Circuit Current | I _{OS} | CLK 1 - 5 | | | ±80 | | mA |
| Input High Voltage, CLKIN | V _{IH} | Guaranteed Logic Level High | | 1.6 | | | V |
| Input Low Voltage, CLKIN | V _{IL} | Guaranteed Logic Level Low | | | | 0.8 | V |
| Output High Voltage | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.8 | | | V |
| Output Low Voltage | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 12 mA | | | 0.4 | V |
| Input High Current | I _{IH} | VDD = max | V _{IN} = 2.4 V | | | 1 | μA |
| Input Low Current | I _{IL} | VDD = max | V _{IN} = 0.5 V | | | -1 | μA |
| Input High Current | I _I | VDD = max | V _{IN} = VDD (max) | | | 20 | μA |
| Input Capacitance | C _{IN} | V _{IN} = 0V, Note1 | | | 5 | 6.0 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} = 0V, Note1 | | | 5.5 | 8.0 | pF |

Note1: This parameter is not tested, guaranteed by design.

DC Electrical Characteristics—Bank B

VDDB = 2.5 V, Ambient Temperature -40° C to +85° C, unless otherwise noted

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|--------------------------------|-----------------|---------------------------------------|---------|-------|------|-------|-------|
| Operating Voltage | VDDB | | | 1.425 | | 2.625 | V |
| Quiescent Power Supply Current | IDDB | VDDB = 2.5 V No Load F = 40 MHz | | | 7 | | mA |
| | | VDDB = 1.5 V No Load F = 40 MHz | | | 3 | | mA |
| Short Circuit Current | I _{OS} | VDDB = 1.5 V | CLK8-10 | | ±35 | | mA |
| | | VDDB = 2.5 V | CLK8-10 | | ±80 | | mA |

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|---------------------|------------------|--|-------------------------|------|------|------|-------|
| Output High Voltage | V _{OH} | V _{DDB} = 1.5 V V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.1 | | | V |
| | | V _{DDB} = 2.5 V V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.8 | | | V |
| Output Low Voltage | V _{OL} | V _{DDB} = 1.5 V V _{IN} = V _{IH} or V _{IL} | I _{OL} = 12 mA | | | 0.42 | V |
| | | V _{DDB} = 2.5 V V _{IN} = V _{IH} or V _{IL} | I _{OL} = 12 mA | | | 0.4 | V |
| Input High Current | I _{IH} | V _{DDB} = max | | | | 1 | μA |
| Input Low Current | I _{IL} | V _{DDB} = max | | | | -1 | μA |
| Input High Current | I _I | V _{DDB} = max, V _{IN} = V _{DD} (max) | | | | 20 | μA |
| Input Capacitance | C _{IN} | V _{IN} = 0V, Note1 | | | 5 | 6.0 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} = 0V, Note 1 | | | 5.5 | 8.0 | pF |

Note1: This parameter is not tested, guaranteed by design.

DC Electrical Characteristics—Bank C

V_{DDC} = 2.5 V, Ambient Temperature -40° C to +85° C, unless otherwise noted

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|--------------------------------|------------------|--|-------------------------|-------|------|-------|-------|
| Operating Voltage | V _{DDC} | | | 1.425 | | 2.625 | V |
| Quiescent Power Supply Current | I _{DDC} | V _{DDC} = 2.5 V No Load F = 40 MHz | | | 3 | | mA |
| | | V _{DDC} = 1.5 V No Load F = 40 MHz | | | 2 | | mA |
| Short Circuit Current | I _{OS} | V _{DDC} = 1.5 V | CLK6-7 | | ±35 | | mA |
| | | V _{DDC} = 2.5 V | CLK6-7 | | ±80 | | mA |
| Output High Voltage | V _{OH} | V _{DDC} = 1.5 V V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.1 | | | V |
| | | V _{DDC} = 2.5 V V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.8 | | | V |
| Output Low Voltage | V _{OL} | V _{DDC} = 1.5 V V _{IN} = V _{IH} or V _{IL} | I _{OL} = 12 mA | | | 0.42 | V |
| | | V _{DDC} = 2.5 V V _{IN} = V _{IH} or V _{IL} | I _{OL} = 12 mA | | | 0.4 | V |
| Input High Current | I _{IH} | V _{DDC} = max | | | | 1 | μA |
| Input Low Current | I _{IL} | V _{DDC} = max | | | | -1 | μA |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------|------------------|--|------|------|------|-------|
| Input High Current | I _I | V _{DDC} = max, V _{IN} = V _{DD} (max) | | | 20 | μA |
| Input Capacitance | C _{IN} | V _{IN} = 0V, Note1 | | 5 | 6.0 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} = 0V, Note 1 | | 5.5 | 8.0 | pF |

Note1: This parameter is not tested, guaranteed by design.

AC Electrical Characteristics—Bank A

V_{DDA} = 2.5 V, Ambient Temperature -40° C to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-------------------------------------|-------------------------------------|------|------|------|-------|
| Output Skew: skew between outputs of same package | t _{SK(O)} | CL = 3 pF, RL = 500Ω Figure 3 | -200 | | 200 | ps |
| Pulse Skew: skew between opposite transitions of same output (t _{PLH} -t _{PHL}) | t _{SK(P)} | CL = 3 pF, RL = 500Ω Figure 4 | -200 | | 200 | ps |
| Propagation Delay | t _{pLH} / t _{pHL} | CL = 3 pF, RL = 500Ω Figure 2 | 1.5 | 2.6 | 3.5 | ns |
| Part to Part Skew | t _{SK(t)} | CL = 3 pF, RL = 500Ω Figure 5 | -650 | | 650 | ps |
| Output Rise Time 20% to 80% | t _{r(o)} | CL = 3 pF, RL = 500Ω | | 0.8 | | ns |
| Output Fall Time 80% to 20% | t _{f(o)} | CL = 3 pF, RL = 500Ω | | 0.8 | | ns |
| Additive Jitter | t _J | All Outputs | | | 50 | ps |
| Duty Cycle Measured at V _{DD} /2 | DC | CL = 3 pF, RL = 500Ω | 45 | | 55 | % |
| Duty Cycle, V _{DDA} =1.8V | DC | | 40 | 50 | 60 | % |
| Output Frequency Range | | | 1 | | 133 | MHz |

AC Electrical Characteristics—Bank B

VDDB = 2.5 V, Ambient Temperature -40° C to +85° C, unless otherwise noted

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------------|---|------|------|------|-------|
| Output Skew: skew between outputs of same package | $t_{SK(O)}$ | CL = 3 pF, RL = 500Ω Figure 3 | -200 | | 200 | ps |
| Pulse Skew: skew between opposite transitions of same output (tPLH-tPHL) | $t_{SK(P)}$ | CL = 3 pF, RL = 500Ω Figure 4 | -200 | | 200 | ps |
| Propagation Delay | t_{pLH} / t_{pHL} | CL = 3 pF, RL = 500Ω, VDDB = 1.5 V Figure 2 | | 5.5 | | ns |
| | | CL = 3 pF, RL = 500Ω, VDDB = 2.5 V Figure 2 | 1.5 | 2.6 | 3.5 | ns |
| Part to Part Skew | | CL = 3 pF, RL = 500Ω VDDB = 1.5 V Figure 5 | -1 | | 1 | ns |
| | | CL = 3 pF, RL = 500Ω VDDB = 2.5 V Figure 5 | -650 | | 650 | ps |
| Output Rise Time 20% to 80% | $t_{r(O)}$ | CL = 3 pF, RL = 500Ω VDDB = 1.5 V | | 1.0 | | ns |
| | | CL = 3 pF, RL = 500Ω VDDB = 2.5 V | | 0.8 | | ns |
| Output Fall Time 80% to 20% | $t_{f(O)}$ | CL = 3 pF, RL = 500Ω VDDB = 1.5 V | | 1.0 | | ns |
| | | CL = 3 pF, RL = 500Ω VDDB = 2.5 V | | 0.8 | | ns |
| Additive Jitter | t_J | All Outputs, VDDB = 1.5 V | | | 34 | ps |
| | | All Outputs, VDDB = 2.5 V | | | 50 | ps |
| Duty Cycle Measured at VDD/2 | DC | CL = 3 pF, RL = 500Ω | 45 | | 55 | % |
| Duty Cycle, VDDB = 1.8V | DC | | 40 | 50 | 60 | % |
| Output Frequency Range | | | 1 | | 133 | MHz |

AC Electrical Characteristics—Bank C

VDDC = 2.5 V, Ambient Temperature -40° C to +85° C, unless otherwise noted

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------------|--|------|------|------|-------|
| Output Skew: skew between outputs of same package | $t_{SK(O)}$ | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ Figure 3 | -200 | | 200 | ps |
| Pulse Skew: skew between opposite transitions of same output (tPLH-tPHL) | $t_{SK(P)}$ | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ Figure 4 | -200 | | 200 | ps |
| Propagation Delay | t_{pLH} / t_{pHL} | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$, VDDC = 1.5 V Figure 2 | | 5.5 | | ns |
| | | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$, VDDC = 2.5 V Figure 2 | 1.5 | 2.6 | 3.5 | ns |
| Part to Part Skew | | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ VDDC = 1.5 V Figure 5 | -1 | | 1 | ns |
| | | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ VDDC = 2.5 V Figure 5 | -650 | | 650 | ps |
| Output Rise Time 20% to 80% | $t_{r(O)}$ | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ VDDC = 1.5 V | | 1.0 | | ns |
| | | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ VDDC = 2.5 V | | 0.8 | | ns |
| Output Fall Time 80% to 20% | $t_{f(O)}$ | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ VDDC = 1.5 V | | 1.0 | | ns |
| | | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ VDDC = 2.5 V | | 0.8 | | ns |
| Additive Jitter | t_J | All Outputs, VDDC = 1.5 V | | | 34 | ps |
| | | All Outputs, VDDC = 2.5 V | | | 50 | ps |
| Duty Cycle Measured at VDD/2 | DC | $C_L = 3 \text{ pF}$, $R_L = 500\Omega$ | 45 | | 55 | % |
| Duty Cycle, VDDC=1.8V | DC | | 40 | 50 | 60 | % |
| Output Frequency Range | | | 1 | | 133 | MHz |

Thermal Characteristics for 20QSOP

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 135 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 93 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 78 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 60 | | °C/W |

Thermal Characteristics for 20SOIC

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 83 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 71 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 58 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 46 | | °C/W |

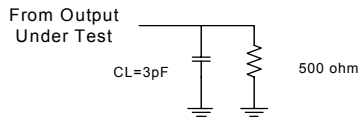


Figure 1. Load Circuit

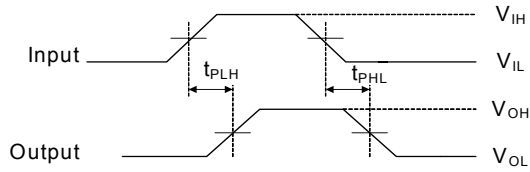
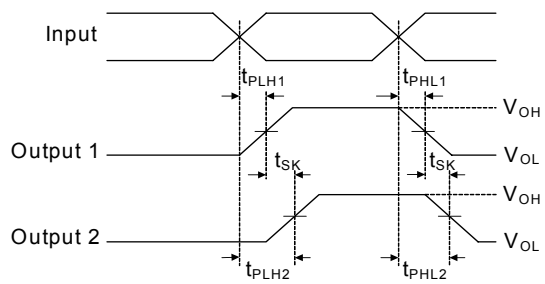


Figure 2. Propagation Delay



($t_{SK(O)} = |t_{PLH2} - t_{PHL2}|$ or $|t_{PLH1} - t_{PHL1}|$)

Figure 3. Output Skew

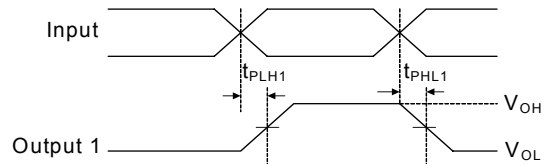
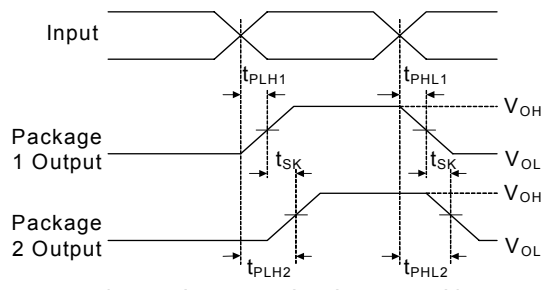


Figure 4. Pulse Skew ($t_{SK(p)} = |t_{pLH} - t_{pHl}|$)

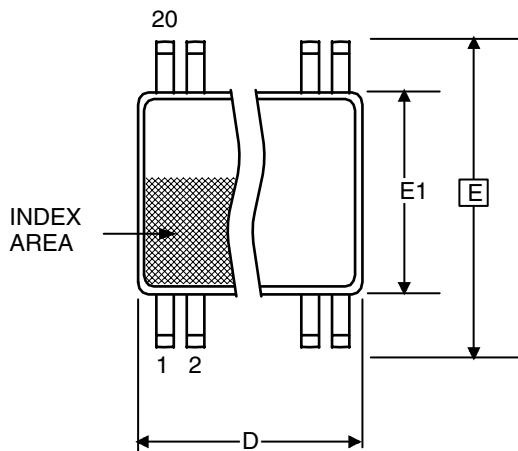


($t_{SK(O)} = |t_{PLH2} - t_{PHL2}|$ or $|t_{PLH1} - t_{PHL1}|$)

Figure 5. Part-to-Part Skew

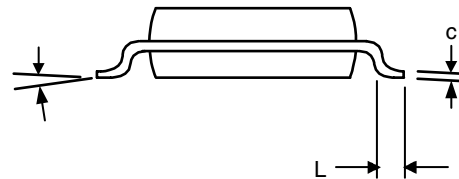
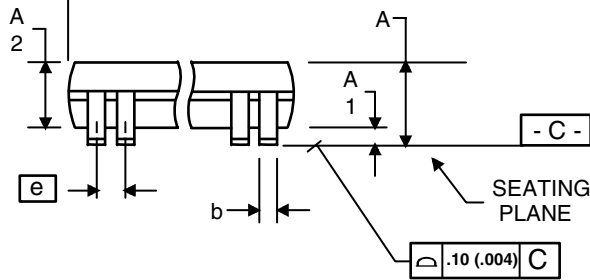
Package Outline and Package Dimensions (20-pin QSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



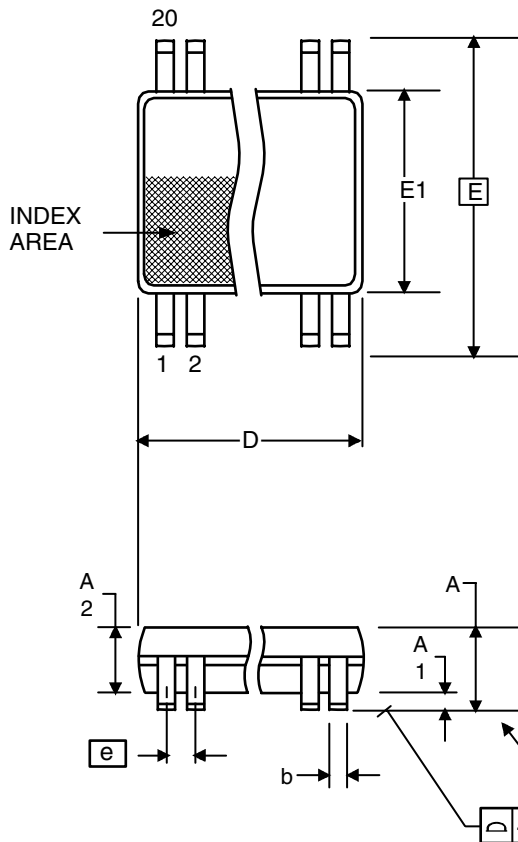
| Symbol | Millimeters | | Inches* | |
|----------|-------------|------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .0040 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| C | 0.18 | 0.25 | .007 | .010 |
| D | 8.55 | 8.75 | .337 | .344 |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 Basic | | 0.025 Basic | |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.



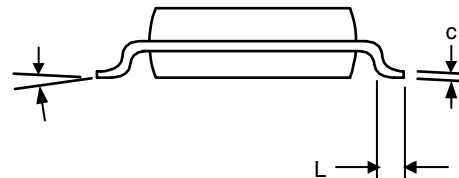
Package Outline and Package Dimensions (20-pin SSOP, 209 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|----------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | — | 2.00 | — | .079 |
| A1 | 0.05 | — | .002 | — |
| A2 | 1.65 | 1.85 | .065 | .073 |
| b | 0.22 | 0.38 | 0.009 | 0.015 |
| c | 0.09 | 0.25 | .0035 | .010 |
| D | 6.90 | 7.50 | .271 | .295 |
| E | 7.40 | 8.20 | .291 | .323 |
| E1 | 5.00 | 5.60 | .197 | .220 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.55 | 0.95 | .022 | .037 |
| α | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-----------|--------------------|-------------|---------------|
| LV810RILF | LV810RILF | Tubes | 20-pin QSOP | -40 to +85° C |
| LV810RILFT | LV810RILF | Tape and Reel | 20-pin QSOP | -40 to +85° C |
| LV810FILF | LV810FILF | Tubes | 20-pin SSOP | -40 to +85° C |
| LV810FILFT | LV810FILF | Tape and Reel | 20-pin SSOP | -40 to +85° C |

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

| Rev. | Originator | Date | Description of Change |
|------|--------------|----------|--|
| A | P.Griffith | 03/25/05 | New device/datasheet. |
| B | P.Griffith | 05/02/05 | Released from Preliminary to final; changed Short Circuit Current parameter in 2.5 V DC Char table to ± 80 mA; changed Short Circuit Current parameter in 1.5 V DC Char table to ± 35 mA |
| C | P.Griffith | 05/12/05 | Added bullet in "Features" for operating voltage of 2.5 V on Bank A and specified that operating voltages of 1.5 and 2.5 V are on Banks B and C; changed block diagram input and pin 1 from IN to CLKIN; removed +1.5 V spec from pin 4 and pin 8 descriptions; added "VDDA + 1.2 V" to "All Inputs and Outputs" section of Absolute Maximum Ratings; added min and max values for Banks A, B, and C "Power Supply Voltage" in Recommended Operating Conditions; expanded DC Electrical Char tables in to include a separate table for Banks A, B, and C; expanded AC Electrical Char tables in to include a separate table for Banks A, B, and C; |
| D | P.Griffith | 06/21/05 | Added 209 mil 20-pin SSOP package and ordering info. |
| E | K. Beckmeyer | 07/27/05 | Specified operating voltage on Bank A from 1.5V to 2.5V; Added figures 4 and 5 on page 10 to explain Pulse Skew and Part-to-Part Skew; Changed Output Frequency Max Specification to 133MHz in AC Electrical Char tables for Banks A, B, and C; Added Duty Cycle Spec for VDD = 1.5V in AC Electrical Char tables for Banks A, B, C; Changed CLK conditions in DC Electrical Char tables on Banks B and C; removed SOIC package. |
| F | K. Beckmeyer | 10/13/05 | Added "LF" packaging and ordering info to both "R" and "F" packages. |
| G | | 12/17/09 | Added EOL note for non-green parts. |
| H | | 05/13/10 | Removed EOL note and non-green orderables. |

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com