

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NB3H83905C

1.8V/2.5V/3.3V Crystal Input to 1:6 LVTTTL/LVCMOS Clock Fanout Buffer with OE

Description

The NB3H83905C is a 1.8 V, 2.5 V or 3.3 V V_{DD} core Crystal input to 1:6 LVTTTL/LVCMOS fanout buffer with outputs powered by flexible 1.8 V, 2.5 V, or 3.3 V supply V_{DDO} (with $V_{DD} \geq V_{DDO}$). The device accepts a fundamental Parallel Resonant crystal from 3 MHz to 40 MHz or a single-ended LVCMOS Clock from up to 100 MHz.

Two synchronous LVTTTL/LVCMOS Enable lines permit independent control over outputs BCLK[0:4] and output BCLK5; enabling or disabling only when the output is in LOW state eliminating potential output glitching or runt pulse generation. When unused, leave floating open, pins will default to HIGH state.

The 6 outputs drive 50 Ω series or parallel terminated transmission lines. Parallel termination should be to $1/2 V_{CC}$. Series terminated lines can drive 2 loads each, or 12 lines total.

Fit, Form, and Function compatible with ICS83905 and PI6C10806.

Features

- Six Copies of LVTTTL/LVCMOS Output Clock
- Supply Operation $V_{DD} \geq V_{DDO}$:
 - ◆ 1.8 V ± 0.2 V, 2.5 V $\pm 5\%$ or 3.3 V $\pm 5\%$ Core V_{DD}
 - ◆ 1.8 V ± 0.2 V, 2.5 V $\pm 5\%$, or 3.3 V $\pm 5\%$ Output V_{DDO}
- Crystal Oscillator Interface
- Crystal Input Frequency Range: 3 MHz to 40 MHz
- Clock Input Frequency Range: Up to 100 MHz
- LVCMOS compatible Enable Inputs
- 5 V Tolerant Enable Inputs
- Low Output to Output Skew: 80 ps Max
- Synchronous Output Enable
- Phase Noise Floor -160 dBc (1 MHz)
- Industrial Temperature Range
- These are Pb-Free Devices

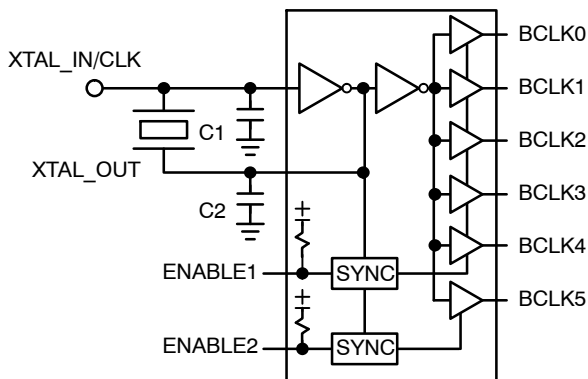


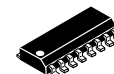
Figure 1. Simplified Block Diagram



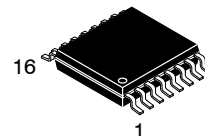
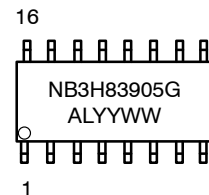
ON Semiconductor®

<http://onsemi.com>

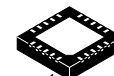
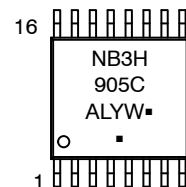
MARKING DIAGRAMS*



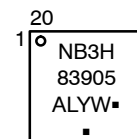
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



QFN20
MN SUFFIX
CASE 485BH



A = Assembly Location
L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(*Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NB3H83905C

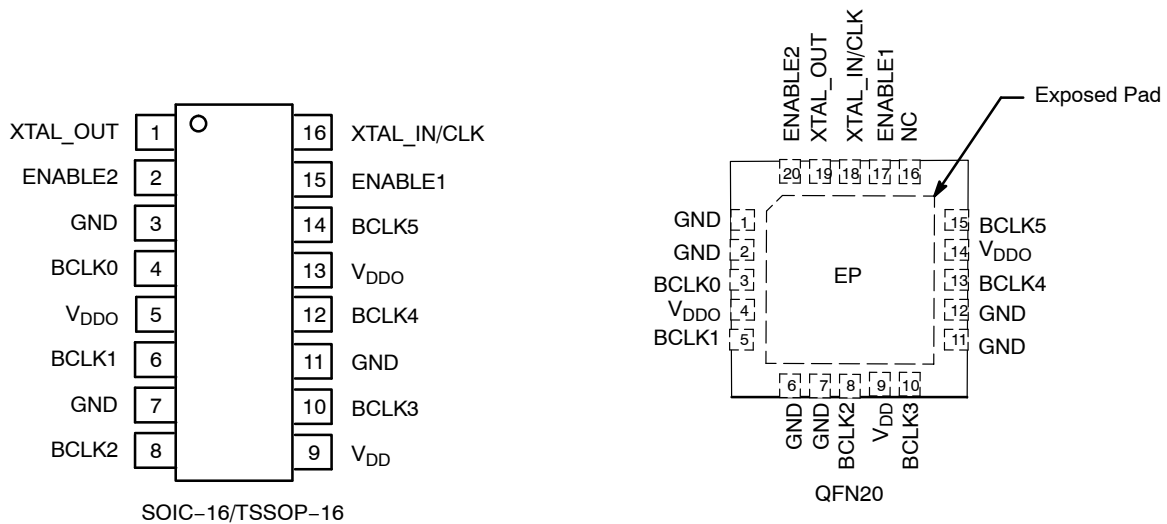


Figure 2. Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

SOIC-16 / TSSOP-16	QFN-20	Name	I/O	Description
1	19	XTAL_OUT	Crystal Interface	Oscillator Output to drive Crystal
2	20	ENABLE 2	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK5 Output. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to V _{CC} .
3, 7, 11	1, 2, 6, 7, 11, 12	GND	GND	GND Supply pins. All GND, V _{DD} and V _{DDO} pins must be externally connected to power supply to guarantee proper operation.
4, 6, 8, 10, 12, 14	3, 5, 8, 10, 13, 15	BCLK0, 1, 2, 3, 4, 5	LVCMOS Outputs	Buffered Clock Outputs
5, 13	4, 14	V _{DDO}	POWER	Positive Supply voltage for outputs. All GND, V _{DD} and V _{DDO} pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
9	9	V _{DD}	POWER	Positive Supply voltage for core. All GND, V _{DD} and V _{DDO} pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
-	16	NC		No Connect
15	17	ENABLE 1	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK0/1/2/3/4 Output block. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to V _{CC}
16	18	XTAL_IN/CLK	Crystal Interface	Oscillator Input from Crystal. Single ended Clock Input.
-	EP		-	The Exposed Pad (EP) on the QFN-20 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

Table 2. CLOCK ENABLE FUNCTION TABLE

Control Inputs		Outputs	
ENABLE1*	ENABLE2*	BCLK0:BCLK4	BCLK5
0	0	LOW	LOW
0	1	LOW	Toggling
1	0	Toggling	LOW
1	1	Toggling	Toggling

*Defaults HIGH when floating open.

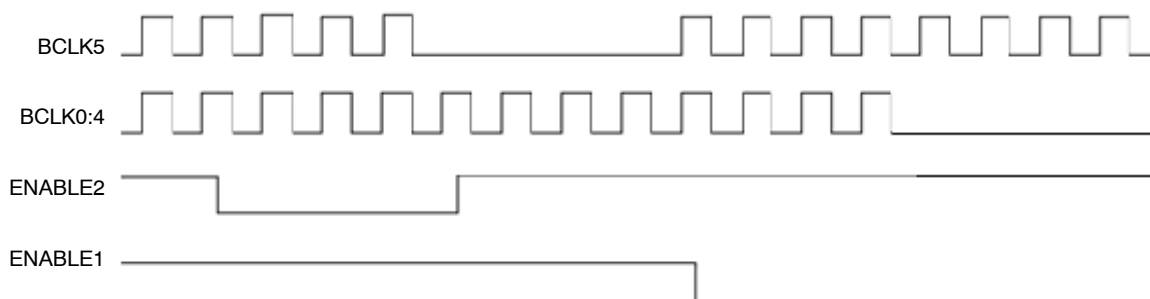


Figure 3. ENABLEx Control Timing Diagram

The ENABLEx control inputs will synchronously enable or disable the selected output(s). This control detects the falling edge of the internal signal and asserts or de-asserts the output after 3 clock cycles. When ENABLEx is LOW, the outputs are disabled to a LOW state. When ENABLEx is HIGH, the outputs are enabled to toggle.

Table 3. RECOMMENDED CRYSTAL PARAMETERS

Crystal	Fundamental AT-Cut
Frequency	10 to 40 MHz
Load Capacitance*	16–20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Drive Level	1 mW

*See APPLICATION INFORMATION; Crystal Input Interface for CL loading

Table 4. ATTRIBUTES (Note 1)

Characteristics	Value
ESD Protection Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index	UL-94 code V-0 A 1/8" 28 to 34
Transistor Count	213 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

NB3H83905C

Table 5. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 1	Rating	Unit
V _{DDx}	Positive Power Supply	GND = 0 V		4.6	V
V _I	Input Voltage			-0.5 ≤ V _I ≤ V _{DD} + 0.5	V
T _A	Operating Temperature Range, Industrial			-40 to ≤ +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-16 SOIC-16	80 55	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 3)	SOIC-16	33-36	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-16 TSSOP-16	138 108	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 3)	TSSOP-16	33-36	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-20 QFN-20	47 33	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 3)	QFN-20	18	°C/W
T _{sol}	Wave Solder	3 sec @ 248°C		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

NB3H83905C

Table 6. DC CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{DD} = V_{DDO} = 3.135\text{ V to }3.465\text{ V (}3.3\text{ V} \pm 5\%); GND = 0\text{ V, }T_A = -40^\circ\text{C to }+85^\circ\text{C}$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			5	mA
V _{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	2		V _{DD} + 0.3 V	V
V _{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	-0.3		0.8	V
V _{OH}	Output HIGH Voltage (Note 4)	2.6			V
V _{OL}	Output LOW Voltage (Note 4)			0.5	V
C _{IN}	Input Capacitance		4		pF
C _{PD}	Power Dissipation Capacitance (per Output) (Note 4)		19		pF
R _{OUT}	Output Impedance (Note 4)		7		Ω

$V_{DD} = V_{DDO} = 2.375\text{ V to }2.625\text{ V (}2.5\text{ V} \pm 5\%); GND = 0\text{ V, }T_A = -40^\circ\text{C to }+85^\circ\text{C}$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			8	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			4	mA
V _{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	1.7		V _{DD} + 0.3 V	V
V _{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	-0.3		0.7	V
V _{OH}	Output HIGH Voltage (I _{OH} = -1 mA) Output HIGH Voltage (Note 4)	2.0 1.8			V
V _{OL}	Output LOW Voltage (I _{OL} = 1 mA) Output LOW Voltage (Note 4)			0.4 0.45	V
C _{IN}	Input Capacitance		4		pF
C _{PD}	Power Dissipation Capacitance (per Output) (Note 4)		18		pF
R _{OUT}	Output Impedance (Note 4)		7		Ω

$V_{DD} = V_{DDO} = 1.6\text{ V to }2.0\text{ V (}1.8\text{ V} \pm 0.2\text{ V); GND = 0\text{ V, }T_A = -40^\circ\text{C to }+85^\circ\text{C}$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			5	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V _{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	0.65*V _{DD}		V _{DD} + 0.3 V	V
V _{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	-0.3		0.35*V _{DD}	V
V _{OH}	Output HIGH Voltage (Note 4)	V _{DDO} -0.3			V
V _{OL}	Output LOW Voltage (Note 4)			0.35	V
C _{IN}	Input Capacitance		4		pF
C _{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R _{OUT}	Output Impedance (Note 4)		10		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to V_{DDO}/2 (see Figure 5).

NB3H83905C

Table 6. DC CHARACTERISTICS (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} = 3.135 V to 3.465 V (3.3 V ± 5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V ± 5%); GND = 0 V, T_A = -40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			4	mA
V _{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	2		V _{DD} + 0.3 V	V
V _{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	-0.3		0.8	V
V _{OH}	Output HIGH Voltage (I _{OH} = -1 mA) Output HIGH Voltage (Note 4)	2.0 1.8			V
V _{OL}	Output LOW Voltage (I _{OL} = 1 mA) Output LOW Voltage (Note 4)			0.4 0.45	V
C _{IN}	Input Capacitance		4		pF
C _{PD}	Power Dissipation Capacitance (per Output) (Note 4)		18		pF
R _{OUT}	Output Impedance (Note 4)		7		Ω

V_{DD} = 3.135 V to 3.465 V (3.3 V ± 5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = -40°C to +85°C

IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V _{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	2		V _{DD} + 0.3 V	V
V _{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	-0.3		0.8	V
V _{OH}	Output HIGH Voltage (Note 4)	V _{DDO} -0.3			V
V _{OL}	Output LOW Voltage (Note 4)			0.35	V
C _{IN}	Input Capacitance		4		pF
C _{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R _{OUT}	Output Impedance (Note 4)		10		Ω

V_{DD} = 2.375 V to 2.625 V (2.5 V ± 5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = -40°C to +85°C

IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			8	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V _{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	1.7		V _{DD} + 0.3 V	V
V _{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	-0.3		0.7	V
V _{OH}	Output HIGH Voltage (Note 4)	V _{DDO} -0.3			V
V _{OL}	Output LOW Voltage (Note 4)			0.35	V
C _{IN}	Input Capacitance		4		pF
C _{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R _{OUT}	Output Impedance (Note 4)		10		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to V_{DDO}/2 (see Figure 5).

NB3H83905C

Table 7. AC CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} = V_{DDO} = 3.135 V to 3.465 V (3.3 V ± 5%); GND = 0 V, T_A = -40°C to +85°C (Note 5)					
F _{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL_IN/CLK)	DC		100	
t _{EN} / t _{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
tSKEW _{DC}	Duty Cycle Skew (See Figure 4)	48		52	%
tSKEW _{O-O}	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase-Noise Performance f _{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		-123 -142 -153 -164		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.08 0.08		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps

V_{DD} = V_{DDO} = 2.375 V to 2.625 V (2.5 V ± 5%); GND = 0 V, T_A = -40°C to +85°C (Note 5)

F _{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t _{EN} / t _{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
tSKEW _{DC}	Duty Cycle Skew (See Figure 4)	47		53	%
tSKEW _{O-O}	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase-Noise Performance f _{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		-118 -137 -151 -165		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.13 0.13		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps

V_{DD} = V_{DDO} = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = -40°C to +85°C (Note 5)

F _{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t _{EN} / t _{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
tSKEW _{DC}	Duty Cycle Skew (See Figure 4)	47		53	%
tSKEW _{O-O}	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase-Noise Performance f _{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		-129 -145 -147 -157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.27 0.27		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Crystal inputs ≤ F_{max}. Outputs loaded with 50 Ω to V_{DDO}/2. CLOCK (LVCMOS levels at XTAL1 input) 50% duty cycle. See Figures 4 and 7. See APPLICATION INFORMATION; Crystal Input Interface for CL loading.

NB3H83905C

Table 7. AC CHARACTERISTICS (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} = 3.135 V to 3.465 V (3.3 V ± 5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V ± 5%); GND = 0 V, T_A = -40°C to +85°C (Note 5)					
F _{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL_IN/CLK)	DC		100	
t _{EN} / t _{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
tSKEW _{DC}	Duty Cycle Skew (See Figure 4)	48		52	%
tSKEW _{O-O}	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase-Noise Performance f _{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		-129 -145 -147 -157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.14 0.14		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps

V_{DD} = 3.135 V to 3.465 V (3.3 V ± 5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = -40°C to +85°C (Note 5)

F _{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t _{EN} / t _{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
tSKEW _{DC}	Duty Cycle Skew (See Figure 4)	48		52	%
tSKEW _{O-O}	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase-Noise Performance f _{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		-129 -145 -147 -157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.18 0.18		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

V_{DD} = 2.375 V to 2.625 V (2.5 V ± 5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = -40°C to +85°C (Note 5)

F _{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t _{EN} / t _{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
tSKEW _{DC}	Duty Cycle Skew (See Figure 4)	47		53	%
tSKEW _{O-O}	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase-Noise Performance f _{out} = 25 MHz/ 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		-129 -145 -147 -157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.19 0.19		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Crystal inputs ≤ F_{max}. Outputs loaded with 50 Ω to V_{DDO}/2. CLOCK (LVCMOS levels at XTAL1 input) 50% duty cycle. See Figures 4 and 7. See APPLICATION INFORMATION; Crystal Input Interface for CL loading.

NB3H83905C

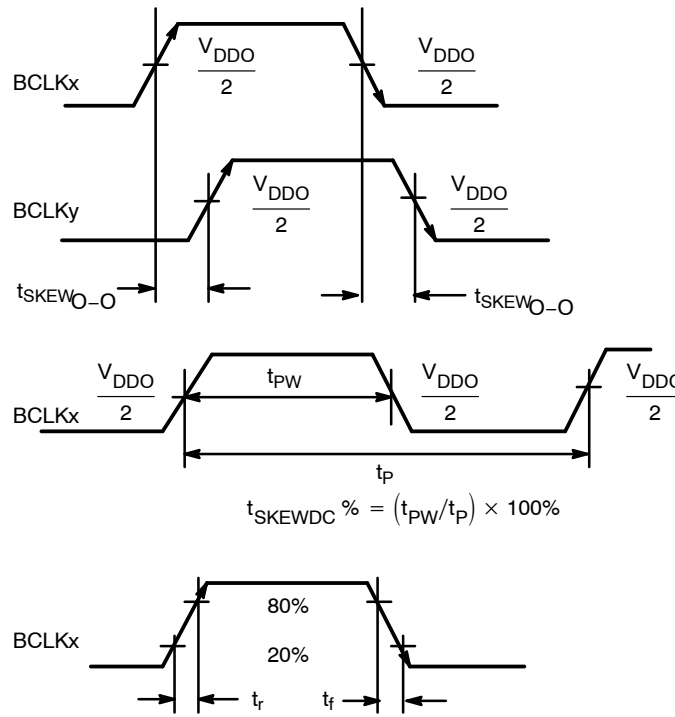


Figure 4. AC Reference Measurement

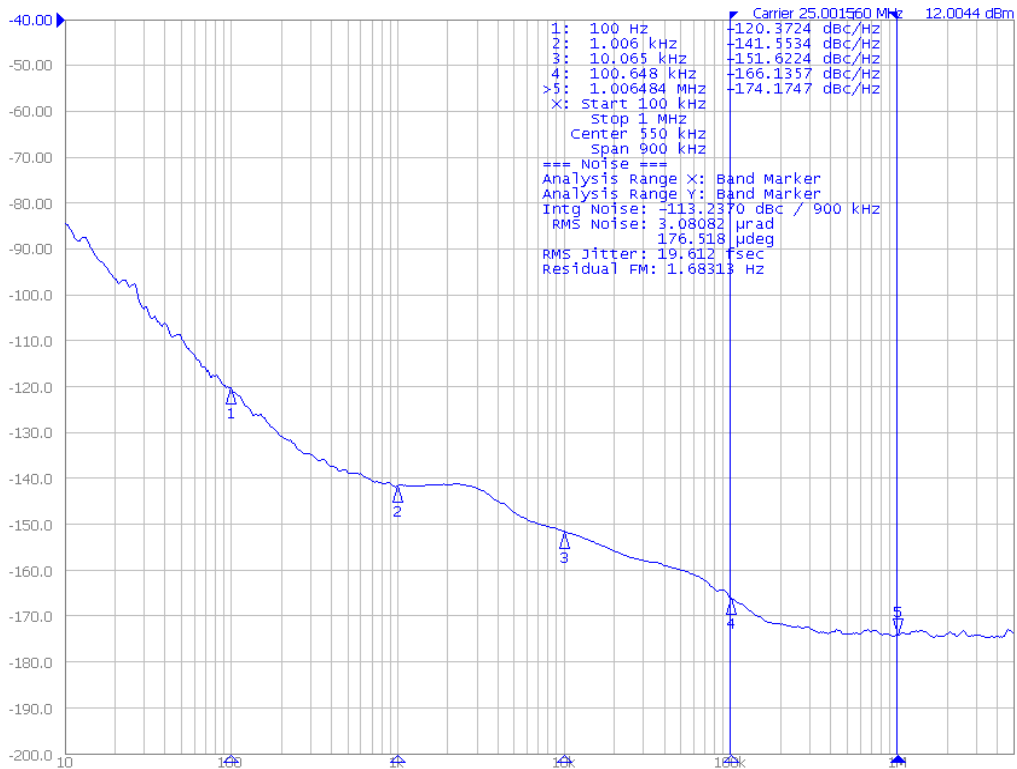


Figure 5. Typical Phase Noise Plot of the NB3H83905C Operating at 25 MHz $V_{DD} = V_{DDO} = 3.3$ V

NB3H83905C

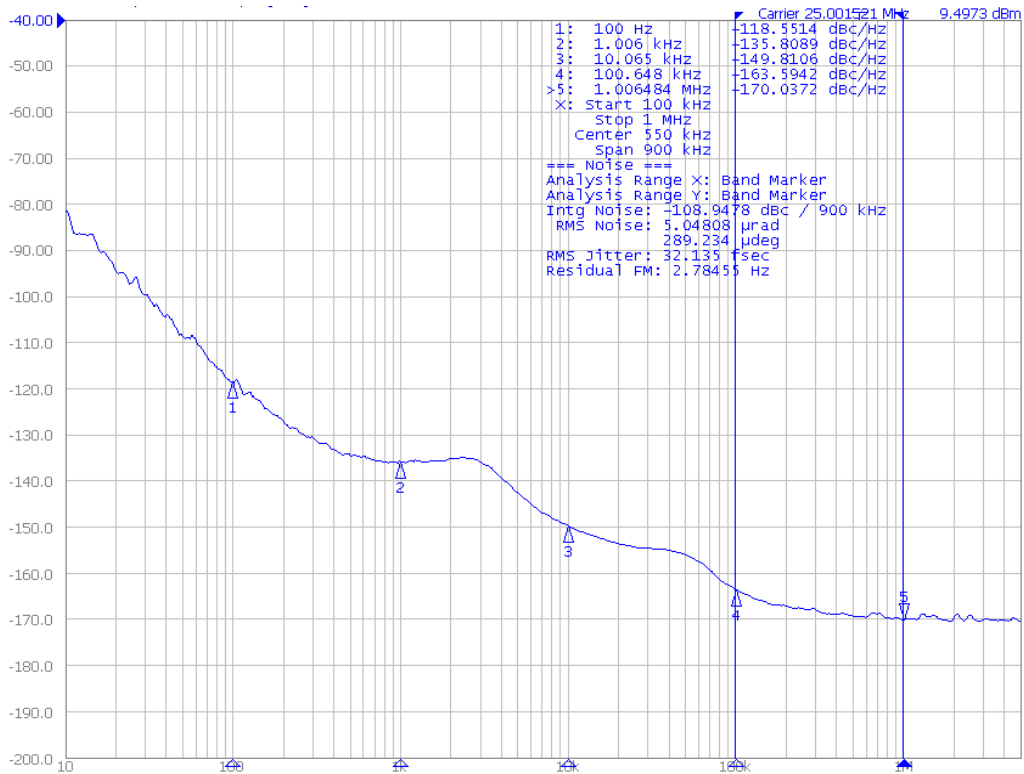


Figure 6. Typical Phase Noise Plot of the NB3H83905C Operating at 25 MHz $V_{DD} = V_{DDO} = 2.5$ V

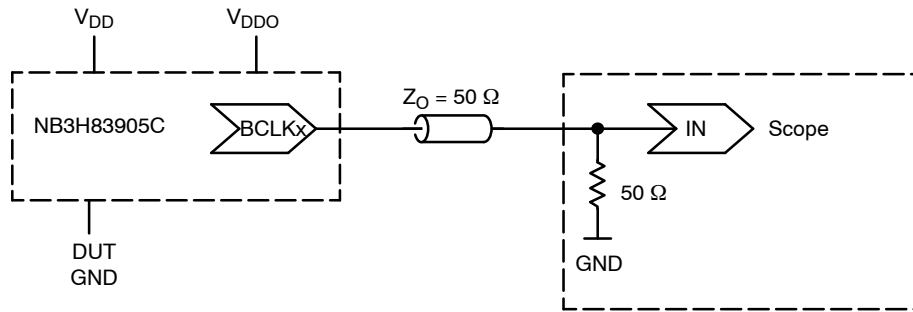


Figure 7. Typical Device Evaluation and Termination Setup – See Table 8

Table 8. TEST SUPPLY SETUP. V_{DDO} SUPPLY MAY BE CENTERED ON 0.0 V (SCOPE GND) TO PERMIT DIRECT CONNECTION INTO “50 Ω TO GND” SCOPE MODULE. V_{DD} SUPPLY TRACKS DUT GND PIN

Spec Condition:	Test Setup V_{DD} :	Test Setup V_{DDO} :	Test Setup DUT GND:
$V_{DD} = V_{DDO} = 3.135$ V to 3.465 V (3.3 V $\pm 5\%$)	1.56 to 1.73 V	1.56 to 1.73 V	-1.56 to -1.73 V
$V_{DD} = V_{DDO} = 2.375$ V to 2.625 V (2.5 V $\pm 5\%$)	1.1875 to 1.3125 V	1.1875 to 1.3125 V	-1.1875 to -1.3125 V
$V_{DD} = V_{DDO} = 1.6$ V to 2.0 V (1.8 V ± 0.2 V)	0.8 to 1.0 V	0.8 to 1.0 V	-0.8 to -1.0 V
$V_{DD} = 3.135$ V to 3.465 V (3.3 V $\pm 5\%$); $V_{DDO} = 2.375$ V to 2.625 V (2.5 V $\pm 5\%$)	1.955 to 2.1525 V	1.1875 to 1.3125 V	-1.1875 to -1.3125 V
$V_{DD} = 3.135$ V to 3.465 V (3.3 V $\pm 5\%$); $V_{DDO} = 1.6$ V to 2.0 V (1.8 V ± 0.2 V)	2.335 to 2.465 V	0.8 to 1.0 V	-0.8 to -1.0 V
$V_{DD} = 2.375$ V to 2.625 V (2.5 V $\pm 5\%$); $V_{DDO} = 1.6$ V to 2.0 V (1.8 V ± 0.2 V)	1.575 to 1.625 V	0.8 to 1.0 V	-0.8 to -1.0 V

NB3H83905C

APPLICATION INFORMATION

Crystal Input Interface

Figure 8 shows the NB3H83905C device crystal oscillator interface using a typical parallel resonant crystal. A parallel crystal with loading capacitance $C_L = 18 \text{ pF}$ would use $C1 = 32 \text{ pF}$ and $C2 = 32 \text{ pF}$ as nominal values, assuming 4 pF of stray cap per line. The frequency accuracy and duty cycle skew can be fine tuned by adjusting the $C1$ and $C2$ values. For example, increasing the $C1$ and $C2$ values will reduce the operational frequency. Note $R1$ is optional and may be 0Ω .

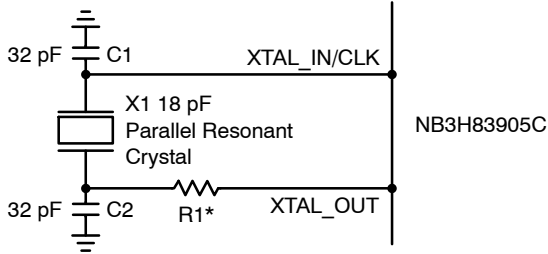


Figure 8. NB3H83905C Crystal Oscillator Interface
* $R1$ is optional

Termination

NB3H83905C device output series termination may be used by locating a 28Ω series resistor at the driver pin as shown in Figure 9. Alternatively, a Thevenin Parallel termination may be used by locating a 100Ω pullup resistor to V_{DD} and a 100Ω pullup resistor to GND at the receiver pin, instead of an R_s source termination resistor, Figure 10.

Unused Input and Output Pins

All LVCMOS control pins have internal pull-ups or pull-downs; additional external resistors are not required (optionally $1 \text{ k}\Omega$ resistors may be used). All unused LVCMOS outputs can be left floating with no trace attached.

Bypass

The V_{DD} and V_{DDO} supply pins should be bypassed with both a $10 \mu\text{F}$ and a $0.1 \mu\text{F}$ cap from supply pins to GND.

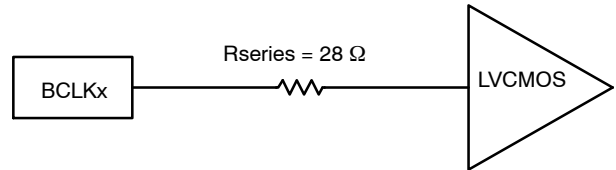


Figure 9. Series Termination

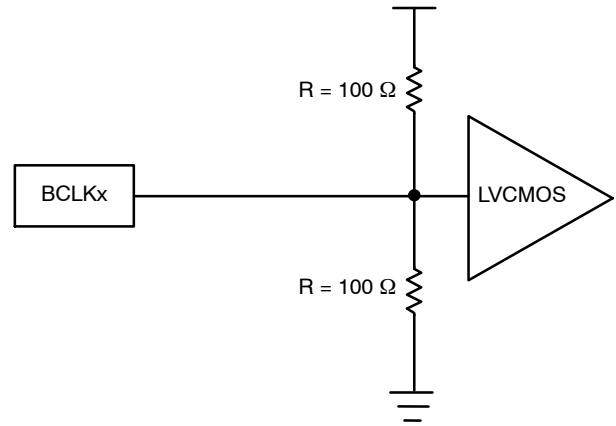


Figure 10. Optional Thevenin Termination

ORDERING INFORMATION

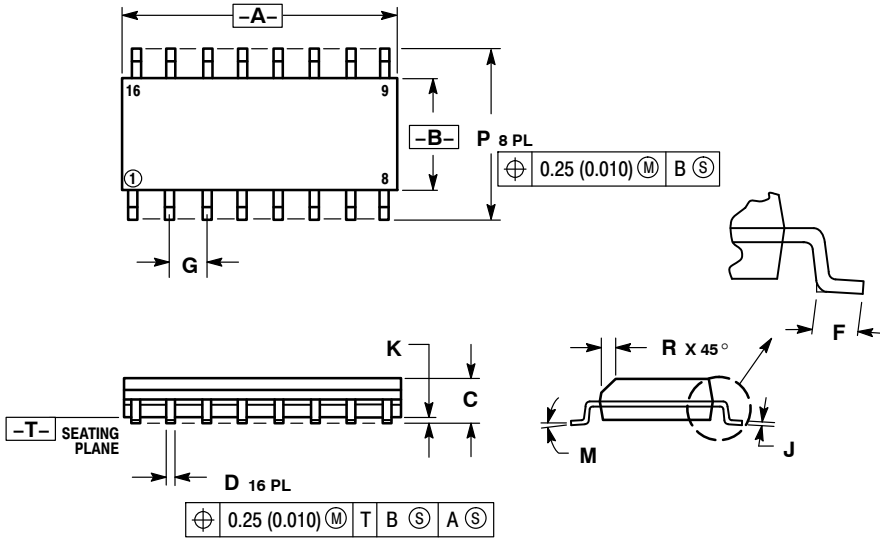
Device	Package	Shipping†
NB3H83905CDG	SOIC-16 (Pb-Free)	48 Units / Rail
NB3H83905CDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NB3H83905CDTG	TSSOP-16 (Pb-Free)	96 Units / Rail
NB3H83905CDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NB3H83905CMNG	QFN-20 (Pb-Free)	92 Units / Rail
NB3H83905CMNTXG	QFN-20 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3H83905C

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

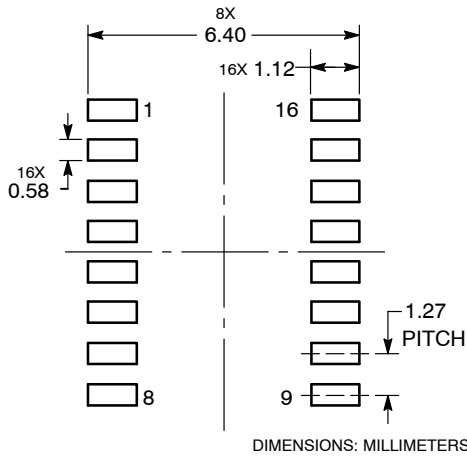


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

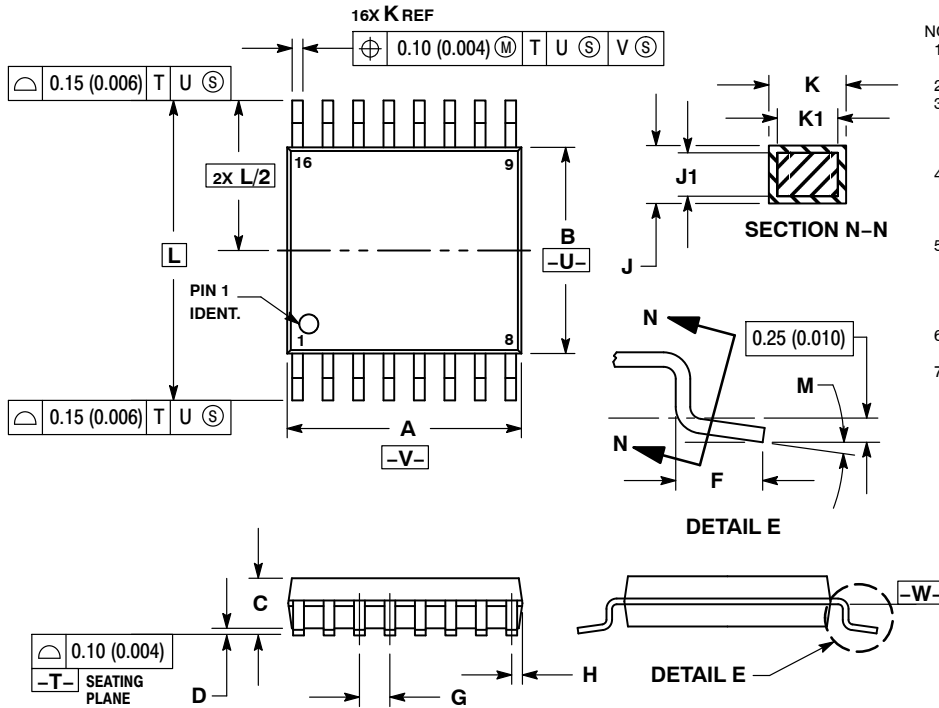


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB3H83905C

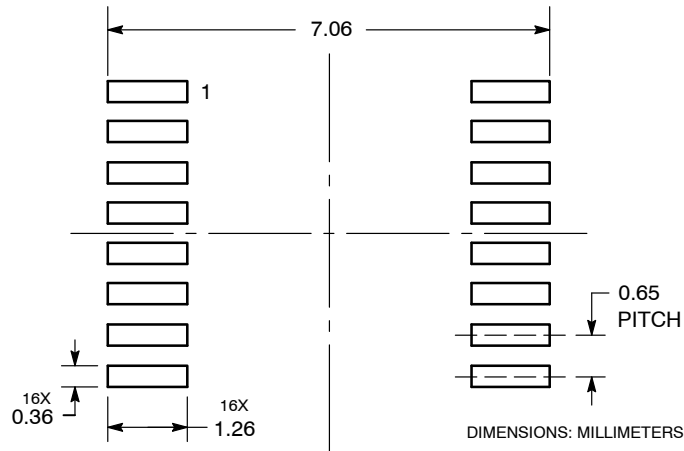
PACKAGE DIMENSIONS

TSSOP-16
CASE 948F
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

SOLDERING FOOTPRINT*

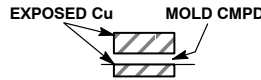
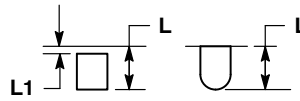
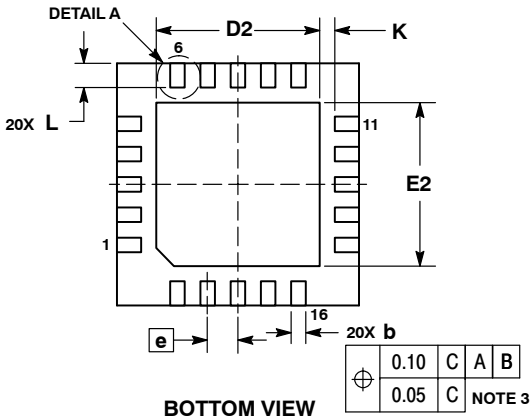
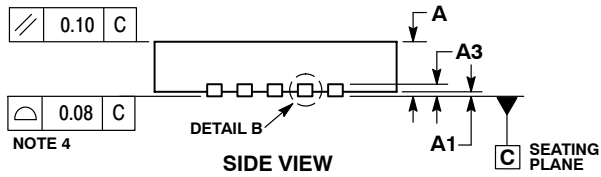
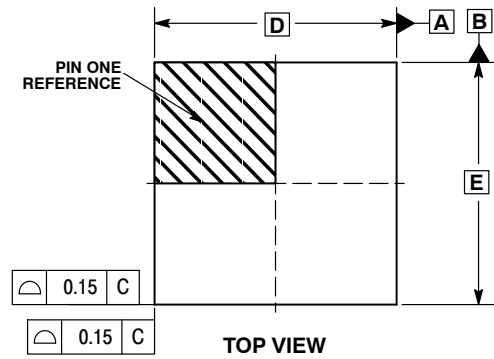


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB3H83905C

PACKAGE DIMENSIONS

QFN20 4x4, 0.5P
CASE 485BH
ISSUE O

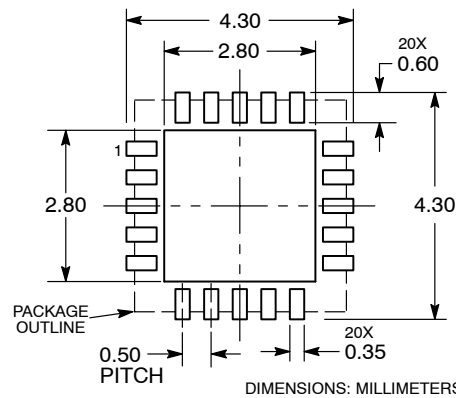


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	0.00	0.15

MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative