

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



FAST CMOS 1-TO-10 CLOCK DRIVER

IDT74FCT807BT/CT

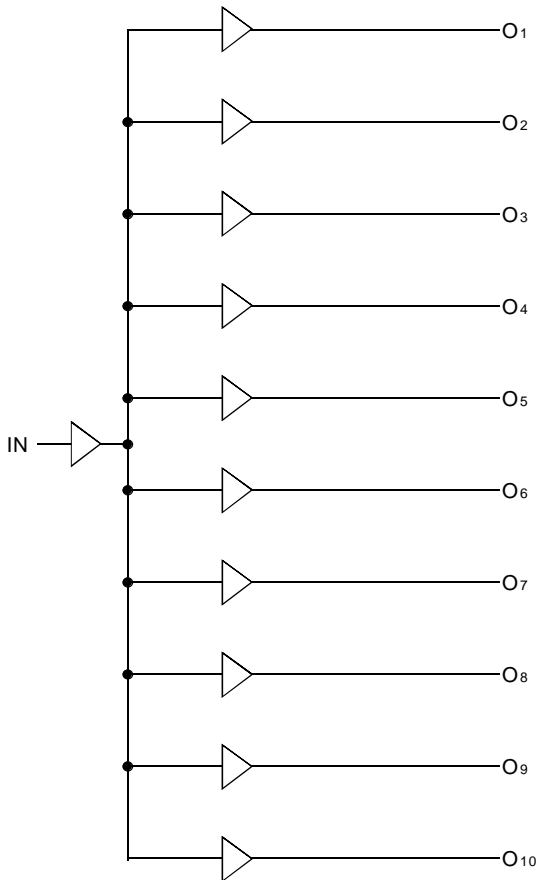
FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 250ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 2.5ns (max.)
- 100MHz operation
- TTL compatible inputs and outputs
- TTL level output voltage swings
- 1:10 fanout
- Output rise and fall time < 1.5ns (max)
- Low input capacitance: 4.5pF typical
- High drive: -32mA I_{OH}, +48mA I_{OL}
- Available in QSOP, SSOP, and SOIC packages

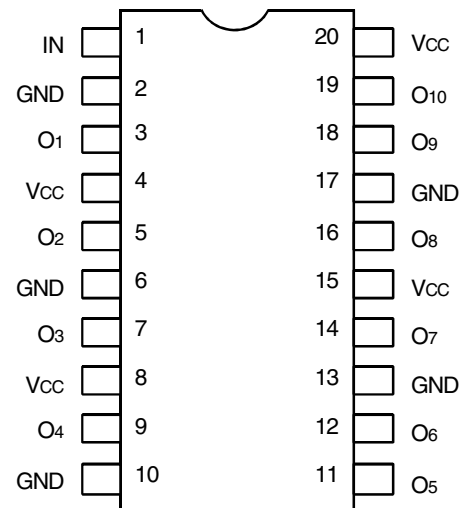
DESCRIPTION:

The FCT807T clock driver is built using advanced dual metal CMOS technology. This low skew clock driver features 1:10 fanout, providing minimal loading on the preceding drivers. The FCT807T offers low capacitance inputs with hysteresis for improved noise margins. TTL level outputs and multiple power and grounds reduce noise. The device also features -32/48mA drive capability for driving low impedance traces.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP/ SOIC/ SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
IN	Inputs
Ox	Outputs

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, Industrial: T_A = -40°C to +85°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	—	V	
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max., V _I = 2.7V	—	—	±1	μA	
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max., V _I = 0.5V	—	—	±1	μA	
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = Max., V _O = 2.7V	—	—	±1	μA	
I _{OZL}			V _O = 0.5V	—	—		±1
I _I	Input HIGH Current	V _{CC} = Max., V _I = V _{CC} (Max.)	—	—	±1	μA	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V	
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _O = GND ⁽³⁾	-60	-120	-225	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15mA	2.4	3.3	—	V
			I _{OH} = -32mA	2	3	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	—	0.3	0.55	V	
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±1	μA	
V _H	Input Hysteresis for all inputs	—	—	150	—	mV	
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	—	5	500	μA	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽³⁾	V _{CC} = Max. Input Toggling 50% Duty Cycle Outputs Open	V _{IN} = V _{CC} V _{IN} = GND	—	0.4	0.6	mA/MHz
I _C	Total Power Supply Current ⁽⁵⁾	V _{CC} = Max. Input Toggling 50% Duty Cycle Outputs Open f _i = 50MHz	V _{IN} = V _{CC} V _{IN} = GND	—	20	30.5 ⁽⁴⁾	mA
			V _{IN} = 3.4V V _{IN} = GND	—	20.3	31.3 ⁽⁴⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_o = Output Frequency
 N_o = Number of Outputs at f_o
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL (3,4)

Symbol	Parameter	Conditions ⁽¹⁾	FCT807BT		FCT807CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	50Ω to V _{CC} /2, C _L = 10pF (See figure 1) or 50Ω ac termination, C _L = 10pF (See figure 2) f ≤ 100MHz Outputs connected in groups of two	1.3	2.7	1.3	2.5	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.25	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.65	ns	

Symbol	Parameter	Conditions ⁽¹⁾	FCT807BT		FCT807CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 30pF f ≤ 67MHz (See figure 3)	1.5	3.8	1.5	3.5	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.25	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.75	ns	

Symbol	Parameter	Conditions ⁽¹⁾	FCT807BT		FCT807CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 30pF f ≤ 40MHz (See figure 4)	1.5	3.8	1.5	3.5	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	1	—	0.75	ns	

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL (3,4)

Symbol	Parameter	Conditions ⁽¹⁾	FCT807BT		FCT807CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	50Ω to V _{CC} /2, C _L = 10pF (See figure 1) or 50Ω ac termination, C _L = 10pF (See figure 2) f ≤ 100MHz Outputs connected in groups of two	1.3	2.9	1.3	2.7	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ((t _{PHL} – t _{PLH}))		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.65	ns	

Symbol	Parameter	Conditions ⁽¹⁾	FCT807BT		FCT807CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 30pF f ≤ 67MHz (See figure 3)	1.5	4	1.5	3.7	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ((t _{PHL} – t _{PLH}))		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	0.9	—	0.75	ns	

Symbol	Parameter	Conditions ⁽¹⁾	FCT807BT		FCT807CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 30pF f ≤ 40MHz (See figure 4)	1.5	4	1.5	3.7	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.45	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output ((t _{PHL} – t _{PLH}))		—	0.7	—	0.55	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	—	1	—	0.75	ns	

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS

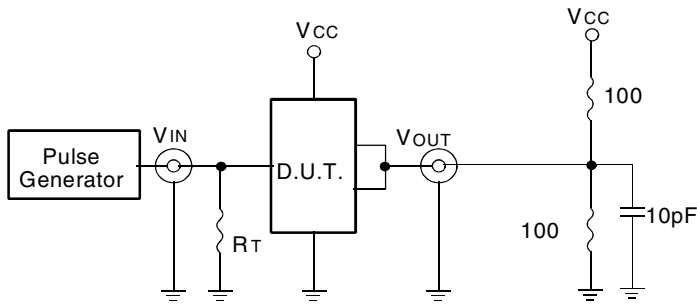


Fig. 1: 50Ω to Vcc/2, CL = 10pF

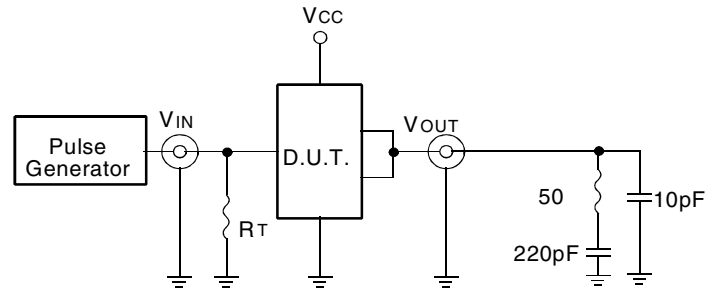


Fig. 2: 50Ω AC Termination, CL = 10pF

The capacitor value for AC termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

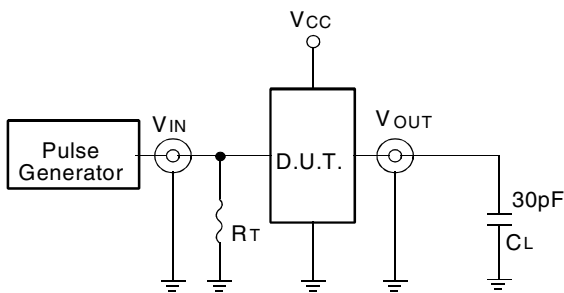


Fig. 3: CL = 30pF Circuit

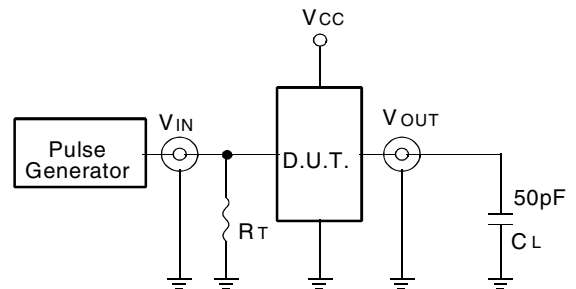


Fig. 4: CL = 50pF Circuit

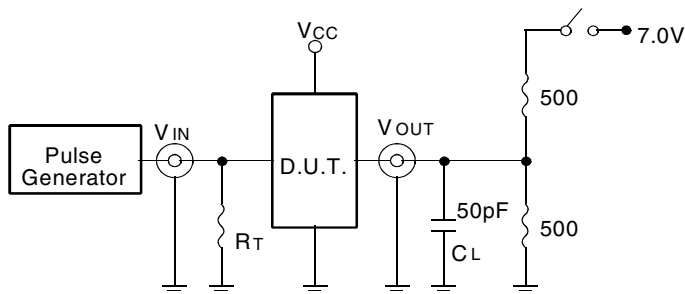


Fig. 5: Enable and Disable Time Circuit

SWITCH POSITION

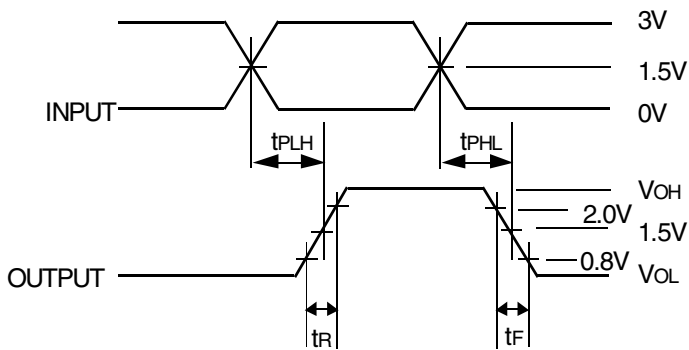
Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND

DEFINITIONS:

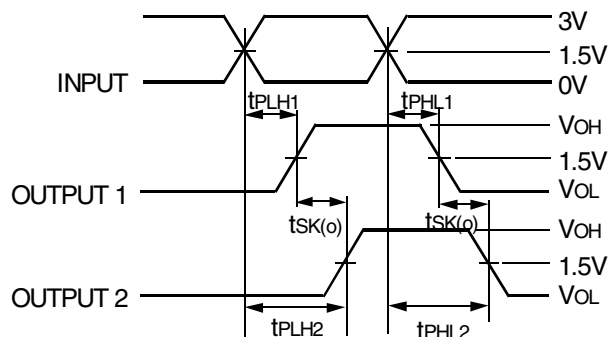
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to Zout of the Pulse Generator.

TEST WAVEFORMS

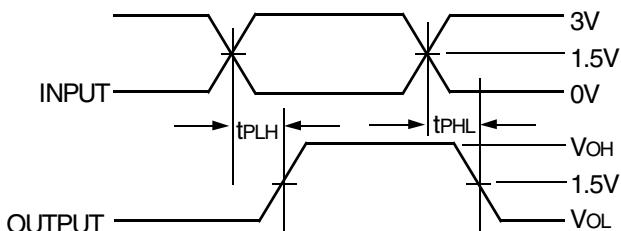


Package Delay



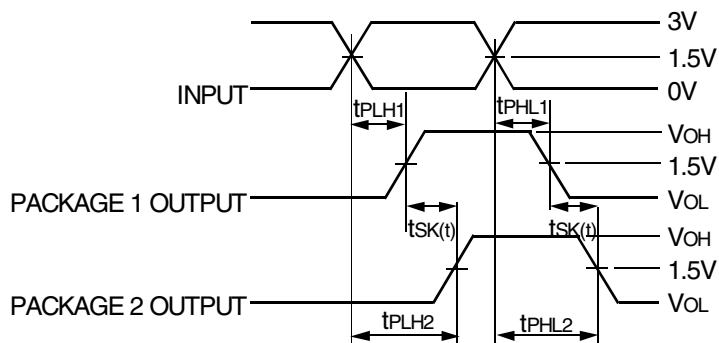
$$tsk(o) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Output Skew - $tsk(o)$



$$tsk(p) = |tPHL - tPLH|$$

Pulse Skew - $tsk(p)$

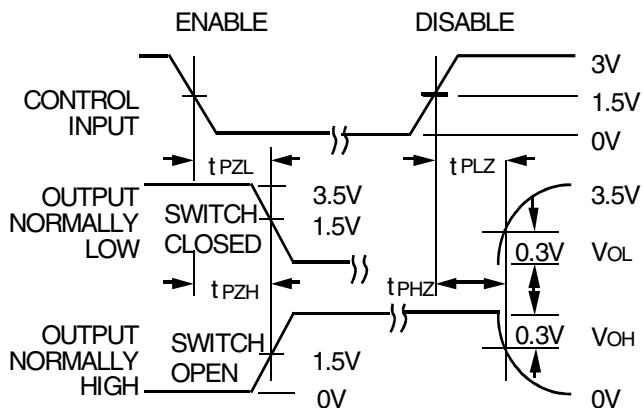


$$tsk(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Part-to-Part Skew - $tsk(t)$

NOTE:

1. Package 1 and Package 2 are same device type and speed grade.

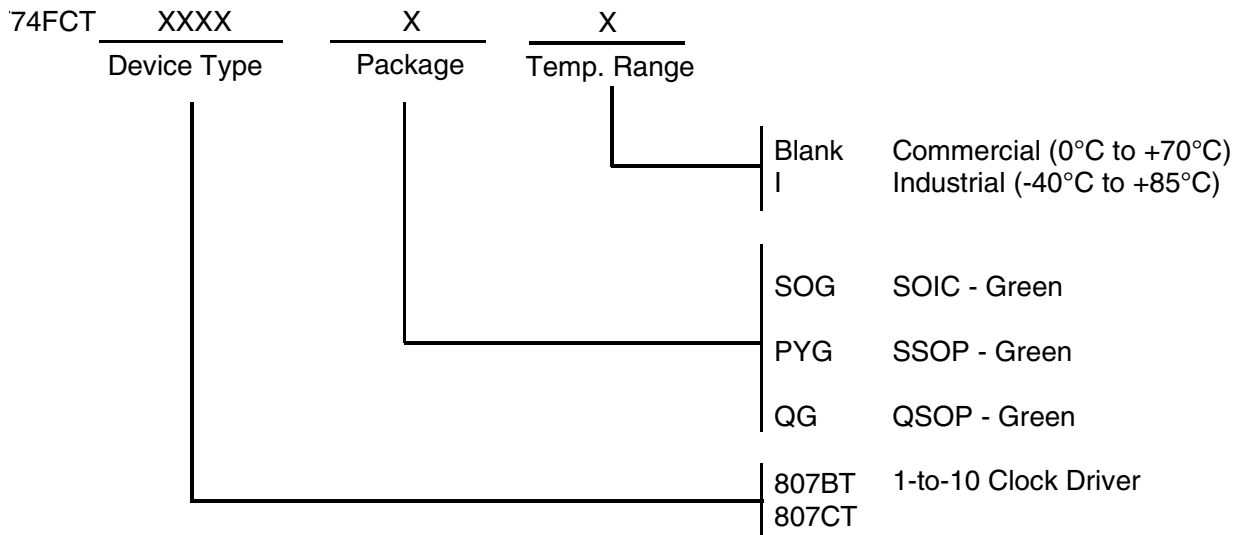


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION



CORPORATE HEADQUARTERS
 6024 Silver Creek Valley Road
 San Jose, CA 95138

for SALES:
 800-345-7015 or 408-284-8200
 fax: 408-284-2775
 www.idt.com

for Tech Support:
 clockhelp@idt.com