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PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016 DATASHEET

#### **FEATURES**:

- Optimized for 2.5V LVTTL
- Guaranteed Low Skew < 125ps (max)
- Very low duty cycle distortion < 300ps (max)</li>
- High speed propagation delay < 2ns. (max)
- Up to 200MHz operation
- Very low CMOS power levels
- · Hot insertable and over-voltage tolerant inputs
- 1:10 fanout buffer
- 2.5V VDD
- · Available in TSSOP package
- NOT RECOMMENDED FOR NEW DESIGNS
- For replacement part use 8T39S11

#### **APPLICATIONS:**

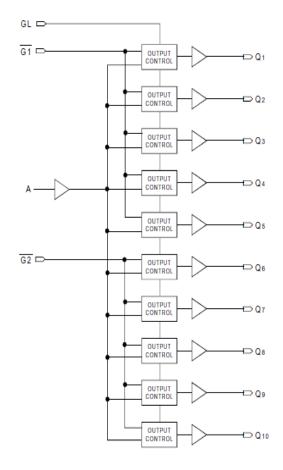
· Clock and signal distribution

## FUNCTIONAL BLOCK DIAGRAM

#### **DESCRIPTION:**

The 5t9070 2.5V single data rate (SDR) clock buffer is a single-ended input to ten single-ended outputs buffer built on advanced metal CMOS technology. The SDR clock buffer fanout from a single input to ten single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network.

The 5t9070 has two output banks that can be asynchronously enabled/ disabled. Multiple power and grounds reduce noise.



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#### **PIN CONFIGURATION**

	ſ		-ر ،		1	
GL		1	$\cup$	48		GND
Vod		2		47		VDD
Vod		3		46		VDD
GND		4		45		GND
GND		5		44		GND
G1		6		43		GND
Vod		7		42		VDD
Q2		8		41		Q3
Q1		9		40		Q4
GND		10		39		GND
Vod		11		38		VDD
GND		12		37		Q5
A		13		36		Q6
Vod		14		35		VDD
GND		15		34		GND
Q10		16		33		Q7
Q9		17		32		Q8
Vod		18		31		VDD
G2		19		30		VDD
GND		20		29		GND
GND		21		28		GND
Vod		22		27		VDD
Vod		23		26		GND
NC		24		25		NC
					]	
		Т	SSOF	5		
	Т	0				

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
Vdd	Power Supply Voltage	-0.5 to +3.6	V
VI	Input Voltage	-0.5 to +3.6	V
Vo	Output Voltage	-0.5 to VDD +0.5	V
TSTG	Storage Temperature	-65 to +165	°C
τJ	Junction Temperature	150	°C

NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **CAPACITANCE<sup>(1)</sup>** (TA = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Tvd.	Max.	Unit
Cin	Input Capacitance	_	6	_	pF

NOTE:

1. This parameter is measured at characterization but not tested.

# **RECOMMENDED OPERATING RANGE**

Symbol	Description	Min.	Tvp.	Max.	Unit
Та	Ambient Operating Temperature	-40	+25	+85	°C
Vdd	Internal Power Supply Voltage	2.3	2.5	2.7	V

Symbol	I/O	Туре	Description
A		LVTTL	Clock input
G1	Ι	LVTTL	Gate for outputs Q1 through Q5. When $\overline{G1}$ is LOW, these outputs are enabled. When $\overline{G1}$ is HIGH, these outputs are asynchronously disabled to the level designated by GL <sup>(1)</sup> .
G2	Ι	LVTTL	Gate for outputs Q <sub>6</sub> through Q <sub>10</sub> . When $\overline{G2}$ is LOW, these outputs are enabled. When $\overline{G2}$ is HIGH, these outputs are asyn- chronously disabled to the level designated by GL <sup>(1)</sup> .
GL		LVTTL	Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW.
Qn	0	LVTTL	Clock outputs
Vdd		PWR	Power supply for the device core, inputs, and outputs
GND		PWR	Power supply return for power

#### **PIN DESCRIPTION**

NOTE:

1. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE <sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(4)</sup>	Max	Unit
Ін	Input HIGH Current	$V_{DD} = 2.7V$ $V_I = V_{DD}/GND$		_	±5	μA
	Input LOW Current	VDD = 2.7V VI = GND/VDD	_	_	±5	
Vik	Clamp Diode Voltage	VDD = 2.3V, IIN = -18mA	_	- 0.7	- 1.2	V
Vin	DC Input Voltage		- 0.3		+3.6	V
Vih	DC Input HIGH <sup>(2)</sup>		1.7		_	V
VIL	DC Input LOW <sup>(3)</sup>		_		0.7	V
Vон	Output HIGH Voltage	Іон = -12mA	Vdd - 0.4		_	V
		Iон = -100 <b>u</b> A	Vdd - 0.1		_	V
Vol	Output LOW Voltage	IoL = 12mA	_		0.4	V
		lol = 100µA	-		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Voltage required to maintain a logic HIGH.

3. Voltage required to maintain a logic LOW.

4. Typical values are at VDD = 2.5V, +25°C ambient.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Тур.	Max	Unit
IDDQ	Quiescent Vbb Power Supply Current Vbb = Max., Reference Clock = LOW		1.5	2	mA
		Outputs enabled, All outputs unloaded			
lddd	Dynamic Vod Power Supply Current per Output	V <sub>DD</sub> = Max., V <sub>DD</sub> = Max., C <sub>L</sub> = 0pF	150	200	µA/MHz
Ітот	Total Power VDD Supply Current	Vdd = 2.5V., Freference clock = 100MHz, Cl = 15pF	70	90	mA
		Vdd = 2.5V., Freference clock = 200MHz, Cl = 15pF	100	150	

NOTE:

1. The termination resistors are excluded from these measurements.

#### INPUT AC TEST CONDITIONS

Symbol	Parameter	Value	Units
Vih	Input HIGH Voltage	Vdd	V
VIL	Input LOW Voltage	0	V
Vтн	Input Timing Measurement Reference Level <sup>(1)</sup>	VDD/2	V
tr, tr	Input Signal Edge Rate <sup>(2)</sup>	2	V/ns

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.

2. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

#### AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE<sup>(4)</sup>

Symbol	Parameter	Min.	Тур.	Мах	Unit
Skew Parameters		I			
<u>tsк(о)</u>	Same Device Output Pin-to-Pin Skew <sup>(1)</sup>		_	125	ps
tsk(p)	Pulse Skew <sup>(2)</sup>			300	ps
tsk(pp)	Part-to-Part Skew <sup>(3)</sup>	_	_	300	ps
Propagation Dela	у			1	
<b>t</b> PLH	Propagation Delay A to Qn	—	—	2	ns
<u>tphl</u>					L
tr	Output Rise Time (20% to 80%)	350		850	ps
tF	Output Fall Time (20% to 80%)	350		850	ps
fo	Frequency Range	-	_	200	MHz
Output Gate Enat	ole/Disable Delay	•			
<b>t</b> PGE	Output Gate Enable to Qn		_	3.5	ns
tpgd	Output Gate Enable to Qn Driven to GL Designated Level	-	—	3	ns

NOTES:

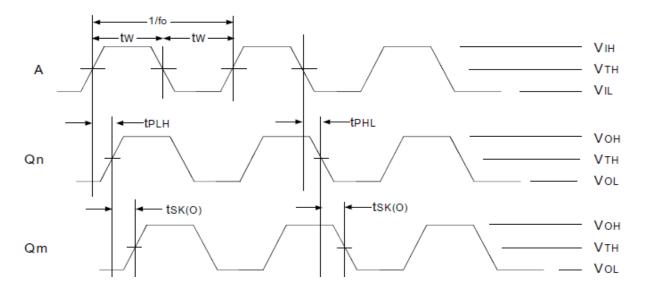
1. Skew measured between all outputs under identical input and output transitions and load conditions on any one device.

2. Skew measured is the difference between propagation delay times tPHL and tPLH of any output under identical input and output transitions and load conditions on any one device.

3. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical Vbb levels and temperature.

4. Guaranteed by design.

#### AC TIMING WAVEFORMS

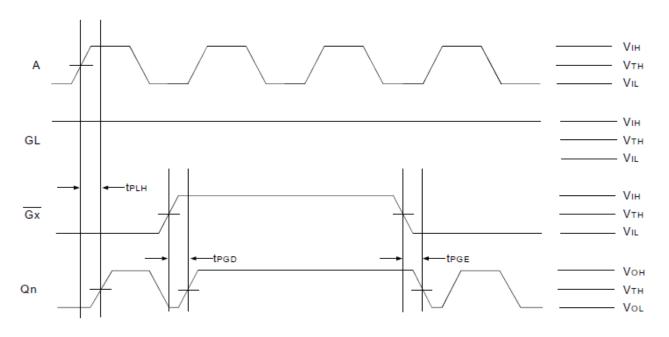


#### Propagation and Skew Waveforms

NOTE: Pulse Skew is calculated using the following expression:

tsk(p) = | tphl - tplh |

where tPHL and tPLH are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the tPHL and tPLH shown are not valid measurements for this calculation because they are not taken from the same pulse.

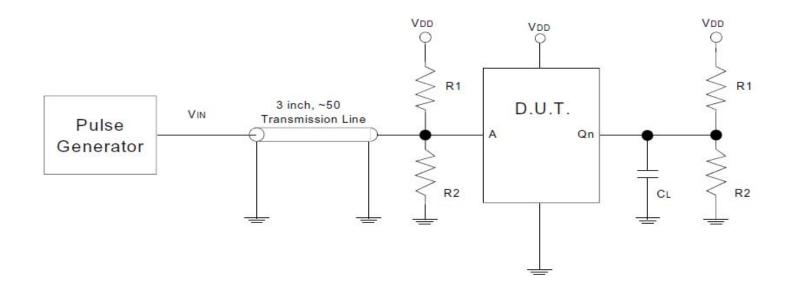


#### Gate Disable/Enable Runt Pulse Generation

#### NOTE:

As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their Gx signals to avoid this problem.

# **TEST CIRCUIT AND CONDITIONS**

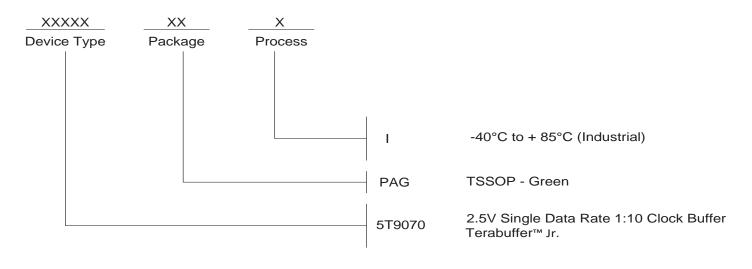


Test Circuit for Input/Output

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
VTH	Vdd / 2	V
R1	100	Ω
R2	100	Ω
CL	15	pF

#### **INPUT/OUTPUT TEST CONDITIONS**

## **ORDERING INFORMATION**



## **REVISION HISTORY**

Rev	Table	Page	Discription of Change	Date
A		1	NRND - Not Recommended for New Designs	5/5/13
А		7	Ordering Information - removed PA leaded device Updated datsheet format	4/14/15
А		1	Product Discontinuation Notice - Last Time Buy Expires September 7, 2016. PDN# N-16-02.	3/10/16



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