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CLOCK DISTRIBUTION CIRCUIT

IDT6P30006A

Description

The IDT6P30006A is a low-power, eight output clock distribution circuit. The device takes a TCXO or LVCMOS input and generates eight high-quality outputs.

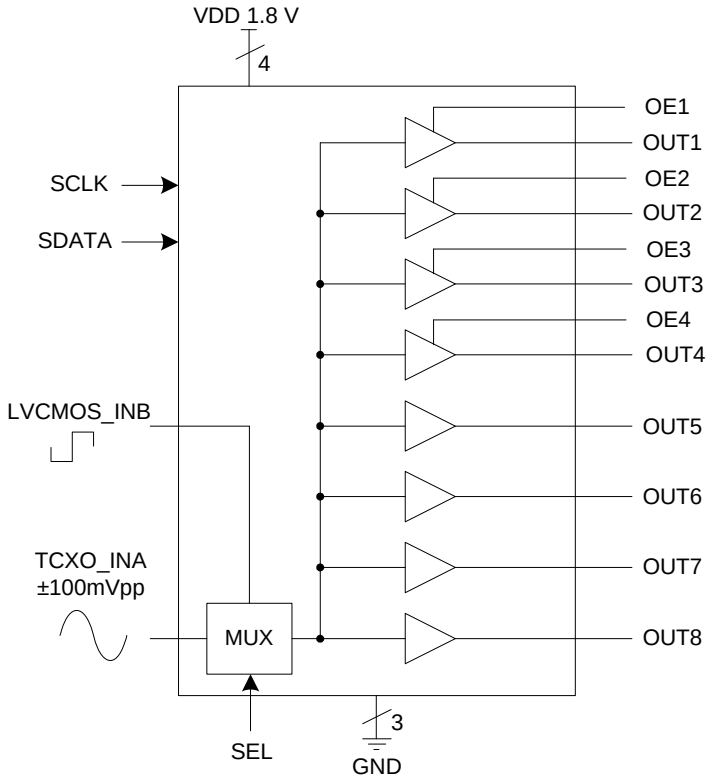
It includes a redundant input with automatic glitch-free switching when the primary reference is removed. The primary input may be selected by the user by pulling the SEL pin low or high. If the primary input is removed and brought back, it will not be re-selected until 1024 cycles have passed.

The IDT6P30006A specifically addresses the needs of handheld applications in both performance and package size. The device is packaged in a small 4mm x 4mm 24-pin QFN, allowing optimal use for limited board space.

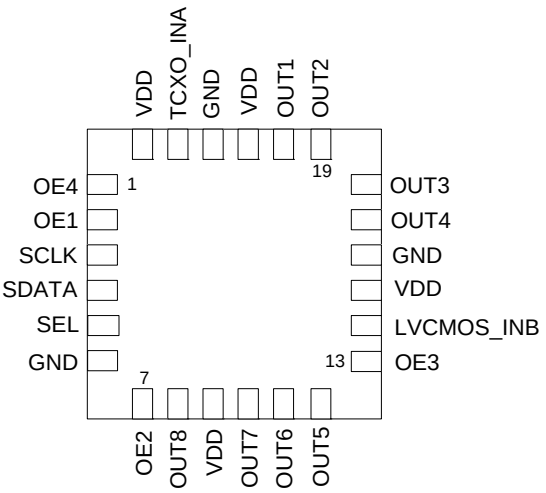
Features

- Packaged in 24-pin QFN
- LVCMOS or TCXO sine wave input
- +1.8 V operating voltage
- Glitch-free input switching
- Eight buffered square wave outputs at 1.8 V LVCMOS levels
- Individual output enables controlled via I^2C or OEx
- Pb free, RoHS compliant package
- Industrial temperature range (-40°C to +85°C)

Block Diagram



Pin Assignment



24- pin QFN

SEL Pin Configuration Table

SEL	Primary Input
0	LVCMOS_INB
1	TCXO_INA

OE Pin Configuration Table

OEx	OUTx
0	Disabled
1	Enabled

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	OE4	Input	Output enable control for OUT4. Internal pull-up resistor. See table above.
2	OE1	Input	Output enable control for OUT1. Internal pull-up resistor. See table above.
3	SCLK	Input	I^2C clock input.
4	SDATA	I/O	I^2C data input.
5	SEL	Input	Select pin for primary inputs. See table above. Internal pull-up resistor.
6	GND	Power	Connect to ground.
7	OE2	Input	Output enable control for OUT2. Internal pull-up resistor. See table above.
8	OUT8	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
9	VDD	Power	Connect to +1.8 V.
10	OUT7	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
11	OUT6	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
12	OUT5	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
13	OE3	Input	Output enable control for OUT3. Internal pull-up resistor. See table above.
14	LVCMOS_INB	Input	Connect to 13 MHz LVCMOS clock input. See table above.
15	VDD	Power	Connect to +1.8 V.
16	GND	Power	Connect to ground.

Pin Number	Pin Name	Pin Type	Pin Description
17	OUT4	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
18	OUT3	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
19	OUT2	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
20	OUT1	Output	Buffered output. Outputs tri-state with weak pull-down when disabled.
21	VDD	Power	Connect to +1.8 V.
22	GND	Power	Connect to ground.
23	TCXO_INA	Input	Connect to 13 MHz TCXO input.
24	VDD	Power	Connect to +1.8 V.

General I²C Serial Interface

How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D2_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock will *acknowledge*
- Controller (host) starts sending *Byte N through Byte N + X - 1* (see Note 2)
- IDT clock will *acknowledge* each byte *one at a time*
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D2_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- IDT clock will *acknowledge*
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $D3_{(H)}$
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock sends *Byte N + X - 1*
- IDT clock sends *Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starTbit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte = N		.	
			ACK
O			
O		BYTE	O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starTbit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		.	Beginning Byte N
ACK			
		BYTE	O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I²C Address

The IDT6P30006A is a slave-only device that supports block read and block write protocol using a single 7 bit address and read/write bit. A block write ($D2_{(H)}$) or block read ($D3_{(H)}$) is made up of seven (7) bits and one (1) read/write bit.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	X

In applications where the indexed block write and block read are used, the dummy byte (bit 11-18) functions as a register-offset (8 bits) pointer.

Byte 0: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved	RW	Undefined	Not applicable	
6	Reserved	RW	Undefined	Not applicable	
5	Reserved	RW	Undefined	Not applicable	
4	Reserved	RW	Undefined	Not applicable	
3	OE for clock output	RW	1	Output_5 clock output	1=enabled 0=disabled
2	OE for clock output	RW	1	Output_6 clock output	1=enabled 0=disabled
1	OE for clock output	RW	1	Output_7 clock output	1=enabled 0=disabled
0	OE for clock output	RW	1	Output_8 clock output	1=enabled 0=disabled

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	RW	Undefined	Not applicable	

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	RW	Undefined	Not applicable	

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	RW	Undefined	Not applicable	

Byte 4 through 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	RW	Undefined	Not applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up	Output(s) Affected	Notes
7	Revision ID bit 3	RW	0	Not applicable	
6	Revision ID bit 2	RW	0	Not applicable	
5	Revision ID bit 1	RW	0	Not applicable	
4	Revision ID bit 0	RW	0	Not applicable	
3	Vendor ID bit 3	RW	0	Not applicable	
2	Vendor ID bit 2	RW	0	Not applicable	
1	Vendor ID bit 1	RW	0	Not applicable	
0	Vendor ID bit 0	RW	1	Not applicable	

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 µF should be connected between VDD and GND as close to the device as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into IDT pin.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT6P30006A.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT6P30006A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Max Supply Voltage, VDD	5 V
LVCMOS_INB, SCLK and SDATA Inputs	-0.5 V to +3.3 V
All Other Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Peak Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	1.62	+1.8	1.98	V

DC Electrical Characteristics

Unless otherwise specified, **VDD=1.8 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Voltage	VDD		1.62	1.8	1.98	V
Input High Voltage	V_{IH}	SEL, OE pins, LVCMOS_INB, TCXO_INA	0.75xVDD			V
		SCLK and SDATA	0.7xVDD			
Input Low Voltage	V_{IL}	SEL, OE pins, LVCMOS_INB, TCXO_INA			0.35xVDD	V
		SCLK and SDATA			0.3xVDD	
High-Level Output Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4 mA			0.4	V
Operating Supply Current	IDD	No load, all outputs switching at 13 MHz		4	6	mA
		All outputs disabled		500		µA
Short Circuit Current	I_{OS}	Single-ended clocks		±70		mA
Output Impedance	Z_O	All clock outputs, OEx=1		15		Ω
Internal Pull-Up Resistor	R_{PU}	SEL, OEx		500		kΩ
Internal Pull-Down Resistor	R_{PD}	All clock outputs, OEx=0		250		kΩ
Input Capacitance	C_{IN}	All input pins		6		pF

AC Electrical Characteristics – Single-Ended Outputs

Unless otherwise stated, **VDD = 1.8 V ±10%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}		12.6	13	13.4	MHz
TCXO Input Swing			±100		±900	mV
Variance Input Frequencies		LVCMOS_INB, TCXO_INA, Note 2			0.4	MHz
Time Switch Clock Inputs		LVCMOS_INB, TCXO_INA, Note 3		80		µs
Output Frequency Error				0		ppm
Output Rise Time	t_{OR}	20% to 80%, Note 1		1	1.5	ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1	1.5	ns
Output Clock Duty Cycle		Measured at VDD/2, Note 1	45	50	55	%
Clock Stabilization Time from Power Up		Power up, output within 1% of final frequency		3	10	ms

Note 1: CL = 5 pF.

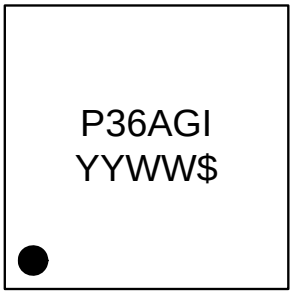
Note 2: Delta from 13 MHz.

Note 3: By removing primary input and then bringing back primary input.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		29.1		°C/W
	θ_{JA}	1 m/s air flow		22.8		°C/W
	θ_{JA}	2.5 m/s air flow		21.0		°C/W
Thermal Resistance Junction to Case	θ_{JC}			41.8		°C/W

Marking Diagram

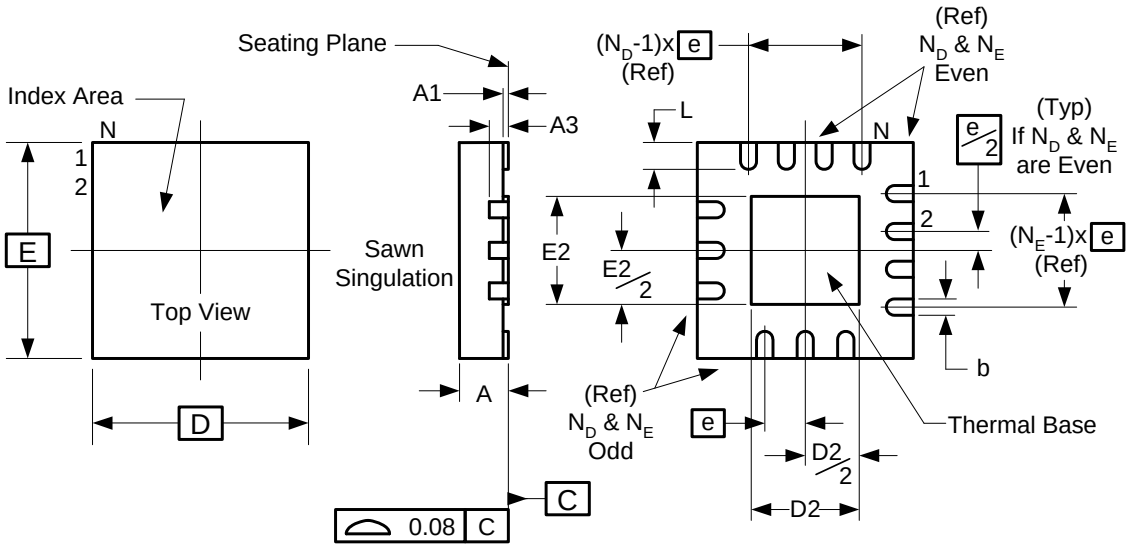


Notes:

1. YYWW is the last two digits of the year and week that the part was assembled.
3. “$” is the assembly mark code.
4. “G” after the two-letter package code designates RoHS compliant package.
5. “I” at the end of part number indicates industrial temperature range.
6. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (24-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	24	
N_D	6	
N_E	6	
D x E BASIC	4.00 x 4.00	
D2	2.3	2.55
E2	2.3	2.55
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
6P30006ANLGI	see pg. 10	Trays	24-pin QFN	-40 to +85° C
6P30006ANLGI8		Tape and Reel	24-pin QFN	-40 to +85° C

"G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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