

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NB7V58M

1.8 V / 2.5 V / 3.3 V Differential 2:1 Clock / Data Multiplexer / Translator with CML Outputs

Multi-Level Inputs w/ Internal Termination

Description

The NB7V58M is a high performance differential 2-to-1 Clock or Data multiplexer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB7V58M to accept various logic level standards, such as LVPECL, CML or LVDS.

The NB7V58M produces minimal Clock or Data jitter operating up to 7 GHz or 10.7 Gb/s, respectively. As such, the NB7V58M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The 16 mA differential CML outputs provide matching internal 50 Ω terminations and 400 mV output swings when externally terminated with a 50 Ω resistor to V_{CC} .

The NB7V58M is offered in a low profile 3 mm x 3 mm 16-pin QFN package and is a member of the GigaComm™ family of high performance Clock / Data products. For applications that require equalization, the pin-compatible NB7VQ58M is also available. Application notes, models, and support documentation are available at www.onsemi.com.

Features

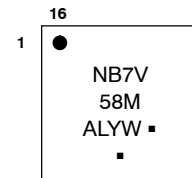
- Maximum Input Data Rate > 10.7 Gb/s
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 7 GHz
- Random Clock Jitter < 0.8 ps RMS
- 180 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 1.71$ V to 3.6 V with GND = 0 V
- Internal 50 Ω Input Termination Resistors
- QFN-16 Package, 3 mm x 3 mm
- -40°C to +85°C Ambient Operating Temperature
- This is a Pb-Free Device



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*

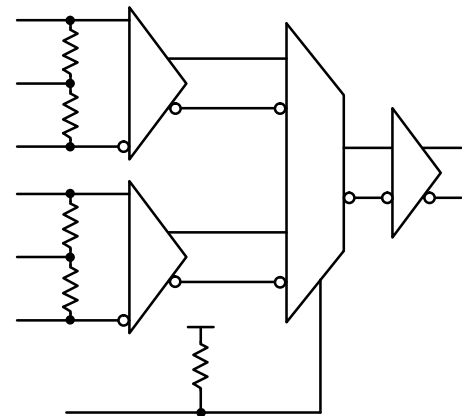


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NB7V58M

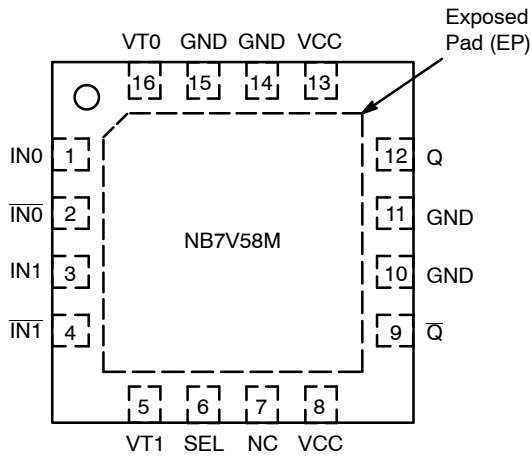


Figure 1. Pin Configuration (Top View)

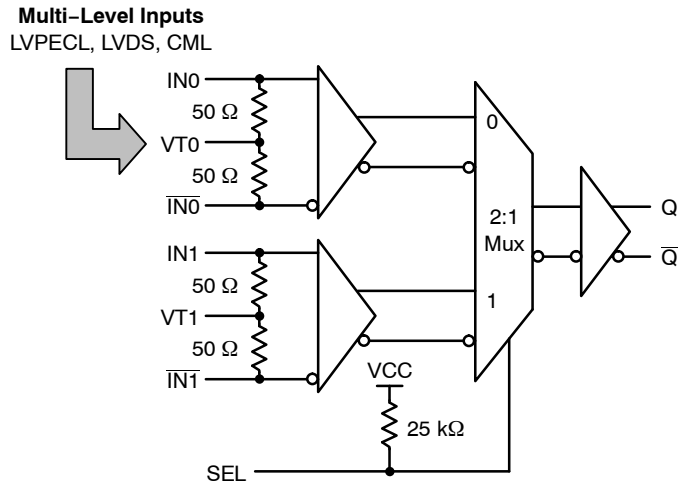


Figure 2. Detailed Block Diagram

Table 1. SElect FUNCTION TRUTH TABLE

SEL	Q	Q̄
L	IN0	IN0̄
H	IN1	IN1̄

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	IN0	LVPECL, CML, LVDS Input	Noninverted Differential Input (Note 1)
2	IN0̄	LVPECL, CML, LVDS Input	Inverted Differential Input (Note 1)
3	IN1	LVPECL, CML, LVDS Input	Noninverted Differential Input (Note 1)
4	IN1̄	LVPECL, CML, LVDS Input	Inverted Differential Input (Note 1)
5	VT1	-	Internal 50 Ω Termination Pin for IN1/IN1̄
6	SEL	LVTTTL/LVCMOS Input	SEL Input. Low for IN0 inputs, high for IN1 inputs. (Note 1) Pin will default HIGH when left open (has internal pull-up resistor)
7	NC	-	No Connect
8	VCC	-	Positive Supply Voltage (Note 2)
9	Q̄	CML Output	Inverted Differential Output
10	GND	-	Negative Supply Voltage
11	GND	-	Negative Supply Voltage
12	Q	CML Output	Noninverted Differential Output
13	VCC	-	Positive Supply Voltage (Note 2)
14	GND	-	Negative Supply Voltage
15	GND	-	Negative Supply Voltage
16	VT0	-	Internal 50 Ω Termination Pin for IN0/IN0̄
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on IN0/IN0̄, IN1/IN1̄ inputs, then the device will be susceptible to self-oscillation. Q/Q̄ outputs have internal 50 Ω source termination resistors.
2. All VCC and GND pins must be externally connected to a power supply for proper operation.

NB7V58M

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R _{PU} – SEL Input Pull-up Resistor		25 kΩ
Moisture Sensitivity (Note 3)	QFN-16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		312
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		4.0	V
V _{IN}	Positive Input Voltage	GND = 0 V		-0.5 to V _{CC} +0.5	V
V _{INPP}	Differential Input Voltage I _{Nn} – I _{Nn}			1.89	V
I _{OUT}	Output Current	Continuous Surge		34 40	mA
I _{IN}	Input Current Through R _T (50 Ω Resistor)			± 40	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 LFPM 500 LFPM	QFN-16 QFN-16	42 35	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case) (Note 4)		QFN-16	4	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB7V58M

Table 5. DC CHARACTERISTICS POSITIVE CML OUTPUT ($V_{CC} = 1.71\text{ V to }3.6\text{ V}$; $GND = 0\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$) (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
--------	----------------	-----	-----	-----	------

POWER SUPPLY CURRENT

I_{CC}	Power Supply Current (Inputs and Outputs Open)		100	150	mA
----------	--	--	-----	-----	----

CML OUTPUTS (Note 6)

V_{OH}	Output HIGH Voltage	$V_{CC} - 30$ 3270 $V_{CC} = 2.5\text{ V}$ 2470 $V_{CC} = 1.8\text{ V}$ 1770	$V_{CC} - 5$ 3295 2495 1795	V_{CC} 3300 2500 1800	mV
V_{OL}	Output LOW Voltage	$V_{CC} - 500$ 2800 $V_{CC} = 2.5\text{ V}$ 2000 $V_{CC} = 1.8\text{ V}$ 1300	$V_{CC} - 400$ 2900 2100 1400	$V_{CC} - 300$ 3000 2200 1500	mV

DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Note 7) (Figures 6 & 8)

V_{th}	Input Threshold Reference Voltage Range (Note 8)	1050		$V_{CC} - 100$	mV
V_{IH}	Single-ended Input HIGH Voltage	$V_{th} + 100$		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage	GND		$V_{th} - 100$	mV
V_{ISE}	Single-ended Input Voltage ($V_{IH} - V_{IL}$)	200		1200	mV

DIFFERENTIAL IN0/IN0, IN1/IN1, INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 9) (Note 9)

V_{IHD}	Differential Input HIGH Voltage	1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		$V_{CC} - 100$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 10)	1050		$V_{CC} - 50$	mV
I_{IH}	Input HIGH Current (VTn Open)	-150		150	μA
I_{IL}	Input LOW Current (VTn Open)	-150		150	μA

CONTROL INPUT (SEL)

V_{IH}	Input HIGH Voltage	$V_{CC} \times 0.65$		V_{CC}	mV
V_{IL}	Input LOW Voltage	GND		$V_{CC} \times 0.35$	mV
I_{IH}	Input HIGH Current	-150		+150	μA
I_{IL}	Input LOW Current	-200		+200	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} .
- CML outputs loaded with $50\ \Omega$ to V_{CC} for proper operation.
- V_{th} , V_{IH} , V_{IL} and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

NB7V58M

Table 6. AC CHARACTERISTICS ($V_{CC} = 1.71\text{ V to }3.6\text{ V}$; $GND = 0\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$) (Note 11)

Symbol	Characteristic	Min	Typ	Max	Unit	
f_{MAX}	Maximum Input Clock Frequency $V_{outpp} \geq 200\text{ mV}$	7	8		GHz	
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)	10.7	12		Gbps	
f_{SEL}	Maximum Toggle Frequency, SEL	25	50		MHz	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 12) (Figures 8 & 10)	$f_{in} \leq 7\text{ GHz}$	200	400		mV
t_{PLH} , t_{PHL}	Propagation Delay to Differential Outputs, @ 1 GHz, measured at differential cross-point	IN_n/\overline{IN}_n to Q, \overline{Q} SEL to Q, \overline{Q}	120 5	180 13	240 22	ps ns
$t_{PLH\ TC}$	Propagation Delay Temperature Coefficient		50		$\Delta fs/^\circ C$	
t_{skew}	Device – Device skew ($t_{pdmax} - t_{pdmin}$)			50	ps	
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq 5.0\text{ GHz}$ $f_{in} \leq 7.0\text{ GHz}$	45 40	50 50	55 60	%
t_{JITTER}	RJ – Output Random Jitter (Note 13) DJ – Residual Output Deterministic Jitter (Note 14)	$f_{in} \leq 7.0\text{ GHz}$ $f_{in} \leq 10.7\text{ Gbps}$		0.2	0.8 10	ps RMS ps pk-pk
Φ_N	Phase Noise, $f_c = 1\text{ GHz}$	10 kHz 100 kHz 1 MHz 10 MHz 20 MHz 40 MHz		-135 -136 -150 -151 -151 -151		dBc
$t_{\Phi N}$	Integrated Phase Jitter (Figure 4) $f_c = 1\text{ GHz}$, 12 kHz – 20 MHz Offset (RMS)		35			fs
	Crosstalk Induced Jitter (Adjacent Channel) (Note 15)			0.7		ps RMS
V_{INPP}	Input Voltage Swing (Differential Configuration) (Figure 10) (Note 16)	100		1200		mV
t_r , t_f	Output Rise/Fall Times @ 1 GHz (20% – 80%)	Q, \overline{Q}	15	35	50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a $V_{INPPmin}$ source, 50% duty cycle clock source. All output loading with external $50\ \Omega$ to V_{CC} . Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23 at 3 Gbps.
15. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.
16. Input voltage swing is a single-ended measurement operating in differential mode.

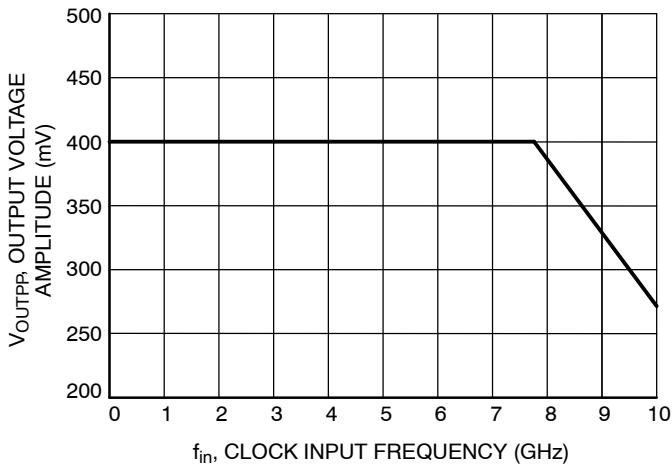


Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

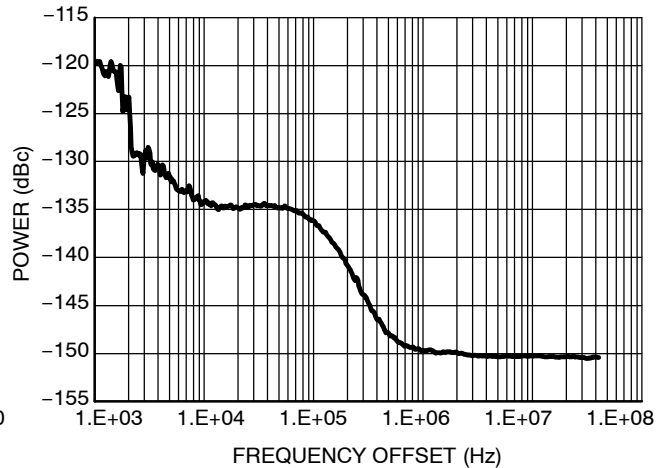


Figure 4. Typical Phase Noise ($V_{CC} = 1.8\text{ V}$, $T = 25^\circ\text{C}$, $f_c = 1\text{ GHz}$)

NB7V58M

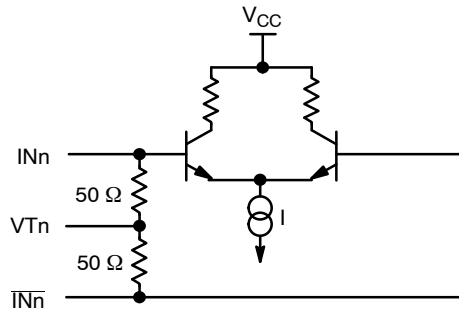


Figure 5. Input Structure

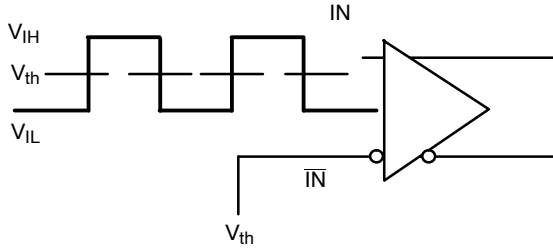


Figure 6. Differential Input Driven Single-Ended

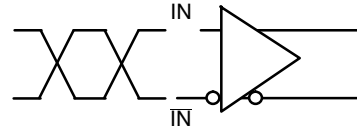


Figure 7. Differential Inputs Driven Differentially

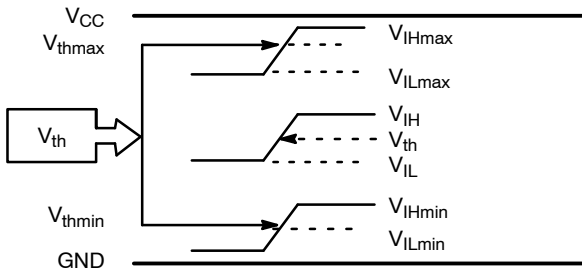


Figure 8. V_{th} Diagram

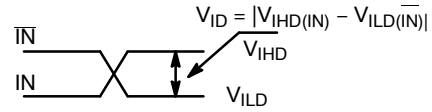


Figure 9. V_{ID} - Differential Inputs Driven Differentially

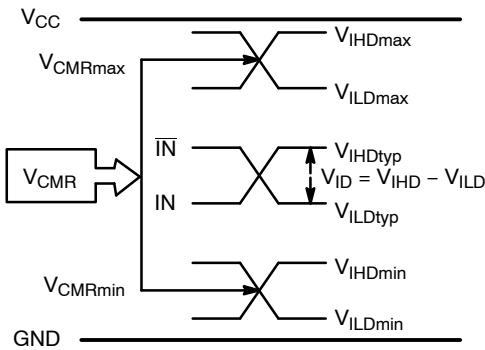


Figure 10. V_{CMR} Diagram

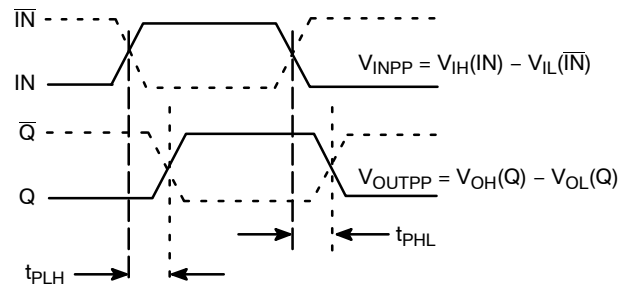


Figure 11. AC Reference Measurement

NB7V58M

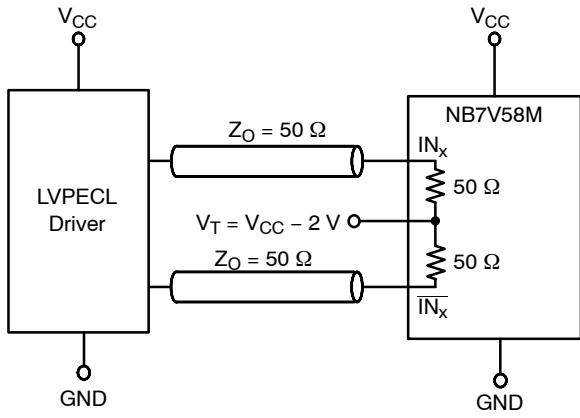


Figure 12. LVPECL Interface

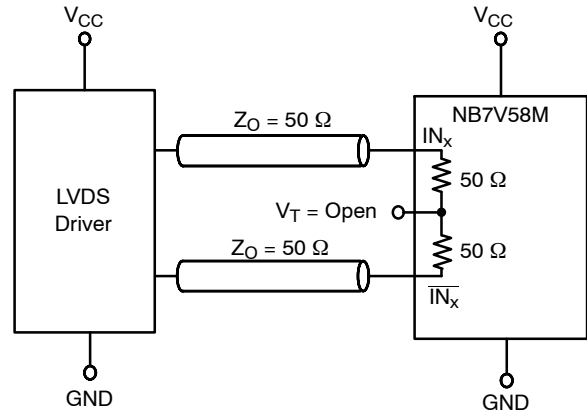


Figure 13. LVDS Interface

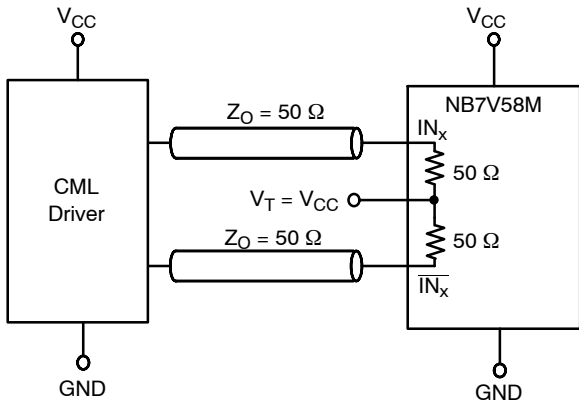


Figure 14. Standard 50 Ω Load CML Interface

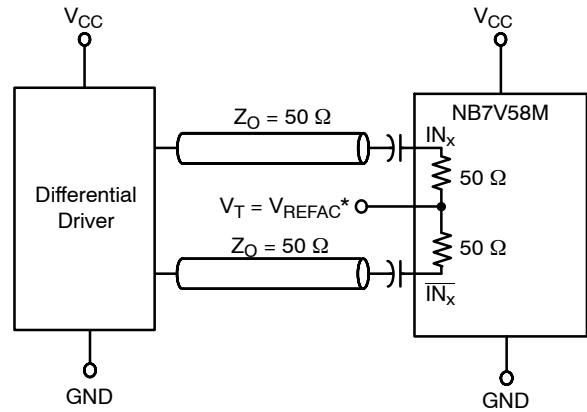


Figure 15. Capacitor-Coupled Differential Interface
(V_T Connected to External V_{REFAC})

* V_{REFAC} Bypassed to Ground with 0.01 μF Capacitor

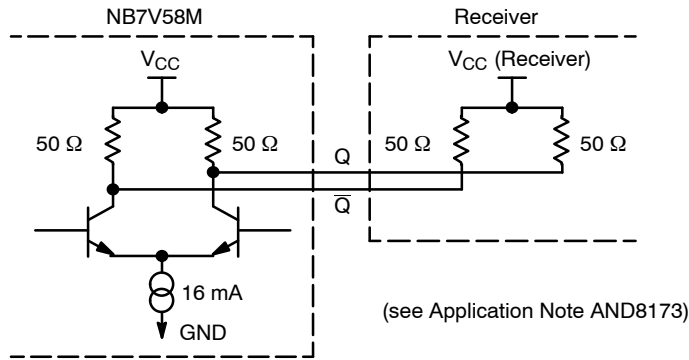


Figure 16. Typical CML Output Structure and Termination

ORDERING INFORMATION

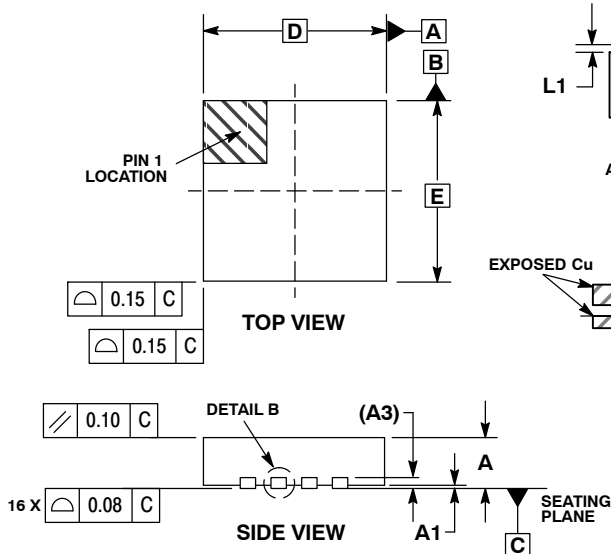
Device	Package	Shipping [†]
NB7V58MMNG	QFN-16 (Pb-Free)	123 Units / Rail
NB7V58MMNHTBG	QFN-16 (Pb-Free)	100 / Tape & Reel
NB7V58MMNTXG	QFN-16 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7V58M

PACKAGE DIMENSIONS

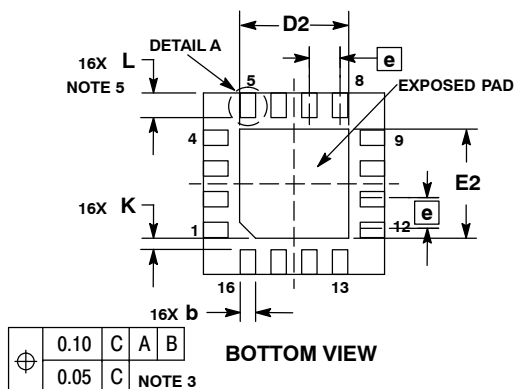
16 PIN QFN
CASE 485G-01
ISSUE D



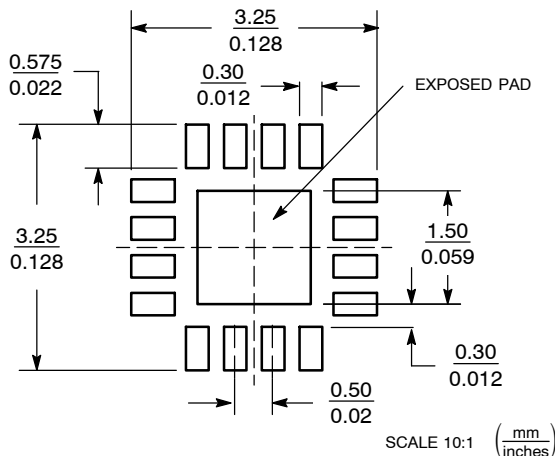
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50
L1	0.00	0.15



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GigaComm is a trademark of Semiconductor Component Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative