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NB4L339

2.5 V / 3.3 V Differential 2:1 Clock IN to Differential LVPECL Clock Generator / Divider / Fan-Out Buffer

Multi−Level Inputs w/ Internal Termination

Description

The NB4L339 is a multi−function Clock generator featuring a 2:1 Clock multiplexer front end and simultaneously outputs a selection of four different divide ratios from its four divider blocks; ÷1/÷2/÷4/÷8. One divide block has a choice of ÷1 or ÷ 2.

The output of each divider block is fanned−out to two identical differential LVPECL copies of the selected clock. All outputs provide standard LVPECL voltage levels when externally terminated with a 50−ohm resistor to V_{CC} − 2 V.

The differential Clock inputs incorporate internal 50−Ω termination resistors and will accept LVPECL, CML or LVDS logic levels.

The common Output Enable pin ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip−flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

This device is housed in a 5x5 mm 32 pin QFN package.

Features

- Maximum Input/Output Clock Frequency > 700 MHz
- Low Skew LVPECL Outputs, 15 ps typical
- 1 ns Typical Propagation Delay
- 150 ps Typical Rise and Fall Times
- 0.15 ps Typical RMS Phase Jitter
- 0.5 ps Typical RMS Random Clock Period Jitter
- LVPECL, CML or LVDS Input Compatible
- Operating Range: V_{CC} = 2.375 V to 3.6 V with V_{EE} = 0 V
- LVPECL Output Level; 750 mV Peak−to−Peak, Typical
- Internal 50−Ω Input Termination Provided
- Synchronous Output Enable/Disable
- Asynchronous Master Reset
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- −40°C to 85°C Ambient Operating Temperature
- 32−Pin QFN, 5 mm x 5 mm
- This is a Pb−Free Device

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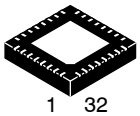
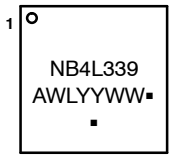


QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

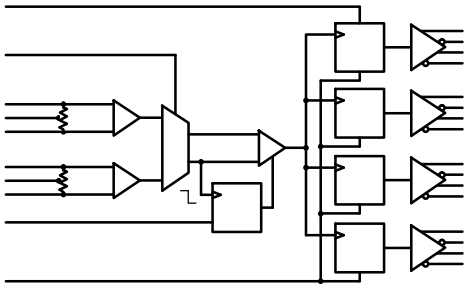


Figure 1. Simplified Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

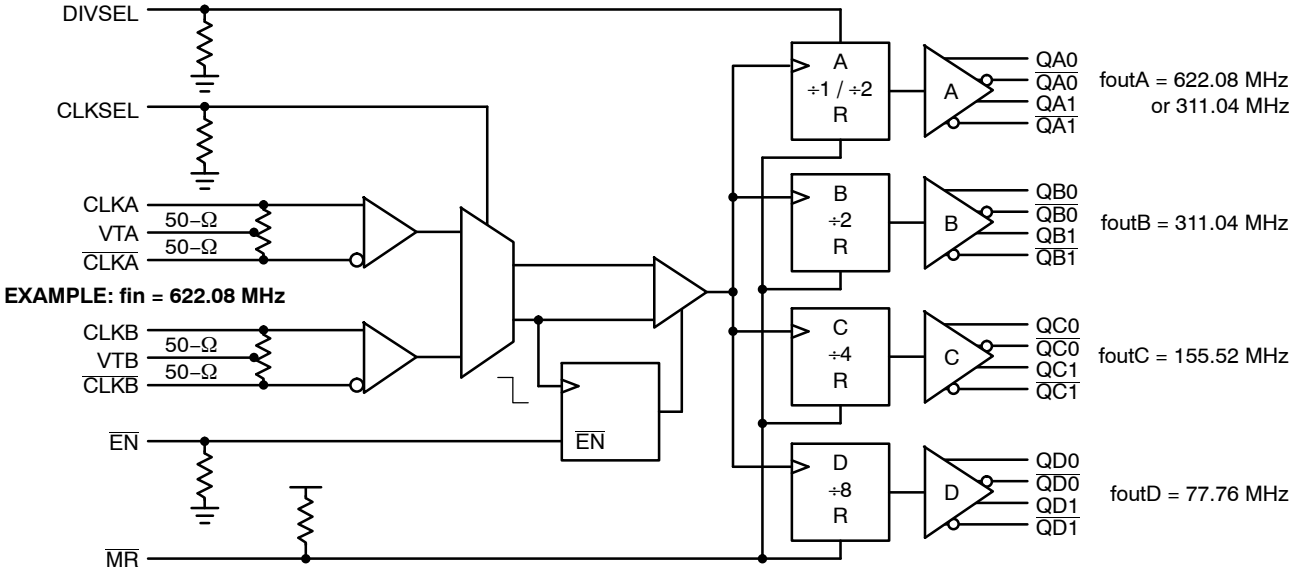


Figure 2. Detailed Logic Diagram

Table 1. Input Select Function Table

CLKSEL*	CLK Input Selected
0	CLKA
1	CLKB

Table 2. Divider Select Function Table

DIVSEL*	QA Divide
0	Divide by 1
1	Divide by 2

Table 3. Clock Enable/Disable Function Table

CLK Input	EN*	MR**	Function
Low to High Transition	0	H	Divide − Outputs Active
High to Low Transition	1	H	Hold Q − Outputs Inactive
X (Don't Care)	X (Don't Care)	L	Reset Q

* Pin will default LOW when left OPEN. ** Pin will default HIGH when left OPEN.

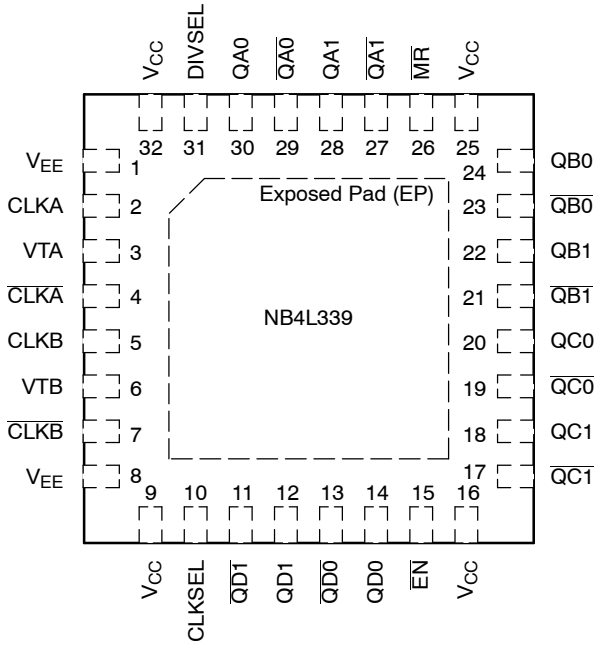


Figure 3. Pinout QFN−32 (Top View)

Table 4. Pin Description

Pin	Name	I/O	Description
1, 8, EP	V_{EE}	–	Negative Supply Voltage
2	CLKA	LVPECL, CML, LVDS Input	Non−inverted differential input (A). (Note 1)
3	VTA	–	Internal 100−Ω center−tapped termination pin for CLKA and $\overline{\text{CLKA}}$ (Note 1).
4	$\overline{\text{CLKA}}$	LVPECL, CML, LVDS Input	Inverted differential input (A). (Note 1)
5	CLKB	LVPECL, CML, LVDS Input	Non−inverted differential input (B). (Note 1)
6	VTB	–	Internal 100−Ω center−tapped termination pin for CLKB and $\overline{\text{CLKB}}$. (Note 1)
7	$\overline{\text{CLKB}}$	LVPECL, CML, LVDS Input	Inverted differential input (B). (Note 1)
9, 16, 25, 32	V_{CC}	–	Positive Supply Voltage
10	CLKSEL	LVCMOS/LVTTL	Asynchronous Clock input select pin. This pin defaults LOW when left open with 80 kΩ resistor to V_{EE}.
11	$\overline{\text{QD1}}$	LVPECL Output	Inverted differential (D1) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V
12	QD1	LVPECL Output	Non−inverted Differential (D1) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
13	$\overline{\text{QD0}}$	LVPECL Output	Inverted differential (D0) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
14	QD0	LVPECL Output	Non−inverted Differential (D0) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
15	$\overline{\text{EN}}$	LVCMOS/LVTTL	Synchronous Output Enable/Disable pin. This pin defaults LOW when left open with 80 kΩ resistor to V_{EE}.
17	$\overline{\text{QC1}}$	LVPECL Output	Inverted differential (C1) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
18	QC1	LVPECL Output	Non−inverted Differential (C1) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
19	$\overline{\text{QC0}}$	LVPECL Output	Inverted differential (C0) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
20	QC0	LVPECL Output	Non−inverted Differential (C0) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
21	$\overline{\text{QB1}}$	LVPECL Output	Inverted differential (B1) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
22	QB1	LVPECL Output	Non−inverted Differential (B1) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
23	$\overline{\text{QB0}}$	LVPECL Output	Inverted differential (B0) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
24	QB0	LVPECL Output	Non−inverted Differential (B0) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
26	$\overline{\text{MR}}$	LVCMOS/LVTTL	Master Reset Asynchronous. This pin defaults HIGH when left open with 80 kΩ resistor to V_{CC}.
27	$\overline{\text{QA1}}$	LVPECL Output	Inverted differential (A1) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
28	QA1	LVPECL Output	Non−inverted Differential (A1) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
29	$\overline{\text{QA0}}$	LVPECL Output	Inverted differential (A0) output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
30	QA0	LVPECL Output	Non−inverted Differential (A0) Output. Typically terminated with 50 Ω resistor to V_{CC} − 2 V.
31	DIVSEL	LVCMOS/LVTTL	Asynchronous Divide Select Pin selects A divide block outputs to divide by 1 or divide by 2. Defaults LOW when left open, divide−by−1, with 80 kΩ resistor to V_{EE}.
–	EP	–	Exposed Pad. The exposed pad (EP) on package bottom (see case drawing) is thermally connected to the die for improved heat transfer out of package and must be attached to a heat−sinking conduit. The pad is electrically connected to V_{EE} and must be connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pin (VTx / $\overline{\text{VTx}}$) are connected to a common termination voltage or left open, and if no signal is applied on CLKx / $\overline{\text{CLKx}}$ input then the device will be susceptible to self−oscillation.

Table 5. ATTRIBUTES

Characteristics		Value
Input Default State Resistors		80 kΩ
ESD Protection	Human Body Model Machine Model	> 2.0 kV > 100 V
Moisture Sensitivity (Note 2)	QFN−32	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		366
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 6. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		4.0	V
V_{IO}	Input/Output Voltage	V_{EE} = 0 V	$-0.5 = V_{Io} \le V_{CC} + 0.5$	4.0	V
V_{INPP}	Differential Input Voltage Swing |CLK − $\overline{CLK}$|			2.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA
I_{OUT}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range	QFN−32		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 LFPM 500 LFPM	QFN−32 QFN−32	31 27	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−32	12	°C/W
T_{sol}	Wave Solder (Pb−Free)			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 7. DC CHARACTERISTICS, CLOCK Inputs, LVPECL Outputs
V_{CC} = 2.375 V to 3.6 V, V_{EE} = 0 V, T_A = −40°C to +85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Inputs and Outputs Open)	58	70	90	mA
LVPECL Outputs (Note 4)					
V_{OH}	Output HIGH Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1135 2155 1355	V_{CC} − 1020 2280 1480	V_{CC} − 760 2540 1740	mV
V_{OL}	Output LOW Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1935 1355 555	V_{CC} − 1770 1530 730	V_{CC} − 1560 1740 940	mV
Differential Input Driven Single−Ended (see Figures 6 & 8)					
Vth	Input Threshold Reference Voltage Range (Note 6)	1125		V_{CC} − 75	mV
V_{IH}	Single−ended Input HIGH Voltage	Vth + 75		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		Vth − 75	mV
V_{ISE}	Single−ended Input Voltage (V_{IH} − V_{IL})	150		2800	mV
Differential Inputs Driven Differentially (see Figures 7 & 9)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{CC} − 150	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 8)	1125		V_{CC} − 75	mV
V_{ID}	Differential Input Voltage Swing (V_{IHD} − V_{ILD})	150		2800	mV
I_{IH}	Input HIGH Current CLKx / $\overline{CLKx}$ (VTx Open)	10		40	μA
I_{IL}	Input LOW Current CLKx / $\overline{CLKx}$ (VTx Open)	−10		10	μA
Single−Ended LVCMOS / LVTTL Control Inputs					
V_{IH}	Single−ended Input HIGH Voltage	2000		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE}		800	mV
I_{IH}	Input HIGH Current CLKSEL, DIVSEL, $\overline{EN}$ $\overline{MR}$	40 −10		115 10	μA
I_{IL}	Input LOW Current CLKSEL, DIVSEL, $\overline{EN}$ $\overline{MR}$	−10 −115		10 −40	μA
Termination Resistors					
R_{TIN}	Internal Input Termination Resistor (Measured across CLKx and $\overline{CLKx}$)	80	100	120	Ω
R_{TIN}	Internal Input Termination Resistor (Measured from CLKx to VTx)	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVPECL outputs require 50 Ω receiver termination resistors to V_{CC} − 2 V for proper operation.
5. Input and output parameters vary 1:1 with V_{CC}.
6. Vth is applied to the complementary input when operating in single−ended mode.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
8. V_{CMR} min varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 8. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.6 V, V_{EE} = 0 V (Note 9)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
fin_{max}	Maximum Input CLOCK Frequency	700			700			700			MHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figure 4) $f_{in} \le 622$ MHz	530	730		530	730		530	730		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential ÷ 1 CLKx/$\overline{CLKx}$ to Qx/$\overline{Qx}$	0.8	1.0	1.3	0.8	1.0	1.3	0.8	1.0	1.3	ns
	$\overline{MR}$ to Qx	1.2	–	5.0	1.2	–	5.0	1.2	–	5.0	
	CLKSEL to Qx	0.8	1.0	1.3	0.8	1.0	1.3	0.8	1.0	1.3	
trr	Reset Recovery	4.0			4.0			4.0			ns
DCO	Output CLOCK Duty Cycle All Divides	40		60	40		60	40		60	%
t_{SKEW}	Within Device Skew (Note 11)		30	60		30	60		30	60	ps
	Device to Device Skew (Note 12)		90	190		90	190		90	190	
t_s	Setup Time @ 50 MHz $\overline{EN}$ to CLKx	900			900			900			ps
	DIVSEL to CLKx	−100			−100			−100			
t_h	Hold Time @ 50 MHz CLKx to $\overline{EN}$	800			800			800			ps
	CLKx to DIVSEL	0			0			0			
t_{PW}	Minimum Pulse Width $\overline{MR}$	5.0			5.0			5.0			ns
Φ_N	Phase Noise f_{in} = 622.08 MHz Outputs (A) Div by 1										dBc
	10 kHz					−136					
	100 kHz					−136					
	1 MHz					−141					
	10 MHz					−141					
	20 MHz					−141					
	40 MHz					−141					
t_{JIT1}	Integrated Phase Jitter (Figure 4) f_{in} = 622.08 MHz, 12 kHz – 20 MHz Offset All Divides		0.15	0.25		0.15	0.25		0.15	0.25	ps RMS
t_{JIT2}	Random Clock Period Jitter (Note 13) f_{in} = 622.08 MHz All Divides		0.5	1.5		0.5	1.5		0.5	1.5	ps RMS
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14)	150			150			150			mV
t_r, t_f	Output Rise/Fall Times @ 622.08 MHz input frequency (20% – 80%)		150	250		150	250		150	250	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Measured by forcing V_{INPP} (Min) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC} – 2 V Input edge rates 100 ps (20% – 80%).
10. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 50 MHz.
11. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross−point of the inputs to the cross−point of the outputs.
12. Device to device skew is measured between outputs under identical transition @ 50 MHz.
13. Additive RMS jitter with 50% duty cycle clock signal; all inputs and outputs active.
14. V_{INPP} (Max) cannot exceed V_{CC} – V_{EE}. Input voltage swing is a single−ended measurement operating in differential mode.

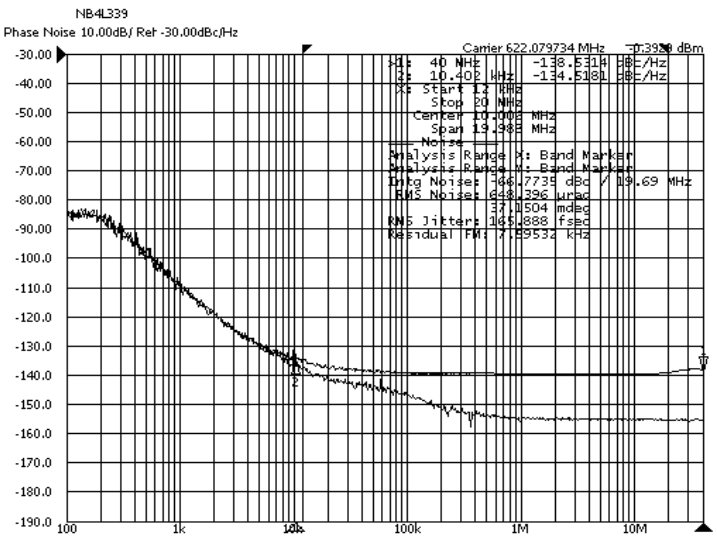


Figure 4. NB4L339 vs. Agilent 8665A 622.08 MHz at 3.3 V, Room Ambient

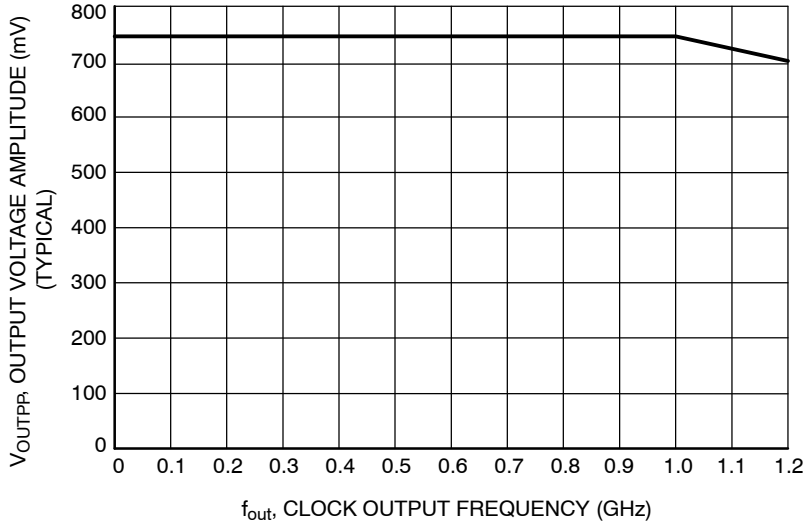


Figure 5. Output Voltage Amplitude (V_{OUTPP}) vs. Input Clock Frequency (f_{in}) at Ambient Temperature (Typical)

Application Information

The NB4L339 is a high−speed, Clock multiplexer, divider and low skew fan−out buffer featuring a 2:1 Clock multiplexer front end and outputs a selection of four different divide ratios; ÷1/2/4/8. One divide block has a choice of ÷1 or ÷ 2. The outputs of all four divider blocks are fanned−out to two pair of identical differential LVPECL copies of the selected clock. All outputs provide standard LVPECL voltage levels when externally terminated with a 50−ohm resistor to $V_{TT} = V_{CC} - 2$ V.

The differential Clock input buffers incorporate internal 50−Ω termination resistors in a 100−Ω center−tapped configuration and are accessible via a VTx pin. This feature provides transmission line termination on−chip, at the receiver end, eliminating external components. Inputs CLKA/B and $\overline{\text{CLKA}}/\overline{\text{B}}$ must be signal driven or auto oscillation may result.

The NB4L339 Clock inputs can be driven by a variety of differential signal level technologies including LVDS, LVPECL, or CML.

The internal dividers are synchronous to each other. Therefore, the common output edges are precisely aligned.

The Output Enable pin ($\overline{\text{EN}}$) is synchronous so that the internal divider flip−flops will only be enabled/disabled when the internal clock is in the LOW state. This avoids any chance of generating a runt pulse on the internal clock when the device is enabled/disabled, as can happen with an asynchronous control. The internal enable flip−flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Master Reset ($\overline{\text{MR}}$) is asynchronous. When $\overline{\text{MR}}$ is forced LOW, all Q outputs go to logic LOW.

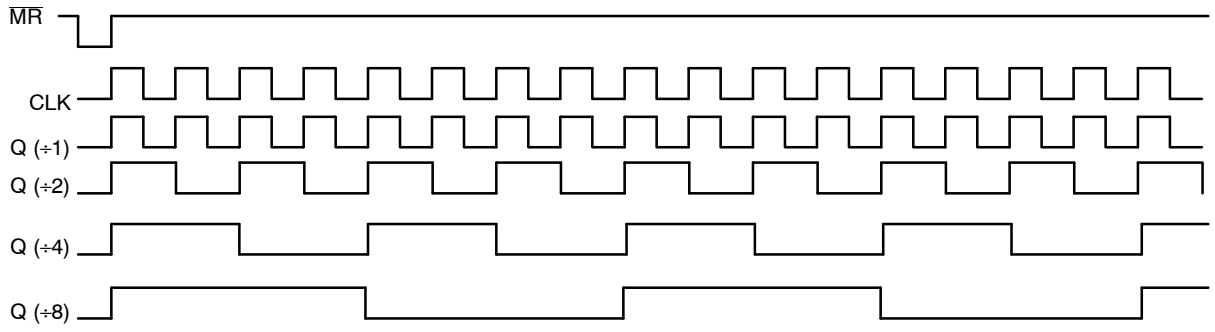
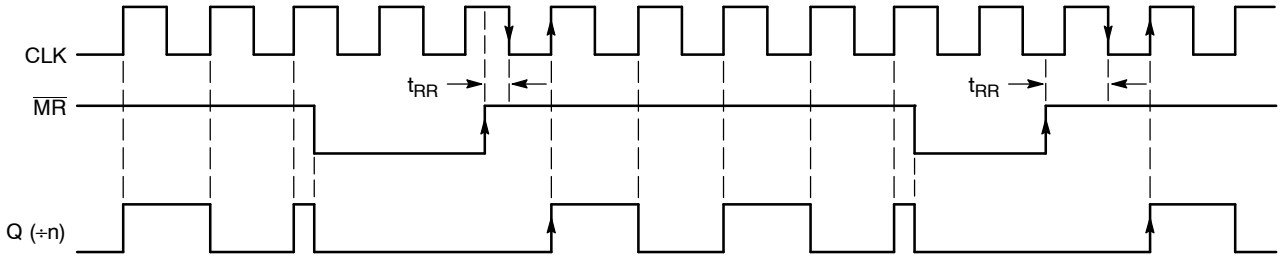


Figure 6. Timing Diagram



NOTE: On the rising edge of $\overline{MR}$, Q goes HIGH after the first rising edge of CLK, following a high−to−low clock transition.

Figure 7. Master Reset Timing Diagram

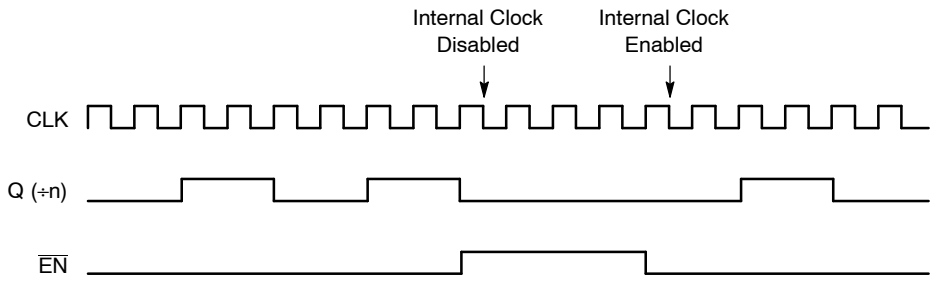


Figure 8. Output Enable Timing Diagrams

The $\overline{EN}$ signal will “freeze” the internal divider flip−flops on the first falling edge of CLK after its assertion. The internal divider flip−flops will maintain their state during the freeze. When $\overline{EN}$ is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip−flops will “unfreeze” and continue to their next state count with proper phase relationships.

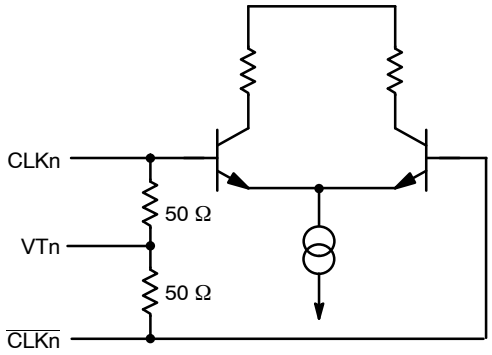


Figure 9. Input Structure

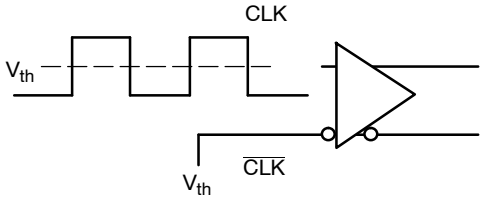


Figure 10. Differential Input Driven Single−Ended

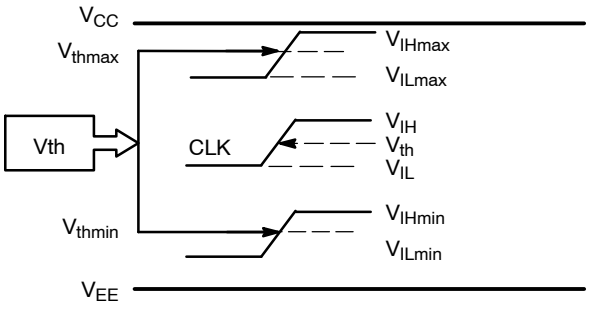


Figure 11. V_{th} Diagram

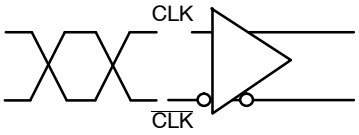


Figure 12. Differential Inputs Driven Differentially

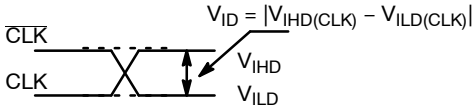


Figure 13. Differential Inputs Driven Differentially

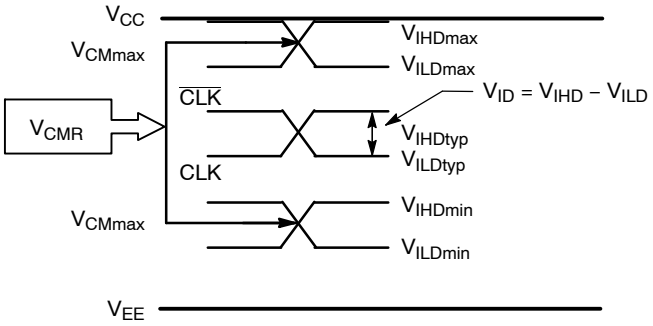


Figure 14. VCMR Diagram

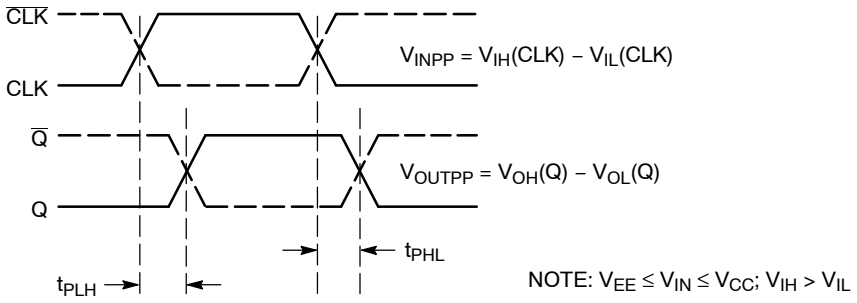


Figure 15. AC Reference Measurement

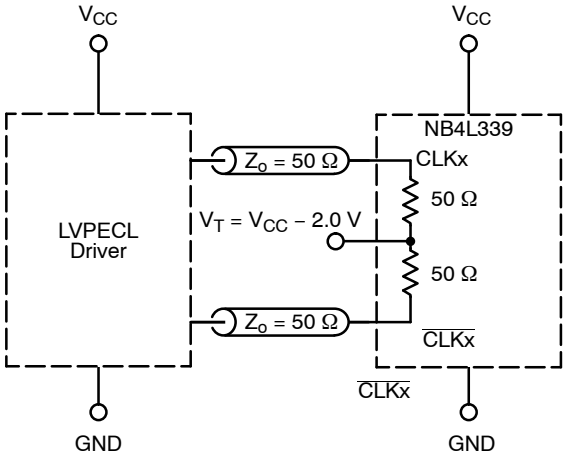


Figure 16. LVPECL Interface

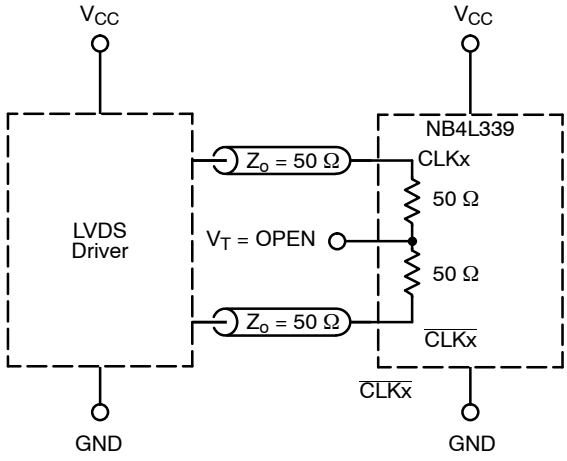


Figure 17. LVDS Interface

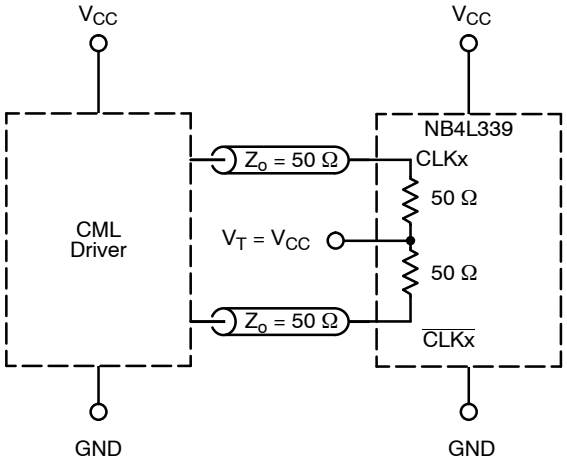


Figure 18. Standard 50 Ω Load CML Interface

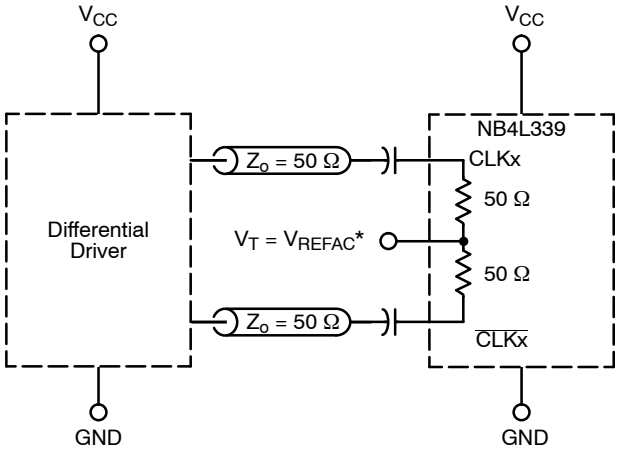


Figure 19. Capacitor−Coupled Differential Interface (V_T Connected to External V_{REFAC})

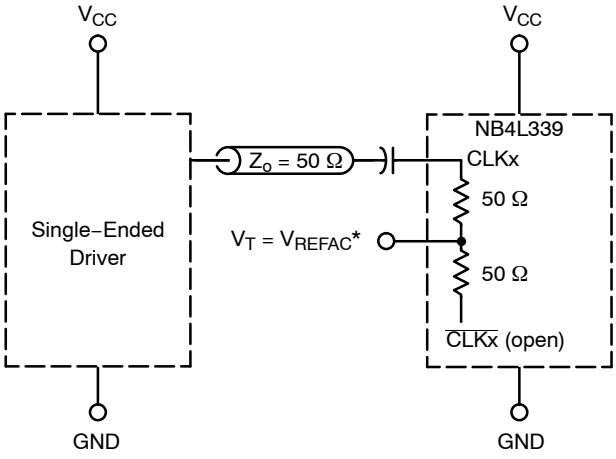


Figure 20. Capacitor−Coupled Single−Ended Interface (V_T Connected to External V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor.

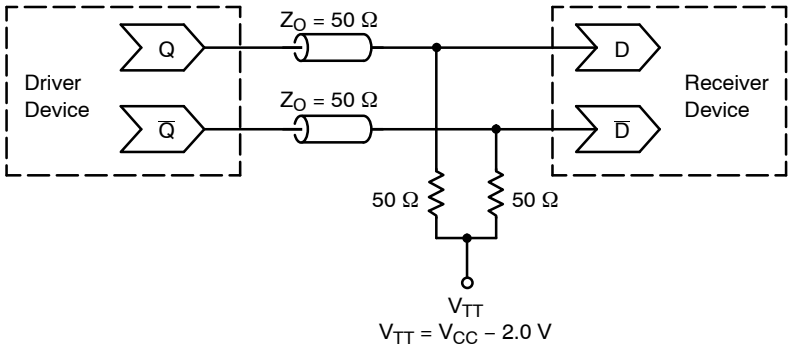


Figure 21. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D − Termination of ECL Logic Devices)

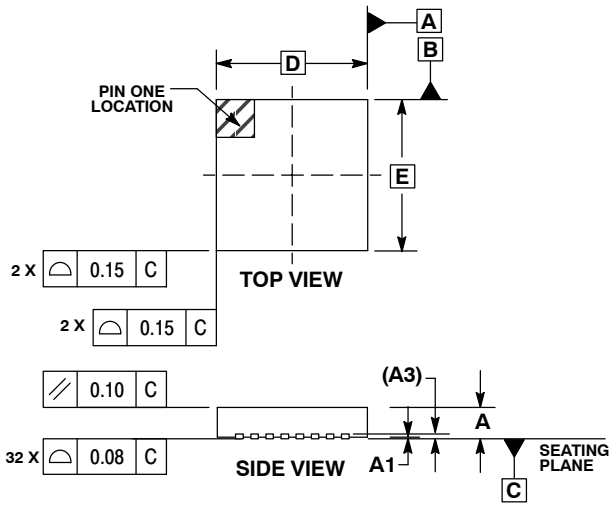
ORDERING INFORMATION

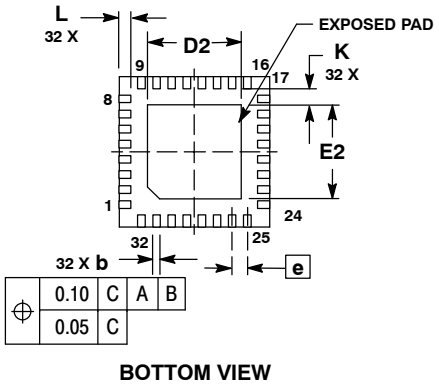
Device	Package	Shipping†
NB4L339MNG	QFN32 (Pb−free)	74 Units / Tray
NB4L339MNR4G	QFN32 (Pb−free)	1000 / Tape & Reel

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

QFN32 5x5, 0.5 P
CASE 488AM
ISSUE O



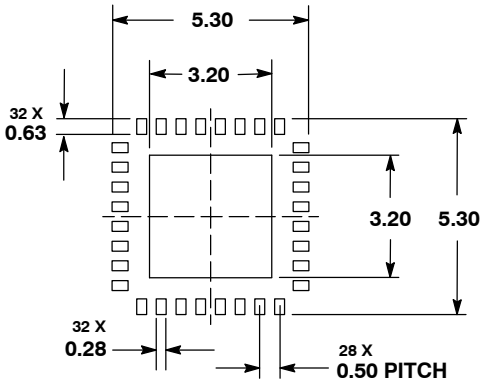


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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