

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

# NB100LVEP221

## 2.5V/3.3V 2:1:20 Differential HSTL/ECL/PECL Clock Driver

### Description

The NB100LVEP221 is a low skew 2:1:20 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The two clock inputs are differential ECL/PECL; CLK1/ $\overline{\text{CLK1}}$  can also receive HSTL signal levels. The LVPECL input signals can be either differential configuration or single-ended (if the  $V_{\text{BB}}$  output is used).

The LVEP221 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure tightest skew, both sides of differential outputs should be terminated identically into 50  $\Omega$  even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The NB100LVEP221, as with most other ECL devices, can be operated from a positive  $V_{\text{CC}}$  supply in LVPECL mode. This allows the LVEP221 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on PECL terminations, designers should refer to Application Note AND8020/D.

The  $V_{\text{BB}}$  pin, an internally generated voltage supply, is available to this device only. For single-ended LVPECL input conditions, the unused differential input is connected to  $V_{\text{BB}}$  as a switching reference voltage.  $V_{\text{BB}}$  may also rebias AC coupled inputs. When used, decouple  $V_{\text{BB}}$  and  $V_{\text{CC}}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{\text{BB}}$  should be left open.

Single-ended CLK input operation is limited to a  $V_{\text{CC}} \geq 3.0$  V in LVPECL mode, or  $V_{\text{EE}} \leq -3.0$  V in NECL mode.

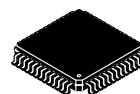
### Features

- 15 ps Typical Output-to-Output Skew
- 40 ps Typical Device-to-Device Skew
- Jitter Less than 2 ps RMS
- Maximum Frequency > 1.0 GHz Typical
- Thermally Enhanced 52-Lead LQFP and QFN
- $V_{\text{BB}}$  Output
- 540 ps Typical Propagation Delay
- LVPECL and HSTL Mode Operating Range:  
 $V_{\text{CC}} = 2.375$  V to 3.8 V with  $V_{\text{EE}} = 0$  V
- NECL Mode Operating Range:  
 $V_{\text{CC}} = 0$  V with  $V_{\text{EE}} = -2.375$  V to -3.8 V
- Q Output will Default Low with Inputs Open or at  $V_{\text{EE}}$
- Pin Compatible with Motorola MC100EP221
- These Devices are Pb-Free and are RoHS Compliant



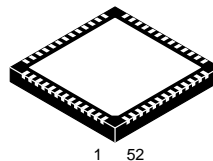
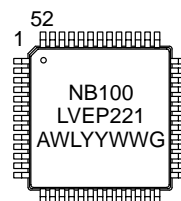
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

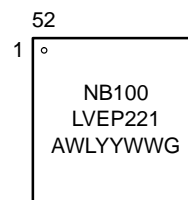


LQFP-52  
FA SUFFIX  
CASE 848H

### MARKING DIAGRAMS\*



QFN-52  
MN SUFFIX  
CASE 485M



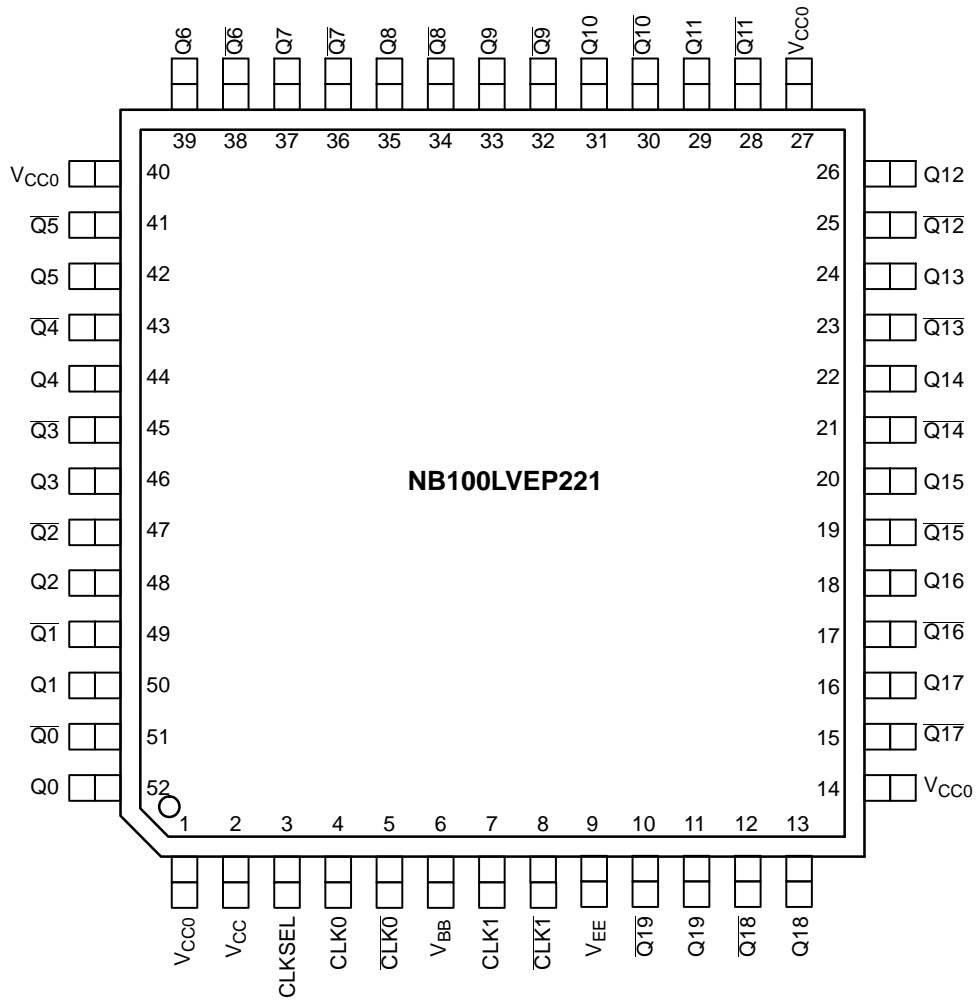
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# NB100LVEP221



All  $V_{CC}$ ,  $V_{CC0}$ , and  $V_{EE}$  pins must be externally connected to appropriate Power Supply to guarantee proper operation. The thermally conductive exposed pad on package bottom (see package case drawing) must be attached to a heat-sinking conduit, capable of transferring 1.2 Watts. This exposed pad is electrically connected to  $V_{EE}$  internally.

**Figure 1. 52-Lead LQFP Pinout (Top View)**

# NB100LVEP221

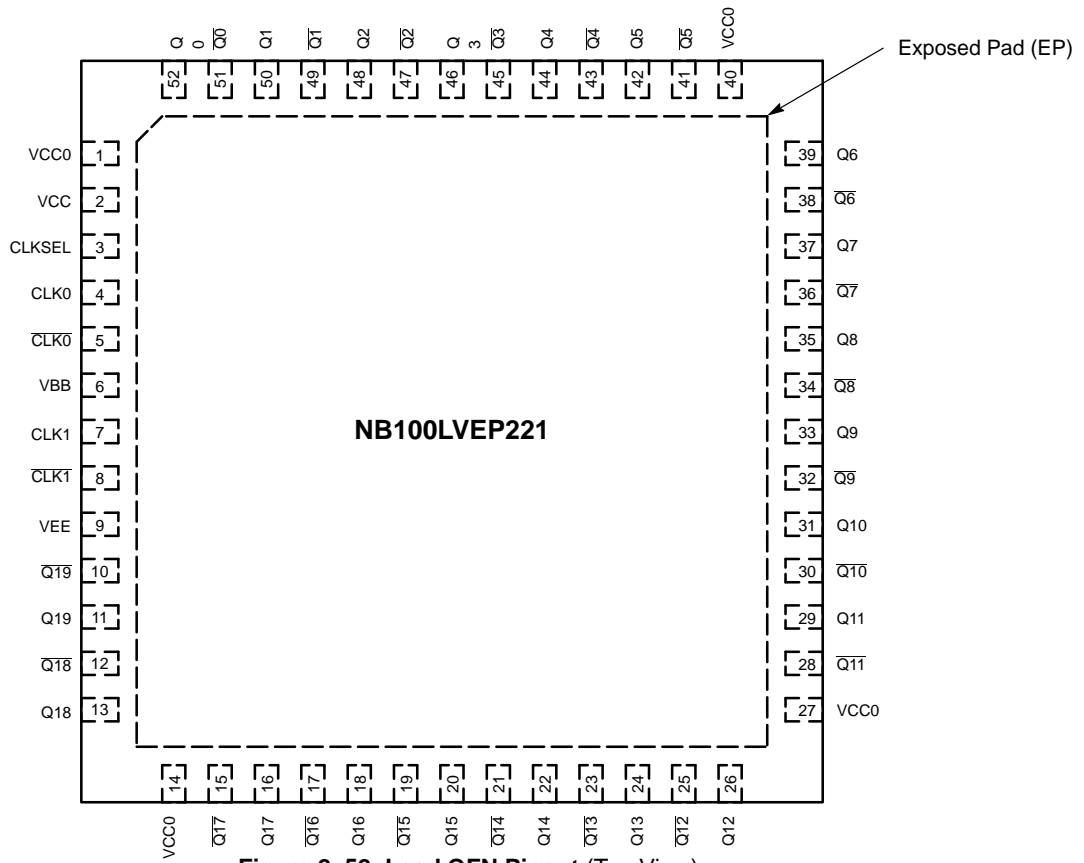


Figure 2. 52-Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK0*, $\overline{\text{CLK0}}$ **	ECL/PECL Differential Inputs
CLK1*, $\overline{\text{CLK1}}$ **	ECL/PECL or HSTL Differential Inputs
Q0:19, $\overline{\text{Q0}}$ : $\overline{\text{Q19}}$	ECL/PECL Differential Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub> /V <sub>CC0</sub>	Positive Supply
V <sub>EE</sub> ***	Negative Supply

\* Pins will default LOW when left open.

\*\* Pins will default HIGH when left open.

\*\*\* The thermally conductive exposed pad on the bottom of the package is electrically connected to V<sub>EE</sub> internally.

Table 2. FUNCTION TABLE

CLK_SEL	Active Input
L	CLK0, $\overline{\text{CLK0}}$
H	CLK1, $\overline{\text{CLK1}}$

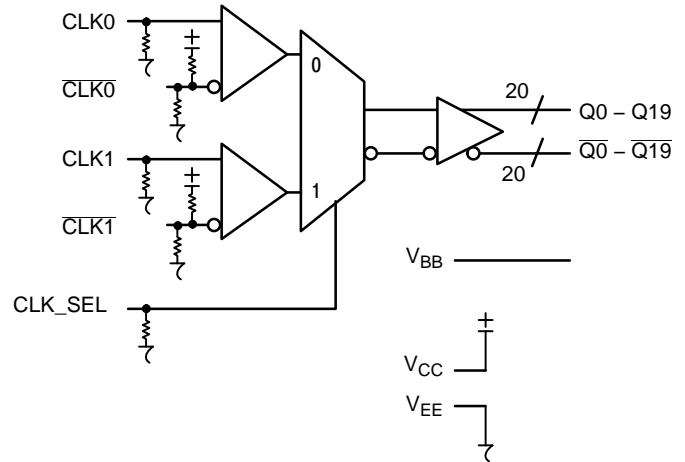


Figure 3. Logic Diagram

# NB100LVEP221

**Table 3. ATTRIBUTES**

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb-Free Pkg
		LQFP-52 QFN-52
		Level 3 Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		533 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 -6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (See Application Information)	0 lfpm 500 lfpm	LQFP-52 LQFP-52	35.6 30	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case) (See Application Information)	0 lfpm 500 lfpm	LQFP-52 LQFP-52	3.2 6.4	°C/W °C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (Note )	0 lfpm 500 lfpm	QFN-52 QFN-52	25 19.6	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case) (Note )	2S2P	QFN-52	21	°C/W
T <sub>sol</sub>	Wave Solder	Pb Pb-Free		265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# NB100LVEP221

**Table 5. LVPECL DC CHARACTERISTICS**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
$V_{OH}$	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{OL}$	Output LOW Voltage (Note 3)	555	680	900	555	680	900	555	680	900	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 4)	555		900	555		900	555		900	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) CLK0/CLK0 CLK1/CLK1	1.2 0.3		2.5 1.6	1.2 0.3		2.5 1.6	1.2 0.3		2.5 1.6	V V
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary + 0.125 V to -1.3 V.
- All outputs loaded with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .
- Do not use  $V_{BB}$  at  $V_{CC} < 3.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 6. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 7)	1355	1480	1700	1355	1480	1700	1355	1480	1700	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1700	1355		1700	1355		1700	mV
$V_{BB}$	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) CLK0/CLK0 CLK1/CLK1	1.2 0.3		3.3 1.6	1.2 0.3		3.3 1.6	1.2 0.3		3.3 1.6	V V
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary + 0.925 V to -0.5 V.
- All outputs loaded with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .
- Single-ended input operation is limited  $V_{CC} \geq 3.0\text{ V}$  in LVPECL mode.
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# NB100LVEP221

**Table 7. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.375\text{ V}$  to  $-3.8\text{ V}$  (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
$V_{OH}$	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 11)	-1945	-1820	-1600	-1945	-1820	-1600	-1945	-1820	-1600	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
$V_{BB}$	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)  CLK0/ $\overline{\text{CLK0}}$ CLK1/ $\overline{\text{CLK1}}$		$V_{EE} + 1.2$ $V_{EE} + 0.3$	0.0 -0.9		$V_{EE} + 1.2$ $V_{EE} + 0.3$	0.0 -0.9		$V_{EE} + 1.2$ $V_{EE} + 0.3$	0.0 -0.9	V V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current CLK $\overline{\text{CLK}}$	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

10. Input and output parameters vary 1:1 with  $V_{CC}$ .

11. All outputs loaded with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

12. Single-ended input operation is limited  $V_{EE} \leq -3.0\text{ V}$  in NECL mode.

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 8. HSTL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage CLK1/ $\overline{\text{CLK1}}$	$V_x + 100$		1600	$V_x + 100$		1600	$V_x + 100$		1600	mV
$V_{IL}$	Input LOW Voltage CLK1/ $\overline{\text{CLK1}}$	-300		$V_x - 100$	-300		$V_x - 100$	-300		$V_x - 100$	mV
$V_x$	Differential Configuration Cross Point Voltage	680		900	680		900	680		900	mV
$I_{IH}$	Input HIGH Current	-150		150	-150		150	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current CLK1 $\overline{\text{CLK1}}$	-150 -250			-150 -250			-150 -250			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

# NB100LVEP221

**Table 9. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -2.375\text{ to }-3.8\text{ V}$  or  $V_{CC} = 2.375\text{ to }3.8\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$V_{Opp}$	Differential Output Voltage (Figure 4)	$f_{out} < 50\text{ MHz}$	550	700		600	700		600	700		mV
		$f_{out} < 0.8\text{ GHz}$	550	700		550	700		500	700		mV
		$f_{out} < 1.0\text{ GHz}$	500	700		500	700		400	600		mV
$t_{PLH}/t_{PHL}$	Propagation Delay (Differential Configuration) CLK0-Qx CLK1-Qx		540	600		540	660		540	750		ps
			590	640		590	710		590	800		ps
$t_{skew}$	Within-Device Skew (Note 15)		15	50		15	50		15	50		ps
	Device-to-Device Skew (Note 16)		40	200		40	200		40	200		ps
$t_{JITTER}$	Random Clock Jitter (RMS) (Figure 4)		1	2		1	2		1	2		ps
$V_{PP}$	Input Swing (Differential Configuration) (Note 17) (Figure 5)	CLK0	400	800	1200	400	800	1200	400	800	1200	mV
		CLK1 HSTL	300	800	1000	300	800	1000	300	800	1000	mV
DCO	Output Duty Cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5		%
$t_r/t_f$	Output Rise/Fall Time (20%–80%)	100	200	300	100	200	300	150	250	350		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

14. Measured with 750 mV source (LVPECL) or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50  $\Omega$  to  $V_{CC}-2\text{ V}$ .

15. Skew is measured between outputs under identical transitions and conditions on any one device.

16. Device-to-Device skew for identical transitions, outputs and  $V_{CC}$  levels.

17.  $V_{PP}$  is the differential configuration input voltage swing required to maintain AC characteristics.



# NB100LVEP221

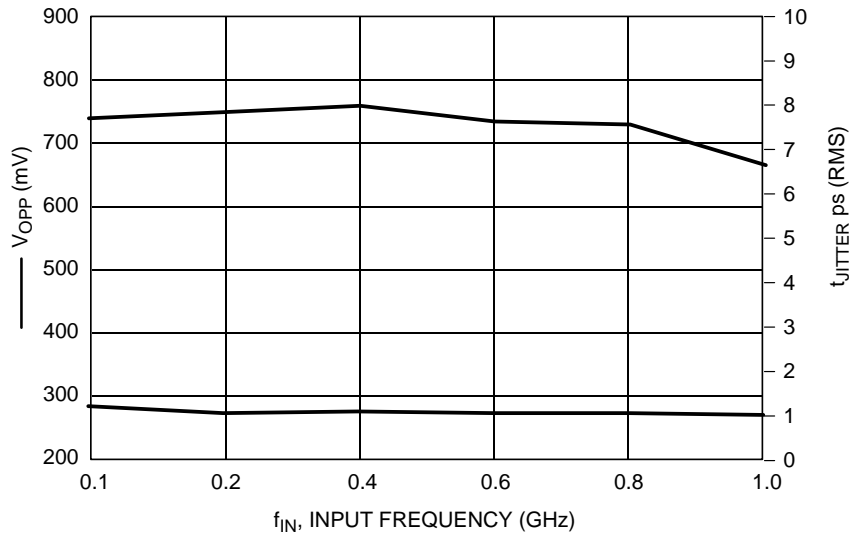


Figure 4. Output Voltage ( $V_{OPP}$ )/Jitter versus Input Frequency ( $V_{CC} - V_{EE} = 3.3 \text{ V} @ 25^\circ\text{C}$ )

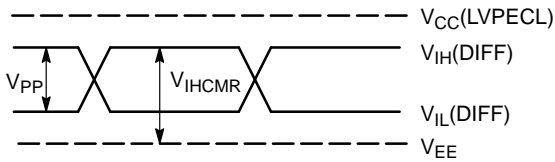


Figure 5. LVPECL Differential Input Levels

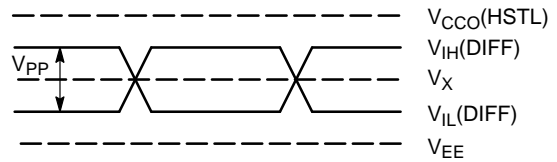


Figure 6. HSTL Differential Input Levels

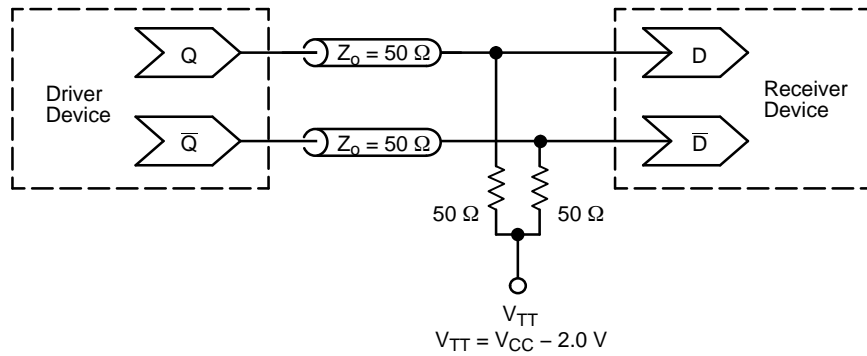


Figure 7. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

APPLICATIONS INFORMATION

Using the thermally enhanced package of the NB100LVEP221

The NB100LVEP221 uses a thermally enhanced 52-lead LQFP package. The package is molded so that a portion of the leadframe is exposed at the surface of the package bottom side. This exposed metal pad will provide the low thermal impedance that supports the power consumption of the NB100LVEP221 high-speed bipolar integrated circuit and will ease the power management task for the system design. In multilayer board designs, a thermal land pattern on the printed circuit board and thermal vias are recommended to maximize both the removal of heat from the package and electrical performance of the NB100LVEP221. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area should be at least the same size and shape as the exposed pad on the package. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal conduit. The thermal vias will connect the exposed pad of the package to internal copper planes of the board. The number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern.

The recommended thermal land design for NB100LVEP221 applications on multi-layer boards comprises a 4 X 4 thermal via array using a 1.2 mm pitch as shown in Figure 8 providing an efficient heat removal path.

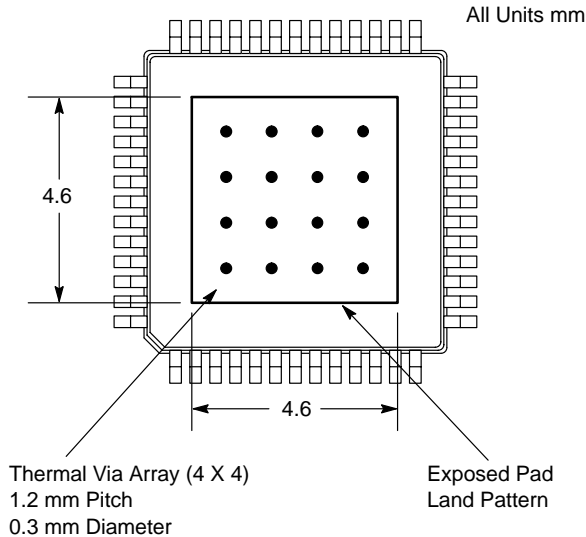


Figure 8. Recommended Thermal Land Pattern

The via diameter should be approximately 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via may result in voiding during the solder process and must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will

supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for the exposed pad package is equivalent to standard surface mount packages. Figure 9, “Recommended solder mask openings”, shows a recommended solder mask opening with respect to a 4 X 4 thermal via array. Because a large solder mask opening may result in a poor rework release, the opening should be subdivided as shown in Figure 9. For the nominal package standoff of 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

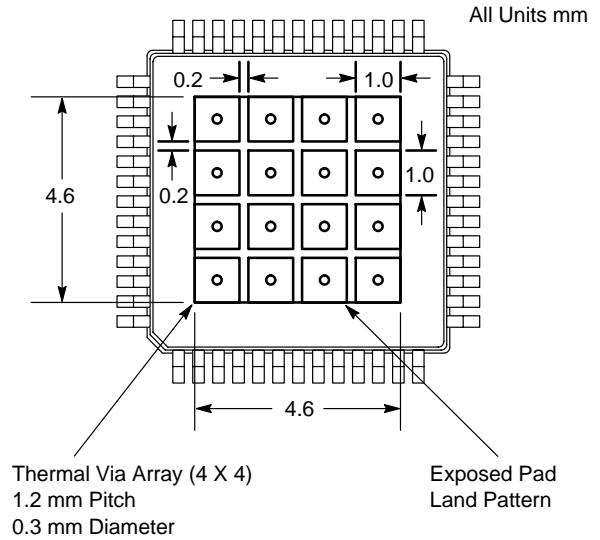


Figure 9. Recommended Solder Mask Openings

Proper thermal management is critical for reliable system operation. This is especially true for high-fanout and high output drive capability products.

For thermal system analysis and junction temperature calculation, the thermal resistance parameters of the package are provided:

Table 10. Thermal Resistance \*

Ifpm	$\theta_{JA}$ °C/W	$\theta_{JC}$ °C/W
0	35.6	3.2
100	32.8	4.9
500	30.0	6.4

\* Junction to ambient and Junction to board, four-conductor layer test board (2S2P) per JESD 51-8

These recommendations are to be used as a guideline, only. It is therefore recommended that users employ sufficient thermal modeling analysis to assist in applying the general recommendations to their particular application to assure adequate thermal performance. The exposed pad of the NB100LVEP221 package is electrically shorted to the substrate of the integrated circuit and  $V_{EE}$ . The thermal land should be electrically connected to  $V_{EE}$ .

# NB100LVEP221

## ORDERING INFORMATION

Device	Package	Shipping†
NB100LVEP221FAG	LQFP-52 (Pb-Free)	160 Units / Tray
NB100LVEP221FARG	LQFP-52 (Pb-Free)	1500 / Tape & Reel
NB100LVEP221MNG	QFN-52 (Pb-Free)	260 Units / Tray
NB100LVEP221MNR2G	QFN-52 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

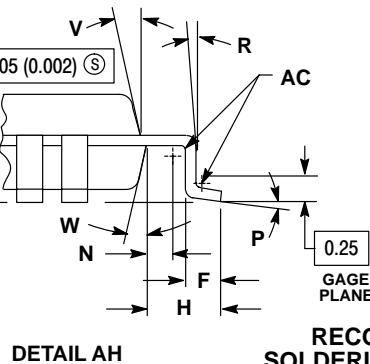
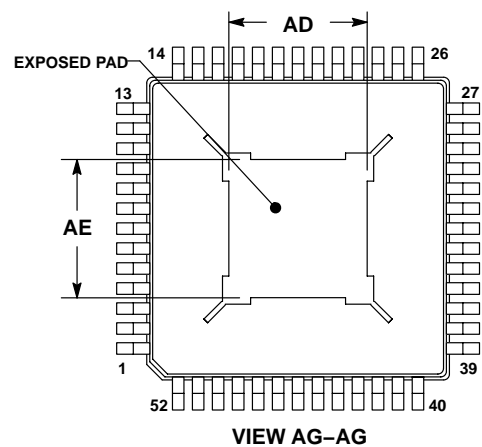
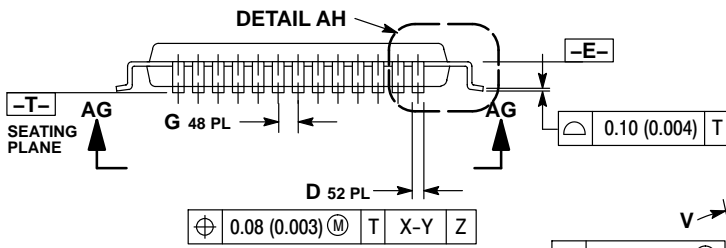
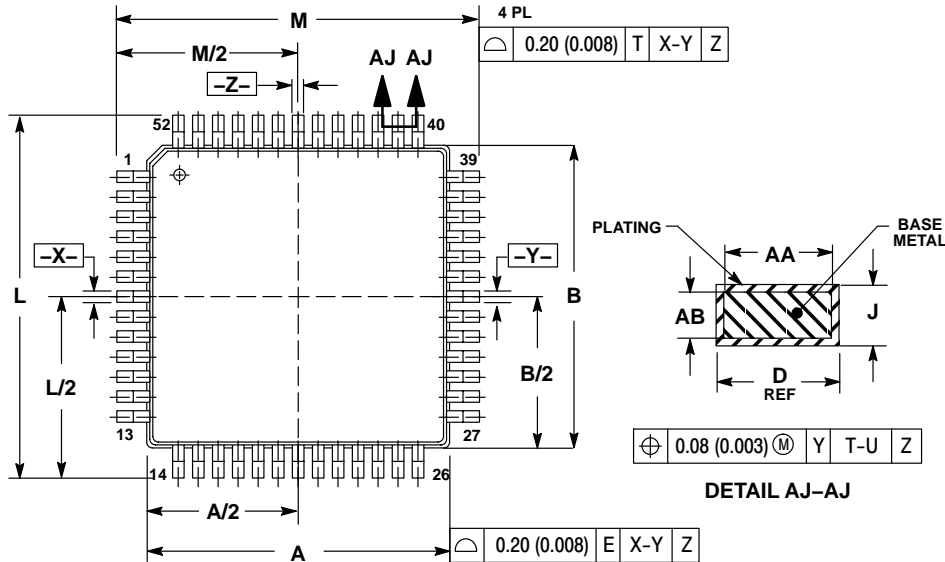
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# NB100LVEP221

## PACKAGE DIMENSIONS

### LQFP 52 EXPOSED PAD CASE 848H ISSUE B

SCALE 1:1

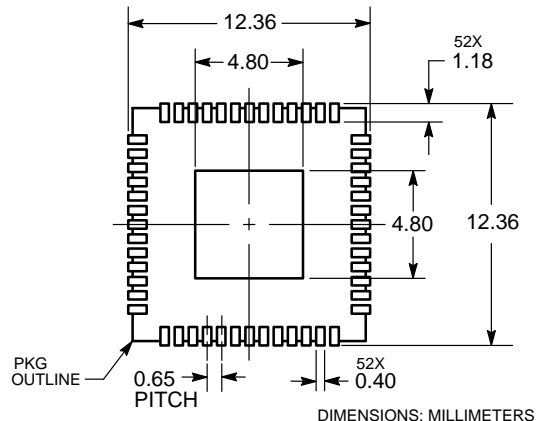


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM PLANE "E" IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
4. DATUM "X", "Y" AND "Z" TO BE DETERMINED AT DATUM PLANE DATUM "E".
5. DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM "T".
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE "E".
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
B	10.00 BSC		0.394 BSC	
C	1.30	1.50	0.051	0.059
D	0.22	0.40	0.009	0.016
F	0.45	0.75	0.018	0.030
G	0.65 BSC		0.026 BSC	
H	1.00 REF		0.039 REF	
J	0.09	0.20	0.004	0.008
K	0.05	0.20	0.002	0.008
L	12.00 BSC		0.472 BSC	
M	12.00 BSC		0.472 BSC	
N	0.20 REF		0.008 REF	
P	0°	7°	0°	7°
R	0°	---	0°	---
S	---	1.70	---	0.067
V	12° REF		12° REF	
W	12° REF		12° REF	
AA	0.20	0.35	0.008	0.014
AB	0.07	0.16	0.003	0.006
AC	0.08	0.20	0.003	0.008
AD	4.58	4.78	0.180	0.188
AE	4.58	4.78	0.180	0.188

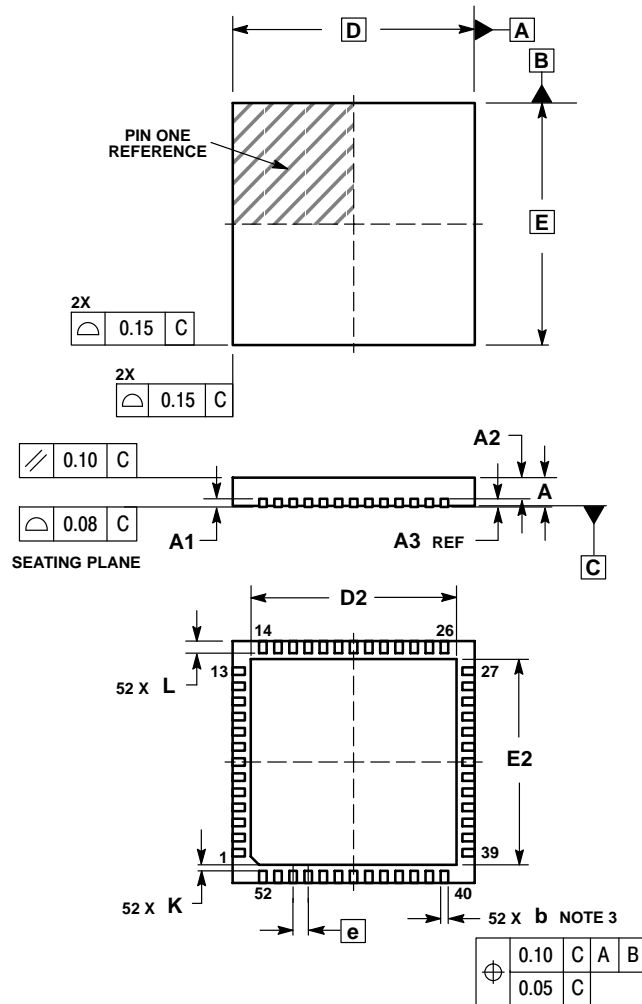
### RECOMMENDED SOLDERING FOOTPRINT



# NB100LVEP221

## PACKAGE DIMENSIONS

QFN52 8x8, 0.5P  
CASE 485M  
ISSUE C

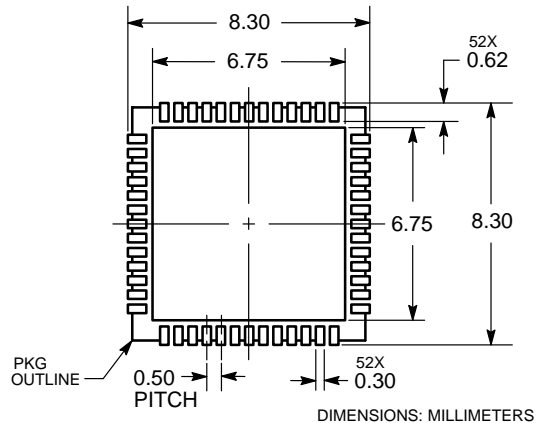


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20	REF
b	0.18	0.30
D	8.00	BSC
D2	6.50	6.80
E	8.00	BSC
E2	6.50	6.80
e	0.50	BSC
K	0.20	---
L	0.30	0.50

**RECOMMENDED SOLDERING FOOTPRINT**



ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative