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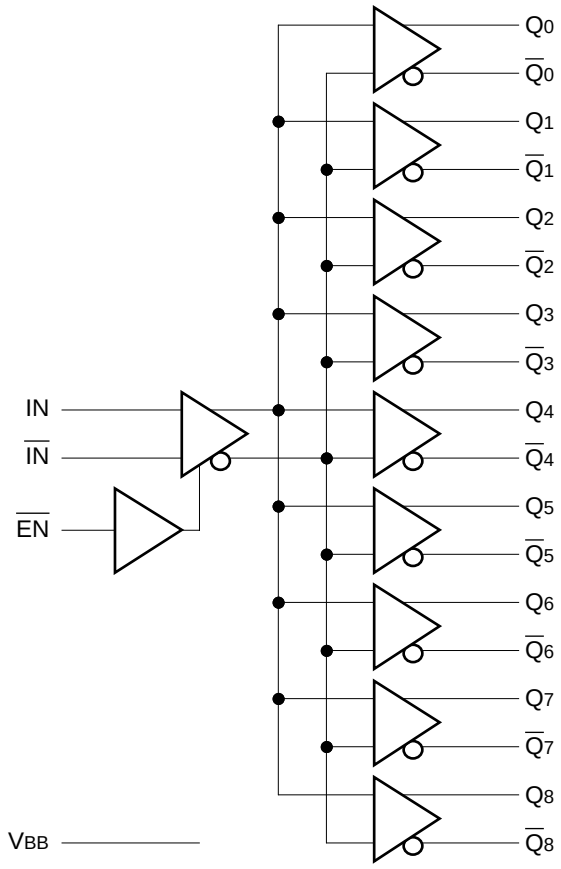
1:9 DIFFERENTIAL CLOCK DRIVER WITH ENABLE

SY10E111
SY100E111

FEATURES

- **Low skew**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Guaranteed skew limits**
- **Differential design**
- **V_{BB} output**
- **Enable input**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **75KΩ input pulldown resistors**
- **Fully compatible with ON Semiconductor MC10E/100E111**
- **Available in 28-pin PLCC package**

BLOCK DIAGRAM



DESCRIPTION

The SY10/100E111 are low skew 1-to-9 differential drivers designed for clock distribution in new, high-performance ECL systems. They accept one differential or single-ended input, with V_{BB} used for single-ended operation. The signal is fanned out to nine identical differential outputs. An enable input is also provided such that a logic HIGH disables the device by forcing all Q outputs LOW and all /Q outputs HIGH.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E111 shares a common set of "basic" processing with the other members of the ECLinPS™ family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

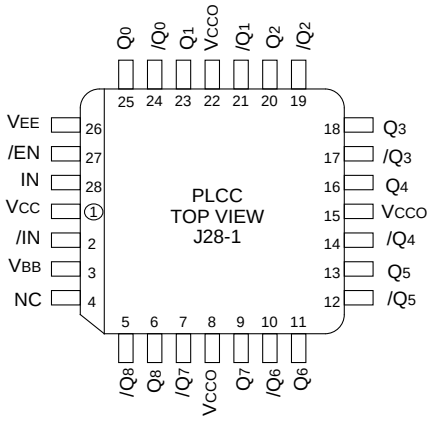
To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO} as the pair(s) being used on that side) in order to maintain minimum skew.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using V_{BB} for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01µF capacitor.

PIN NAMES

Pin	Function
IN, /IN	Differential Input Pair
/EN	Enable Input
Q0, /Q0 — Q8, /Q8	Differential Outputs
V_{BB}	V_{BB} Output
V_{CCO}	V_{CC} to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E111JI	J28-1	Industrial	SY10E111JI	Sn-Pb
SY10E111JITR[2]	J28-1	Industrial	SY10E111JI	Sn-Pb
SY100E111JI	J28-1	Industrial	SY100E111JI	Sn-Pb
SY100E111JITR[2]	J28-1	Industrial	SY100E111JI	Sn-Pb
SY10E111JC	J28-1	Commercial	SY10E111JC	Sn-Pb
SY10E111JCTR[2]	J28-1	Commercial	SY10E111JC	Sn-Pb
SY100E111JC	J28-1	Commercial	SY100E111JC	Sn-Pb
SY100E111JCTR[2]	J28-1	Commercial	SY100E111JC	Sn-Pb
SY10E111JY[3]	J28-1	Industrial	SY10E111JY with Pb-Free bar-line indicator	Matte-Sn
SY10E111JYTR[2, 3]	J28-1	Industrial	SY10E111JY with Pb-Free bar-line indicator	Matte-Sn
SY100E111JY[3]	J28-1	Industrial	SY100E111JY with Pb-Free bar-line indicator	Matte-Sn
SY100E111JYTR[2, 3]	J28-1	Industrial	SY100E111JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TIMING DIAGRAMS

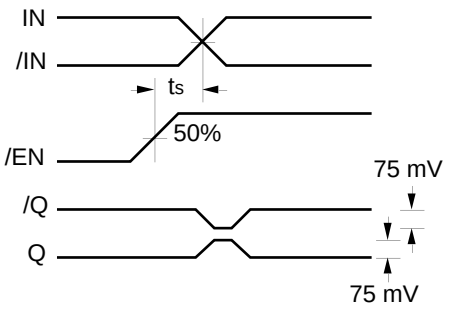


Figure 1. Set-up Time

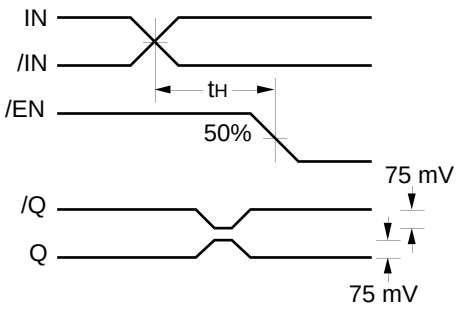


Figure 2. Hold Time

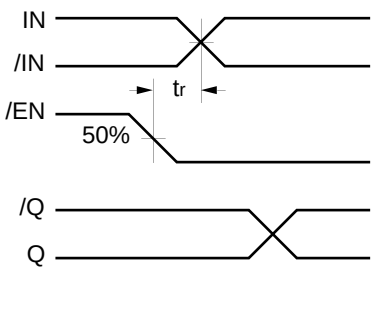


Figure 3. Release Time

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{BB}	Output Reference Voltage 10E				–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V
	100E				–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
I_{IH}	Input HIGH Current				—	—	150	—	—	150	—	—	150	µA
I_{EE}	Power Supply Current 10E				—	48	60	—	48	60	—	48	60	mA
	100E				—	48	60	—	48	60	—	55	69	

AC ELECTRICAL CHARACTERISTICS

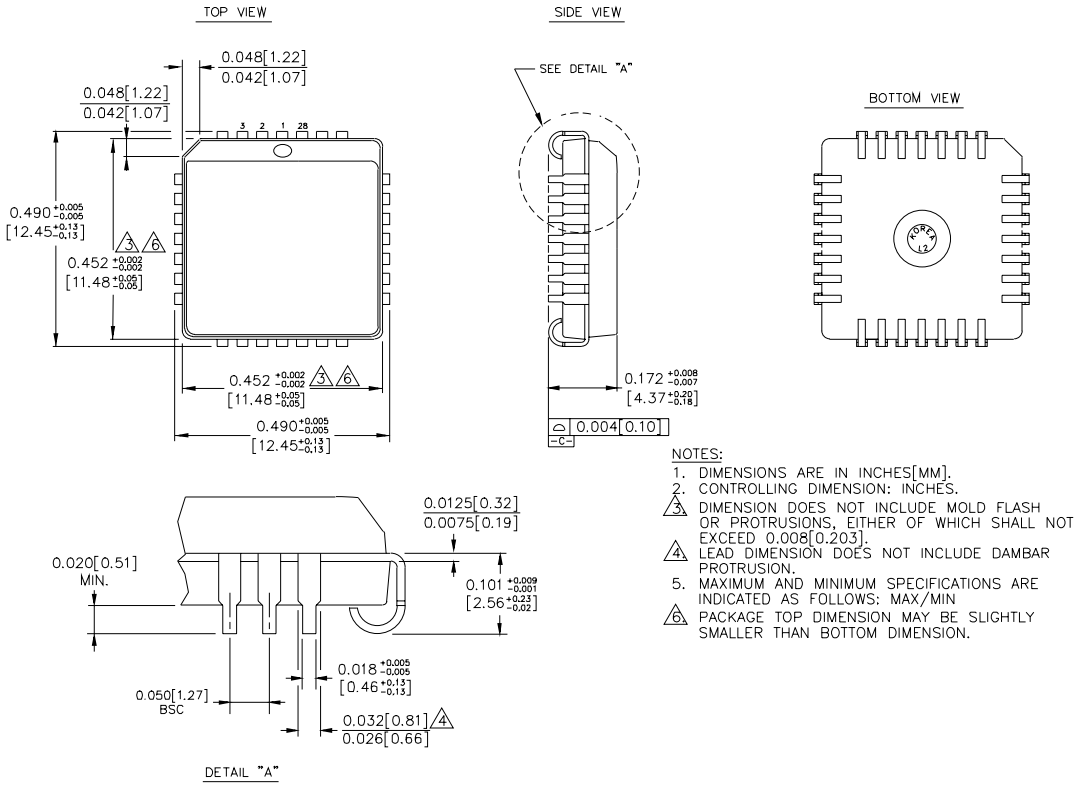
$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	Propagation Delay to Output													ps
	IN (differential)[1]				430	—	630	430	—	630	430	—	630	
	IN (single-ended)[2]				330	—	730	330	—	730	330	—	730	
	Enable[3]				450	—	850	450	—	850	450	—	850	
	Disable[3]				450	—	850	450	—	850	450	—	850	
t_{SKEW}	Within-Device Skew[4]				—	25	50	—	25	50	—	25	50	ps
t_S	Set-up Time /EN to IN[5]				200	0	—	200	0	—	200	0	—	ps
t_H	Hold Time IN to /EN[6]				0	–200	—	0	–200	—	0	–200	—	ps
t_R	Release Time /EN to IN[7]				300	100	—	300	100	—	300	100	—	ps
V_{PP}	Minimum Input Swing[8]				250	—	—	250	—	—	250	—	—	mV
V_{CMR}	Common Mode Range[9]				–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V
t_r t_f	Rise/Fall Times (20% to 80%)				275	375	600	275	375	600	275	375	600	ps

Notes:

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on /EN to the 50% point of a **positive** transition on Q (or a negative transition on /Q). Disable is defined as the propagation delay from the 50% point of a **positive** transition on /EN to the 50% point of a **negative** transition on Q (or a positive transition on /Q).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The set-up time is the minimum time that /EN must be asserted prior to the next transition of /IN/IN to prevent an output response greater than ±75mV to that /IN/IN transition (see Figure 1).
6. The hold time is the minimum time that /EN must remain asserted after a negative going IN or a positive going /IN to prevent an output response greater than ±75mV to that IN, /IN transition (see Figure 2).
7. The release time is the minimum time that /EN must be de-asserted prior to the next IN, /IN transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the E111, as a differential input as low as 50mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

28-PIN PLCC (J28-1)



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