

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

MC10E111, MC100E111

5 V ECL 1:9 Differential Clock Driver

Description

The MC10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all \bar{Q} outputs HIGH.

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

The lowest TPD delay time results from terminating only one output pair, and the greatest TPD delay time results from terminating all the output pairs. This shift is about 10–20 pS in TPD. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest TPD delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest TPD (delay time) occurs and all outputs display about the same 10–20 pS increase in TPD, so the relative skew between any two output pairs remains about 25 nS.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

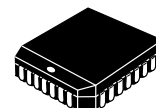
Features

- Guaranteed Skew Spec
- Differential Design
- V_{BB} Output
- PECL Mode Operating Range: $V_{CC} = 4.2$ V to 5.7 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -4.2$ V to -5.7 V
- Internal Input 50 K Ω Pulldown Resistors
- ESD Protection: > 3 kV Human Body Model
- Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)
(For Additional Information, see Application Note [AND8003/D](#))
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 178 Devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



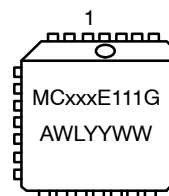
ON Semiconductor®

www.onsemi.com



PLCC-28
FN SUFFIX
CASE 776-02

MARKING DIAGRAM*



xxx = 10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC10E111FNG	PLCC-28 (Pb-Free)	37 Units/Tube
MC10E111FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel
MC100E111FNG	PLCC-28 (Pb-Free)	37 Units/Tube
MC100E111FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MC10E111, MC100E111

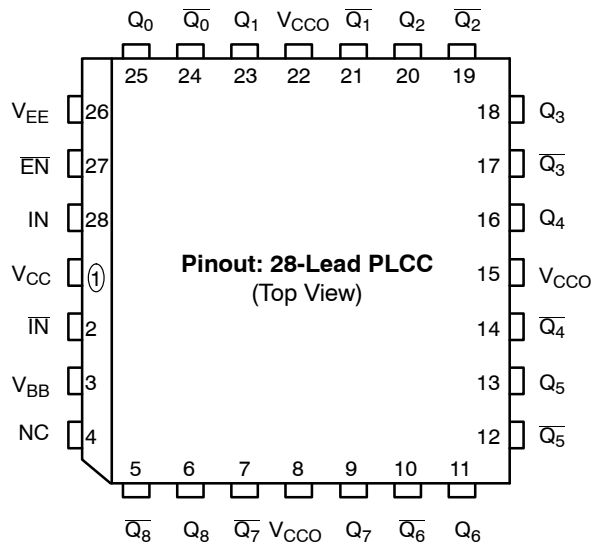


Table 1. PIN DESCRIPTION

PIN	FUNCTION
IN, \overline{IN}	ECL Differential Input Pair
EN	ECL Enable
$Q_0, \overline{Q_0}-Q_8, \overline{Q_8}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC} , V_{CCO} , and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 28-Lead Pinout

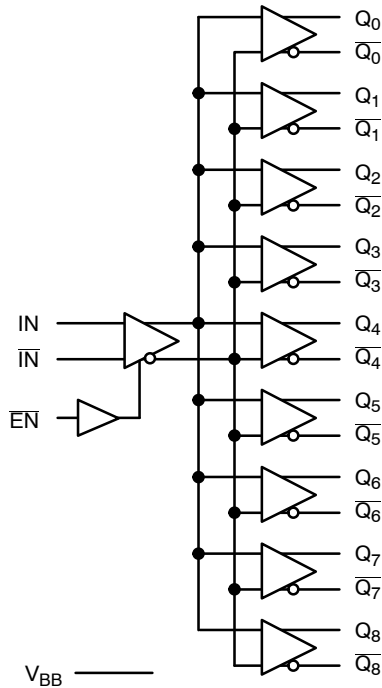


Figure 2. Logic Symbol

MC10E111, MC100E111

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V
I _{out}	Output Current	Continuous Surge		50 100	mA
I _{BB}	V _{BB} Sink/Source			±0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
T _{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. 10E SERIES PECL DC CHARACTERISTICS (V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		41	60		42	60		43	60	mA
V _{OH}	Output HIGH Voltage (Note 2)	3920	4030	4110	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 2)	3050	3230	3350	3050	3210	3370	3050	3227	3405	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	3870	4030	4190	3870	4030	4190	3940	4110	4280	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V _{BB}	Output Voltage Reference	3.6		3.73	3.65		3.75	3.69		3.90	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	3.4		4.6	3.4		4.6	3.4		4.6	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5	0.25		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary -0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.
3. V_{IHCMR} min and max vary 1:1 with V_{CC}.

MC10E111, MC100E111

Table 4. 10E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		41	60		42	60		43	60	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1080	-970	-890	-980	-895	-810	-910	-815	-720	mV
V_{OL}	Output LOW Voltage (Note 2)	-1950	-1770	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1130	-970	-810	-1130	-970	-810	-1060	-890	-720	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
V_{BB}	Output Voltage Reference	-1.40		-1.27	-1.35		-1.25	-1.31		-1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	-1.6		-0.4	-1.6		-0.4		1.6	-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5	0.065		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min and max vary 1:1 with V_{CC} .

Table 5. 100E SERIES PECL DC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		40	60		45	60		50	69	mA
V_{OH}	Output HIGH Voltage (Note 2)	3975	4020	4120	3975	4020	4120	3975	4020	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3190	3300	3380	3190	3300	3380	3190	3300	3380	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
V_{BB}	Output Voltage Reference	3.64		3.75	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	3.4		4.6	3.4		4.6	3.4		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min and max vary 1:1 with V_{CC} .

MC10E111, MC100E111

Table 6. 100E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		40	60		45	60		50	69	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1025	-980	-880	-1025	-980	-880	-1025	-980	-880	mV
V_{OL}	Output LOW Voltage (Note 2)	-1810	-1700	-1620	-1810	-1700	-1620	-1810	-1700	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165	-1025	-880	-1165	-1025	-880	-1165	-1025	-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1645	-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.25	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	-1.6		-0.4	-1.6		-0.4	-1.6		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$
3. V_{IHCMR} min and max vary 1:1 with V_{CC} .

Table 7. AC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		800			800			800		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (Diff) (Note 2) IN (SE) (Note 3) Enable (Note 4) Disable (Note 4)	430 380 400 400		630 680 900 900	430 380 450 450		630 680 850 850	430 380 450 450		630 680 850 850	ps
t_s	Setup Time (Note 5) EN to IN	250	0		200	0		200	0		ps
t_H	Hold Time (Note 6) IN to EN	50	-200		0	-200		0	-200		ps
t_R	Release Time (Note 7) EN to IN	350	100		300	100		300	100		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. 10 Series: V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
100 Series: V_{EE} can vary $-0.46 / +0.8\text{ V}$.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. Enable is defined as the propagation delay from the 50% point of a **negative** transition on EN to the 50% point of a **positive** transition on Q (or a negative transition on \bar{Q}). Disable is defined as the propagation delay from the 50% point of a **positive** transition on EN to the 50% point of a **negative** transition on Q (or a positive transition on \bar{Q}).
5. The setup time is the minimum time that EN must be asserted prior to the next transition of IN/ \bar{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/ \bar{IN} transition (Figure 3).
6. The hold time is the minimum time that EN must remain asserted after a negative going IN or a positive going \bar{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/ \bar{IN} transition (Figure 4).
7. The release time is the minimum time that EN must be deasserted prior to the next IN/ \bar{IN} transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (Figure 5).
8. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

MC10E111, MC100E111

Table 7. AC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{skew}	Within-Device Skew (Note 8)		25	75		25	50		25	50	ps
t_{JITTER}	Random Clock Jitter (RMS)		< 1	< 2		< 1	< 2		< 1	< 2	ps
V_{PP}	Minimum Input Swing	50			50			50			mV
t_r, t_f	Rise/Fall Time	250	450	650	275	375	600	275	375	600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 10 Series: V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
100 Series: V_{EE} can vary $-0.46 / +0.8\text{ V}$.
- The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
- The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
- Enable is defined as the propagation delay from the 50% point of a **negative** transition on \overline{EN} to the 50% point of a **positive** transition on Q (or a negative transition on \overline{Q}). Disable is defined as the propagation delay from the 50% point of a **positive** transition on \overline{EN} to the 50% point of a **negative** transition on Q (or a positive transition on \overline{Q}).
- The setup time is the minimum time that \overline{EN} must be asserted prior to the next transition of IN/\overline{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/\overline{IN} transition (Figure 3).
- The hold time is the minimum time that \overline{EN} must remain asserted after a negative going IN or a positive going \overline{IN} to prevent an output response greater than $\pm 75\text{ mV}$ to that IN/\overline{IN} transition (Figure 4).
- The release time is the minimum time that \overline{EN} must be deasserted prior to the next IN/\overline{IN} transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (Figure 5).
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

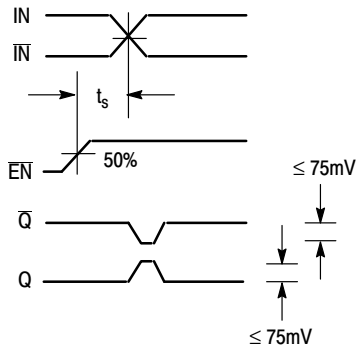


Figure 3. Setup Time

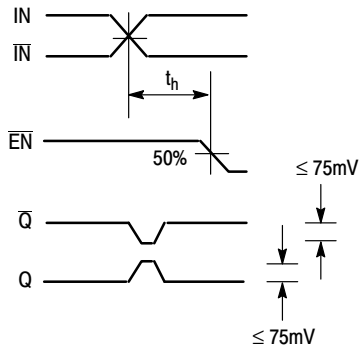


Figure 4. Hold Time

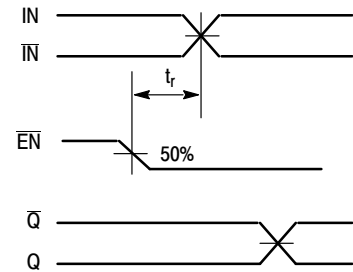


Figure 5. Release Time

MC10E111, MC100E111

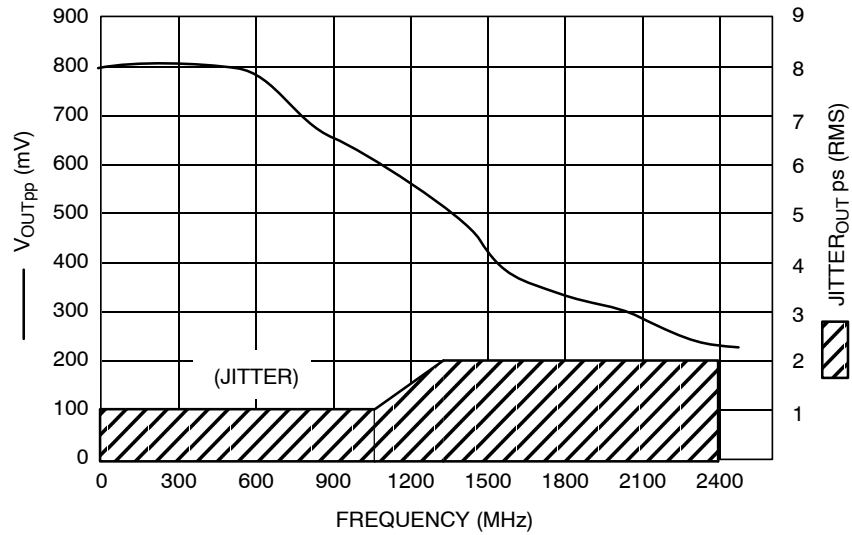


Figure 6. F_{max}/Jitter

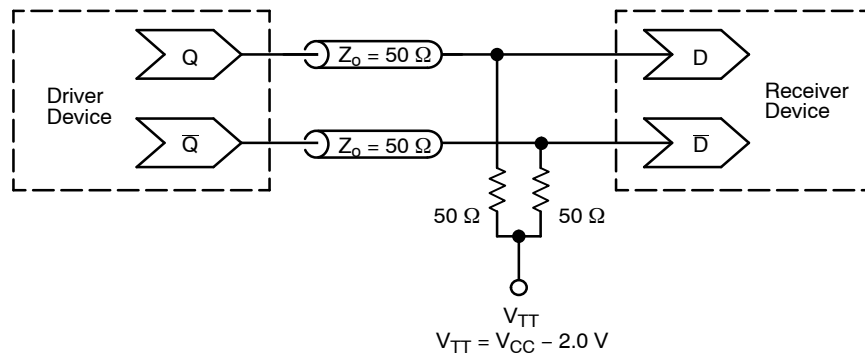


Figure 7. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

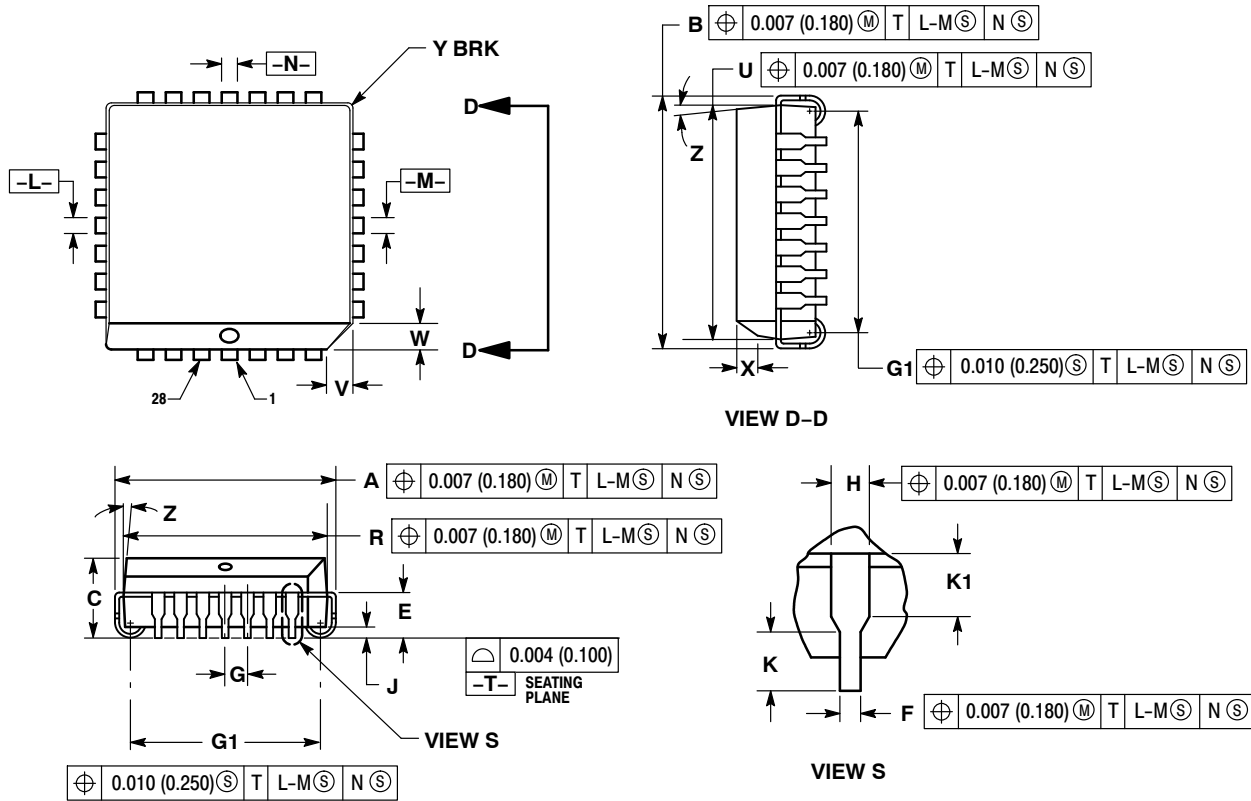
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC10E111, MC100E111

PACKAGE DIMENSIONS

28 LEAD PLLC
FN SUFFIX
CASE 776-02
ISSUE F




NOTES:

- DATUMS $-L-$, $-M-$, AND $-N-$ DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION $G1$, TRUE POSITION TO BE MEASURED AT DATUM $-T-$, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

MC10E111, MC100E111

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative