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NB100LVEP222

2.5 V/3.3 V 2:1:15 Differential ECL/PECL ÷1/÷2 Clock Driver

The NB100LVEP222 is a low skew 2:1:15 differential ÷1/÷2 ECL fanout buffer designed with clock distribution in mind. The LVECL/LVPECL input signal pairs can be used in a differential configuration or single−ended (with V_{BB} output reference bypassed and connected to the unused input of a pair). Either of two fully differential clock inputs may be selected. Each of the four output banks of 2, 3, 4, and 6 differential pairs may be independently configured to fanout 1X or 1/2X of the input frequency. When the output banks are configured with the ÷1 mode, data can also be distributed. The LVEP222 specifically guarantees low output to output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot. This device is an improved version of the MC100LVE222 with higher speed capability and reduced skew.

The fsel pins and CLK_Sel pin are asynchronous control inputs. Any changes may cause indeterminate output states requiring an MR pulse to resynchronize any 1/2X outputs (See Figure 4). Unused output pairs should be left unterminated (open) to reduce power and switching noise.

The NB100LVEP222, as with most ECL devices, can be operated from a positive V_{CC}/V_{CC0} supply in LVPECL mode. This allows the LVEP222 to be used for high performance clock distribution in +2.5/3.3 V systems. In a PECL environment series or Thevenin line, terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to Application Note AN1406/D. For a SPICE model, refer to Application Note AN1560/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single−ended LVPECL input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC}/V_{CC0} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open. Single−ended CLK input operation is limited to a $V_{CC}/V_{CC0} \geq 3.0$ V in LVPECL mode, or $V_{EE} \leq -3.0$ V in NECL mode.

Features

- 20 ps Output−to−Output Skew
- 85 ps Part−to−Part Skew
- Selectable 1x or 1/2x Frequency Outputs
- LVPECL Mode Operating Range: V_{CC}/V_{CC0} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC}/V_{CC0} = 0 V with V_{EE} = −2.375 V to −3.8 V
- Internal Input Pulldown Resistors
- Performance Upgrade to ON Semiconductor’s MC100LVE222
- V_{BB} Output
- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

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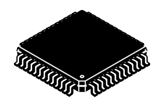
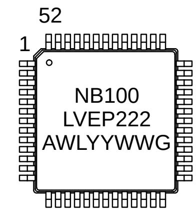
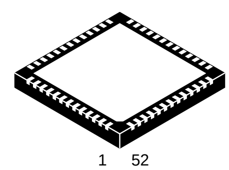
MARKING DIAGRAMS*

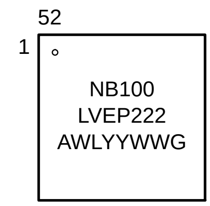


LQFP−52
FA SUFFIX
CASE 848H





QFN−52
MN SUFFIX
CASE 485M

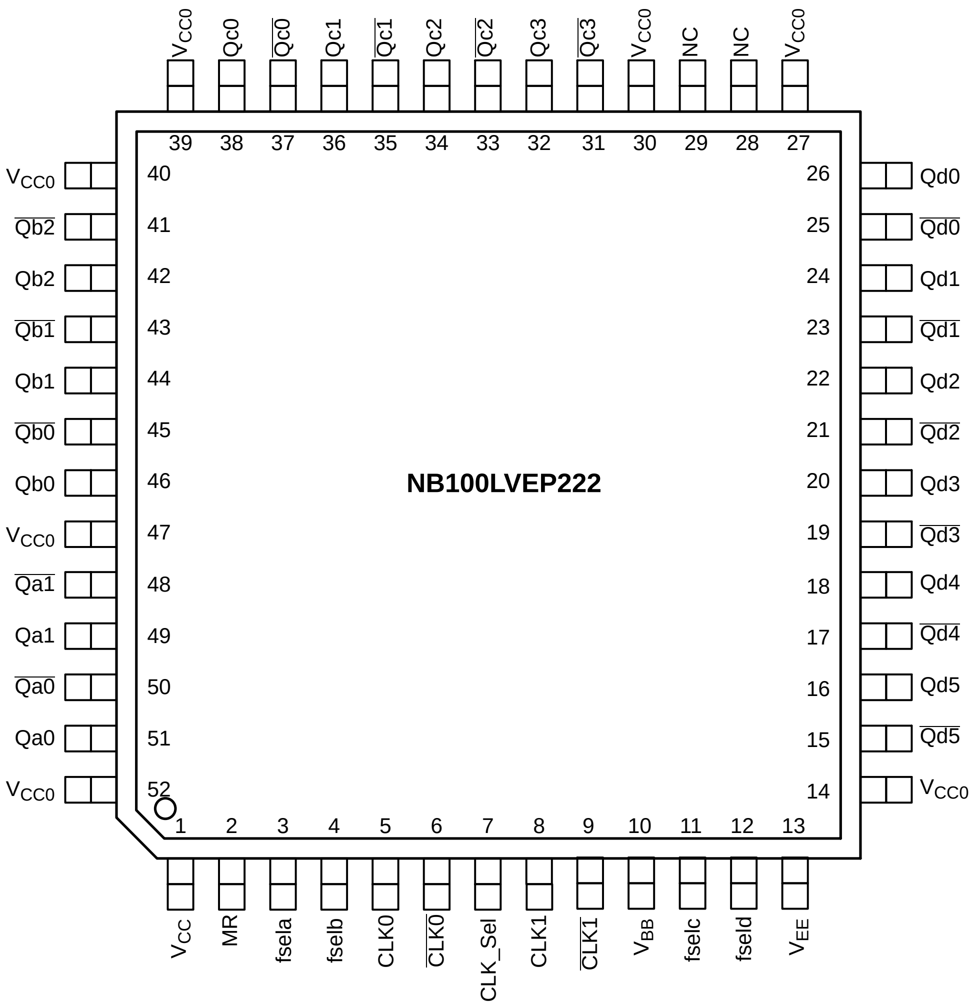


A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.



All V_{CC}, V_{CC0}, and V_{EE} pins must be externally connected to appropriate Power Supply to guarantee proper operation.V_{CC} pin internally connected to V_{CC0} pins. The thermally conductive exposed pad on package bottom (see package case drawing) must be attached to a heat−sinking conduit. This exposed pad is electrically connected to V_{EE} internally.

Figure 1. 52−Lead LQFP Pinout (Top View)

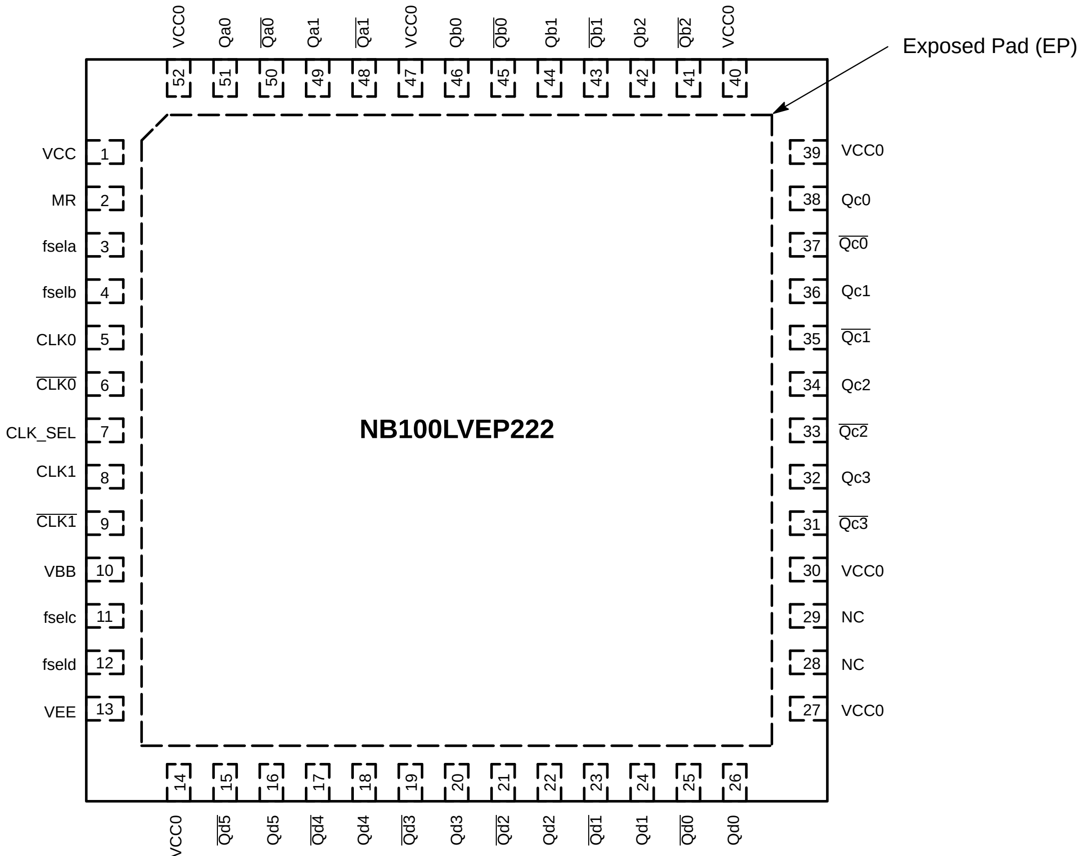


Figure 2. QFN−52 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK0*, $\overline{CLK0}$**	ECL Differential Input Clock
CLK1*, $\overline{CLK1}$**	ECL Differential Input Clock
CLK_Sel*	ECL Clock Select
MR*	ECL Master Reset
Qa0:1, $\overline{Qa0:1}$	ECL Differential Outputs
Qb0:2, $\overline{Qb0:2}$	ECL Differential Outputs
Qc0:3, $\overline{Qc0:3}$	ECL Differential Outputs
Qd0:5, $\overline{Qd0:5}$	ECL Differential Outputs
fseln*	ECL ÷1 or ÷2 Select
V_{BB}	Reference Voltage Output
V_{CC}, V_{CC0}	Positive Supply, $V_{CC} = V_{CC0}$
V_{EE}***	Negative Supply
NC	No Connect

* Pins will default LOW when left open.
** Pins will default HIGH when left open.
*** The thermally conductive exposed pad on the bottom of the package is electrically connected to V_{EE} internally.

Table 2. FUNCTION TABLE

Input	Function	
	L	H
MR	Active	Reset
CLK_Sel	CLK0	CLK1
fseln	÷1	÷2

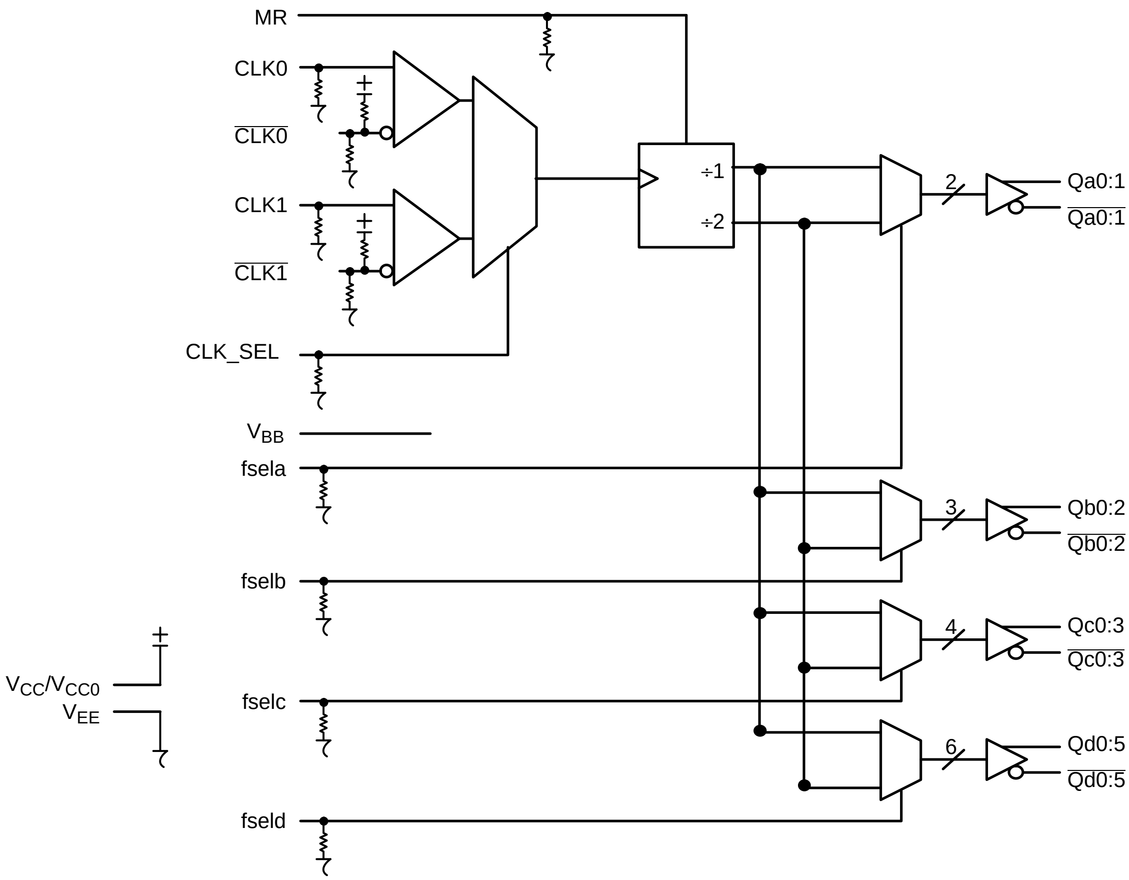


Figure 3. Logic Diagram

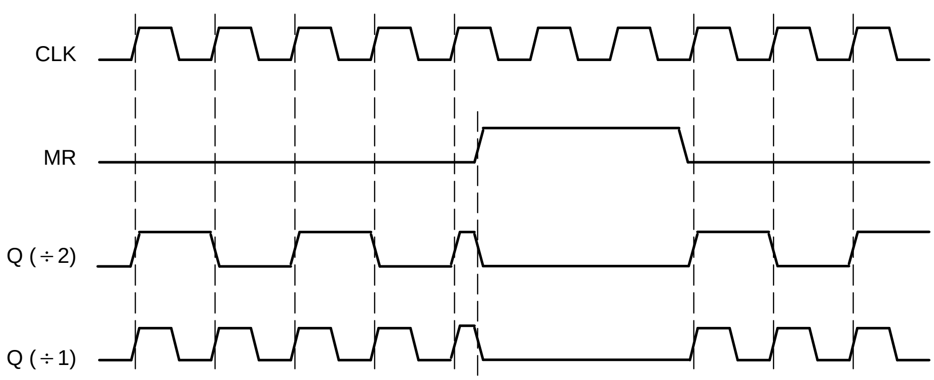


Figure 4. Master Reset (MR) Timing Diagram

Table 3. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	LQFP−52 QFN−52	Level 2 −	Level 3 Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in	
Transistor Count		821 Devices	
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}/V_{CC0}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC}/V_{CC0} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC}/V_{CC0} = 0 V	$V_I \le V_{CC}/V_{CC0}$ $V_I \ge V_{EE}$	6 to 0 −6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (See Application Information)	0 lfpm 500 lfpm	LQFP−52 LQFP−52	35.6 30	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (See Application Information)	0 lfpm 500 lfpm	LQFP−52 LQFP−52	3.2 6.4	°C/W °C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note)	0 lfpm 500 lfpm	QFN−52 QFN−52	25 19.6	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note)	2S2P	QFN−52	21	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. LVPECL DC CHARACTERISTICS $V_{CC} = V_{CC0} = 2.5$ V; $V_{EE} = 0$ V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	150	104	130	156	112	140	168	mA
V_{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 3)	555	680	900	555	680	900	555	680	900	mV
V_{IH}	Input HIGH Voltage (Single−Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Note 4)	555		900	555		900	555		900	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) (Figure 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
2. Input and output parameters vary 1:1 with V_{CC}/V_{CC0}. V_{EE} can vary + 0.125 V to −1.3 V.
3. All loading with 50 Ω to V_{CC}/V_{CC0} − 2.0 V.
4. Do not use V_{BB} Pin #10 at V_{CC}/V_{CC0} < 3.0 V (see AND8066).
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}/V_{CC0}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. LVPECL DC CHARACTERISTICS $V_{CC} = V_{CC0} = 3.3$ V; $V_{EE} = 0.0$ V (Note 6)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	150	104	130	156	112	140	168	mA
V_{OH}	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 7)	1355	1480	1700	1355	1480	1700	1355	1480	1700	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1355		1700	1355		1700	1355		1700	mV
V_{BB}	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) (Figure 6)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
6. Input and output parameters vary 1:1 with V_{CC}/V_{CC0}. V_{EE} can vary + 0.925 V to −0.5 V.
7. All loading with 50 Ω to V_{CC}/V_{CC0}−2.0 V.
8. Single−Ended input operation is limited V_{CC}/V_{CC0} ≥ 3.0 V in LVPECL mode.
9. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}/V_{CC0}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. LVNECL DC CHARACTERISTICS $V_{CC} = V_{CC0} = 0.0$ V; $V_{EE} = -3.8$ V to −2.375 V (Note 10)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	150	104	130	156	112	140	168	mA
V_{OH}	Output HIGH Voltage (Note 11)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 11)	−1945	−1820	−1600	−1945	−1820	−1600	−1945	−1820	−1600	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1945		−1600	−1945		−1600	−1945		−1600	mV
V_{BB}	Output Reference Voltage (Note 12)	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) (Figure 6)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 −150			0.5 −150			0.5 −150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Input and output parameters vary 1:1 with V_{CC}/V_{CC0}.
11. All loading with 50 Ω to $V_{CC}/V_{CC0} - 2.0$ V.
12. Single−Ended input operation is limited $V_{EE} \leq -3.0$ V in NECL mode.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}/V_{CC0}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. AC CHARACTERISTICS $V_{CC} = V_{CC0}$ = 2.375 to 3.8 V; V_{EE} = 0.0 V or $V_{CC} = V_{CC0}$ = 0.0 V; V_{EE} = −2.375 to −3.8 V (Note 14)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{Opp}	Differential Output Voltage (Figure 5) f_{out} = 50 MHz f_{out} = 0.8 GHz f_{out} = 1.0 GHz	 500 550 500	 600 650 650		 500 525 425	 600 650 650		 500 500 400	 600 650 600		mV
t_{PLH} t_{PHL}	Propagation Delay (Differential Configuration) CLKx−Q_X MR−Q_{XX}	 650 700	 800 900	 900 1200	 700 700	 875 900	 1000 1200	 850 700	 975 900	 1150 1200	ps
t_{skew}	Within−Device Skew (Note 15) (÷1 Mode) − Qa[0:1] − Qb[0:2] − Qc[0:3] − Qd[0:5] − Qa_N, Qb_N, Qd_N − All Outputs		 10 10 20 10 10 20	 40 40 60 40 40 60		 10 10 20 10 10 20	 40 40 60 40 40 60		 10 10 20 10 10 20	 40 40 60 40 40 60	ps
t_{skew}	Within−Device Skew (Note 15) (÷2 Mode) − Qa[0:1] − Qb[0:2] − Qc[0:3] − Qd[0:5] − Qa_N, Qb_N, Qd_N − All Outputs		 15 15 20 15 15 20	 70 70 70 70 70 70		 10 10 20 10 10 20	 40 40 50 40 40 50		 15 10 15 15 15 15	 70 40 70 70 70 70	ps
t_{skew}	Device−to−Device Skew (Differential Configuration) (Note 16)		85	300		85	300		85	300	ps
t_{JITTER}	Random Clock Jitter (Figure 5) (RMS)		1	5		1	4		1	5	ps
V_{PP}	Input Swing (Differential Configuration) (Note 17) (Figure 6)	150	800	1200	150	800	1200	150	800	1200	mV
DCO	Output Duty Cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5	%
t_r/t_f	Output Rise/Fall Time 20%−80%	100	200	300	100	200	300	150	250	350	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

14. Measured with LVPECL 750 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to V_{CC}/V_{CC0} − 2.0 V.
15. Skew is measured between outputs under identical transitions and operating conditions.
16. Device−to−Device skew for identical transitions at identical V_{CC}/V_{CC0} levels.
17. V_{PP} is the differential configuration input voltage swing required to maintain AC characteristics including t_{PD} and device−to−device skew.

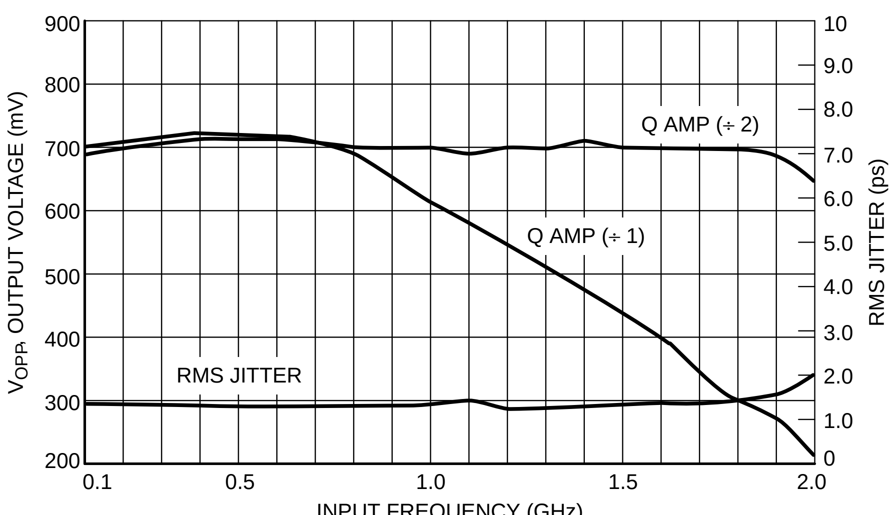


Figure 5. Output Voltage (V_{OPP}) versus Input Frequency and Random Clock Jitter (t_{JITTER}) @ 25°C

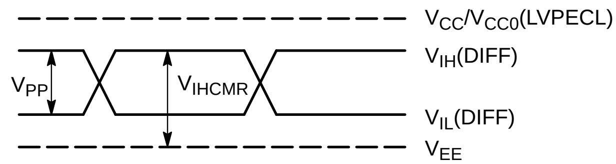


Figure 6. LVPECL Differential Input Levels

APPLICATIONS INFORMATION

Using the thermally enhanced package of the NB100LVEP222

The NB100LVEP222 uses a thermally enhanced 52−lead LQFP package. The package is molded so that a portion of the leadframe is exposed at the surface of the package bottom side. This exposed metal pad will provide the low thermal impedance that supports the power consumption of the NB100LVEP222 high−speed bipolar integrated circuit and will ease the power management task for the system design. In multilayer board designs, a thermal land pattern on the printed circuit board and thermal vias are recommended to maximize both the removal of heat from the package and electrical performance of the NB100LVEP222. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area should be at least the same size and shape as the exposed pad on the package. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal conduit. The thermal vias will connect the exposed pad of the package to internal copper planes of the board. The number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern.

The recommended thermal land design for NB100LVEP222 applications on multi−layer boards comprises a 4 X 4 thermal via array using a 1.2 mm pitch as shown in Figure 7 providing an efficient heat removal path.

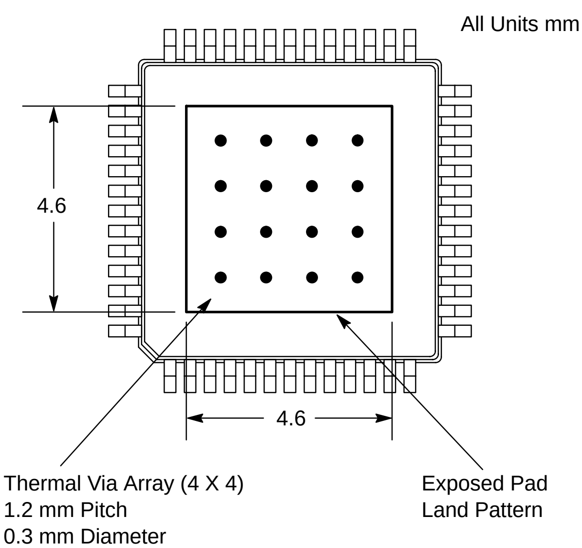


Figure 7. Recommended Thermal Land Pattern

The via diameter should be approximately 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via may result in voiding during the solder process and must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for the exposed pad package is equivalent to standard surface mount packages. Figure 8, “Recommended solder mask openings”, shows a recommended solder mask opening with respect to a 4 X 4 thermal via array. Because a large solder mask opening may result in a poor rework release, the opening should be subdivided as shown in Figure 8. For the nominal package standoff of 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

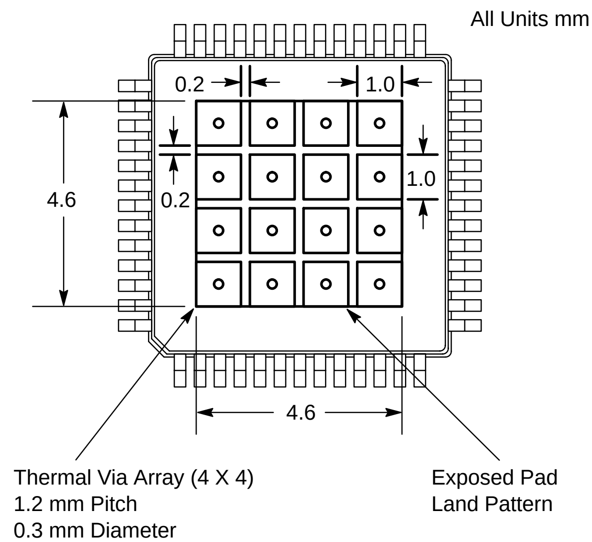


Figure 8. Recommended Solder Mask Openings

Proper thermal management is critical for reliable system operation. This is especially true for high−fanout and high output drive capability products.

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 9. Thermal Resistance *

lfpm	θJA °C/W	θJC °C/W
0	35.6	3.2
100	32.8	4.9
500	30.0	6.4

* Junction to ambient and Junction to board, four−conductor layer test board (2S2P) per JESD 51−8

These recommendations are to be used as a guideline, only. It is therefore recommended that users employ sufficient thermal modeling analysis to assist in applying the general recommendations to their particular application to assure adequate thermal performance. The exposed pad of the NB100LVEP222 package is electrically shorted to the substrate of the integrated circuit and V_{EE}. The thermal land should be electrically connected to V_{EE}.

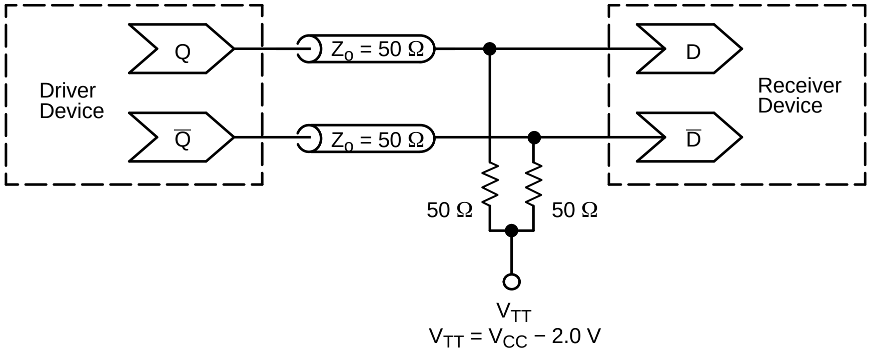


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1642/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

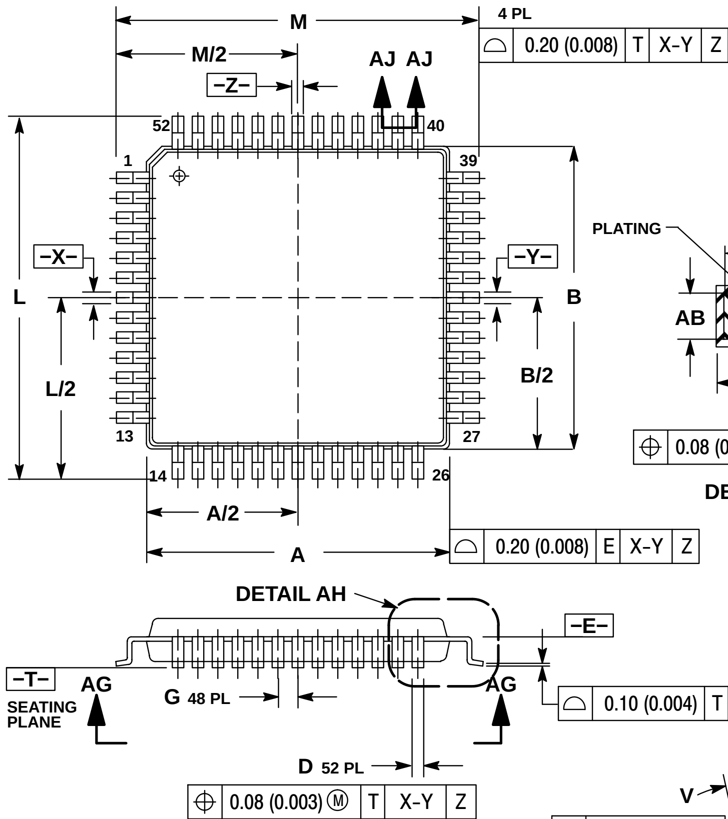
ORDERING INFORMATION

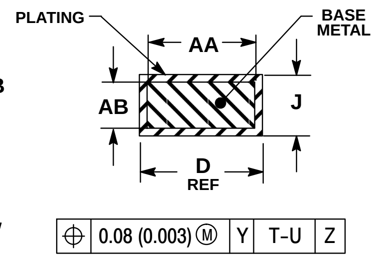
Device	Package	Shipping†
NB100LVEP222FAG	LQFP−52 (Pb−Free)	160 Units / Tray
NB100LVEP222FARG	LQFP−52 (Pb−Free)	1500 / Tape & Reel
NB100LVEP222MNG	QFN−52 (Pb−Free)	260 Units / Tray
NB100LVEP222MNR2G	QFN−52 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

LQFP 52 LEAD EXPOSED PAD
CASE 848H
ISSUE B

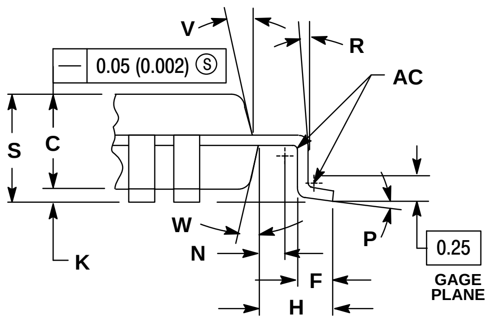




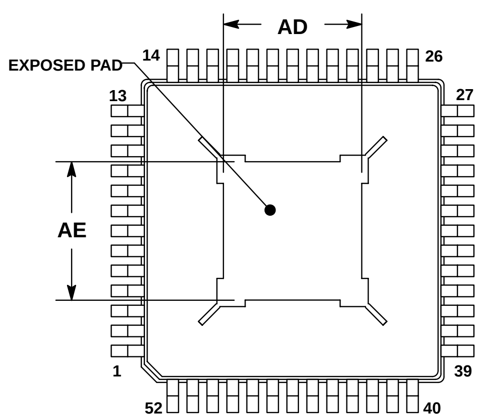
DETAIL AJ–AJ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM PLANE "E" IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
4. DATUM "X", "Y" AND "Z" TO BE DETERMINED AT DATUM PLANE DATUM "E".
5. DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM "T".
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLAND "E".
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
B	10.00 BSC		0.394 BSC	
C	1.30	1.50	0.051	0.059
D	0.22	0.40	0.009	0.016
F	0.45	0.75	0.018	0.030
G	0.65 BSC		0.026 BSC	
H	1.00 REF		0.039 BSC	
J	0.09	0.20	0.004	0.008
K	0.05	0.20	0.002	0.008
L	12.00 BSC		0.472 BSC	
M	12.00 BSC		0.472 BSC	
N	0.20 REF		0.008 REF	
P	0 °	7 °	0 °	7 °
R	0 °	---	0 °	---
S	---	1.70	---	0.067
V	12 ° REF		12 ° REF	
W	12 ° REF		12 ° REF	
AA	0.20	0.35	0.008	0.014
AB	0.07	0.16	0.003	0.006
AC	0.08	0.20	0.003	0.008
AD	4.58	4.78	0.180	0.188
AE	4.58	4.78	0.180	0.188

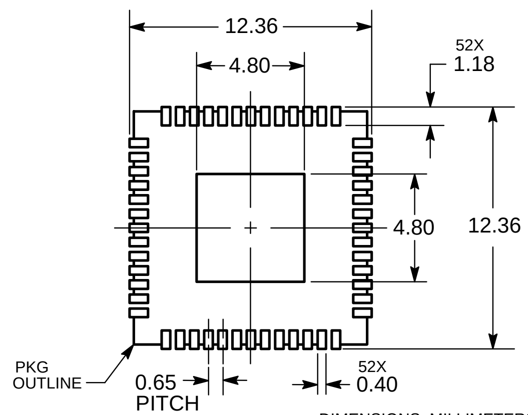


DETAIL AH



VIEW AG–AG

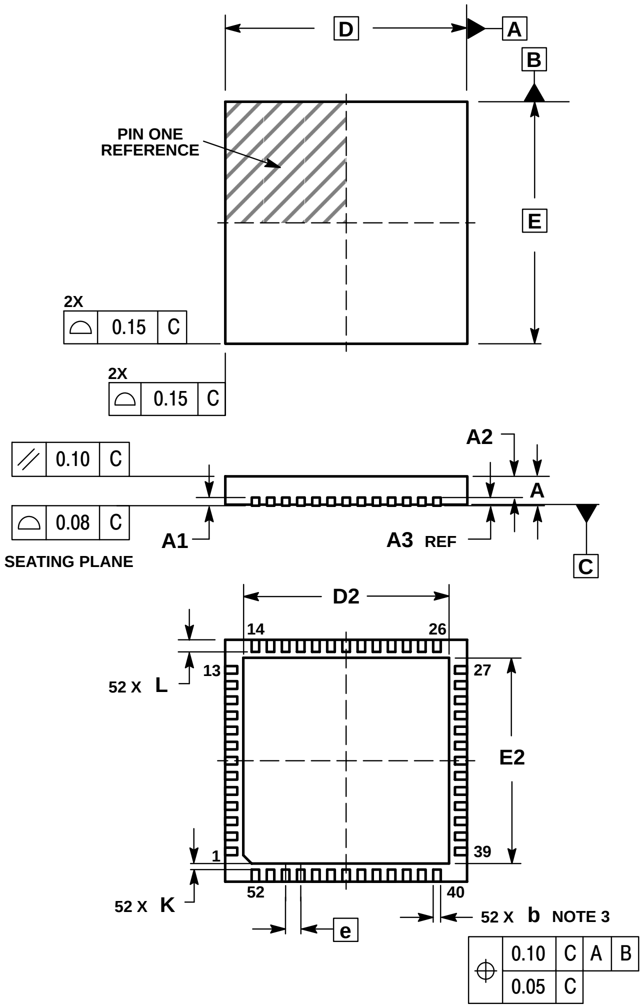
RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

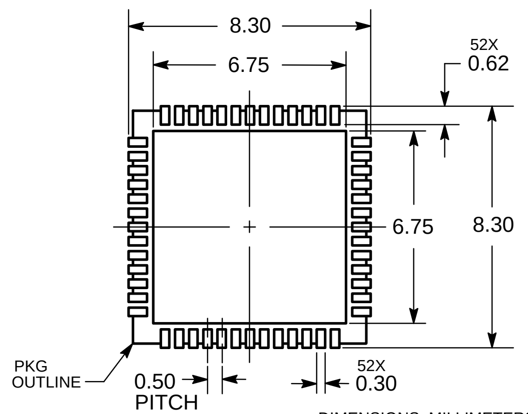
52 PIN QFN 8x8, 0.5P
CASE 485M
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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