

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NB7L14M

2.5V/3.3V Differential 1:4 Clock/Data Fanout Buffer/Translator with CML Outputs and Internal Termination

Description

The NB7L14M is a differential 1-to-4 clock/data distribution chip with internal source terminated CML output structures, optimized for minimal skew and jitter. Device produces four identical output copies of clock or data operating up to 8 GHz or 12 Gb/s, respectively. As such, NB7L14M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications.

Inputs incorporate internal 50 Ω termination resistors and accept LVPECL, CML, LVCMOS, LVTTL, or LVDS (See Table 6). Differential 16 mA CML outputs provide matching internal 50 Ω terminations, and 400 mV output swings when externally terminated with 50 Ω to V_{CC} (See Figure 14).

The device is offered in a low profile 3x3 mm 16-pin QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency up to 8 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- < 0.5 ps of RMS Clock Jitter
- < 10 ps of Data Dependent Jitter
- 30 ps Typical Rise and Fall Times
- 110 ps Typical Propagation Delay
- 6 ps Typical Within Device Skew
- Operating Range: $V_{CC} = 2.375 \text{ V}$ to 3.465 V with $V_{EE} = 0 \text{ V}$
- CML Output Level (400 mV Peak-to-Peak Output) Differential Output Only
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V/3.3 V LVEL, LVEP, EP and SG Devices
- These are Pb-Free Devices

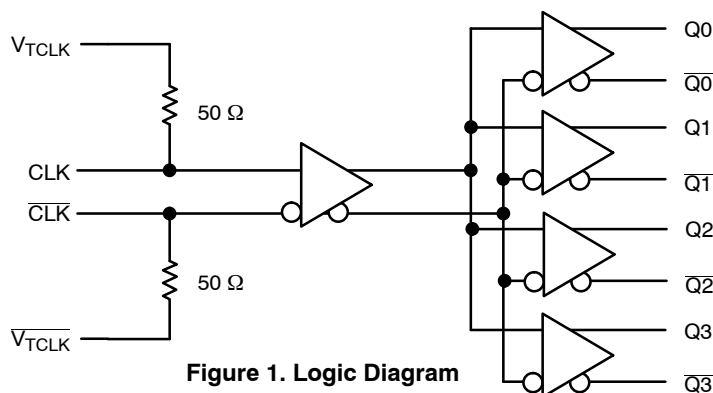


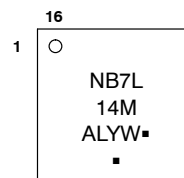
Figure 1. Logic Diagram



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NB7L14M

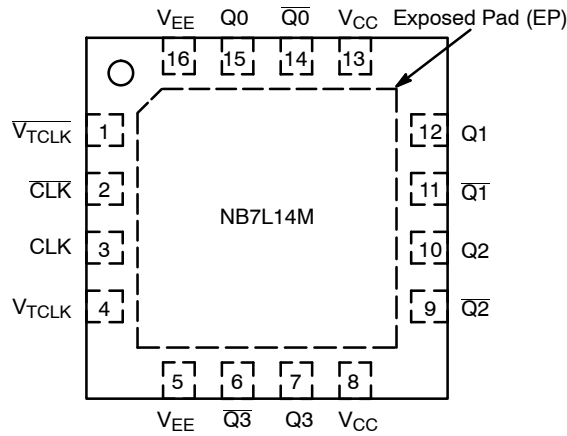


Figure 2. QFN-16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{V_{TCLK}}$	-	Internal 50 Ω Termination Pin for \overline{CLK} .
2	\overline{CLK}	LVPECL, CML, LVC MOS, LV TTL, LVDS	Inverted Differential Clock/Data Input. (Note 1)
3	CLK	LVPECL, CML, LVC MOS, LV TTL, LVDS	Non-inverted Differential Clock/Data Input. (Note 1)
4	V_{TCLK}	-	Internal 50 Ω Termination Pin for CLK.
5,16	V_{EE}	Power Supply	Negative Supply Voltage. All V_{EE} pins must be externally connected to a Power Supply to guarantee proper operation.
6	$\overline{Q3}$	CML Output	Inverted Differential Output 3 with Internal 50 Ω Source Termination Resistor. (Note 2)
7	Q3	CML Output	Non-inverted Differential Output 3 with Internal 50 Ω Source Termination Resistor. (Note 2)
8,13	V_{CC}	Power Supply	Positive Supply Voltage. All V_{CC} pins must be externally connected to a Power Supply to guarantee proper operation.
9	$\overline{Q2}$	CML Output	Inverted Differential Output 2 with Internal 50 Ω Source Termination Resistor. (Note 2)
10	Q2	CML Output	Non-inverted Differential Output 2 with Internal 50 Ω Source Termination Resistor. (Note 2)
11	$\overline{Q1}$	CML Output	Inverted Differential Output 1 with Internal 50 Ω Source Termination Resistor. (Note 2)
12	Q1	CML Output	Non-inverted Differential Output 1 with Internal 50 Ω Source Termination Resistor. (Note 2)
14	$\overline{Q0}$	CML Output	Inverted Differential Output 0 with Internal 50 Ω Source Termination Resistor. (Note 2)
15	Q0	CML Output	Non-inverted Differential Output 0 with Internal 50 Ω Source Termination Resistor. (Note 2)
-	EP	-	Exposed Pad. Thermal pad on the package bottom must be attached to a heatsinking conduit to improve heat transfer. It is recommended to connect the EP to the lower potential (V_{EE}).

1. In the differential configuration when the input termination pins ($\overline{V_{TCLK}}$, V_{TCLK}) are connected to a common termination voltage or left open, and if no signal is applied on CLK and \overline{CLK} , then the device will be susceptible to self-oscillation.
2. CML outputs require 50 Ω receiver termination resistors to V_{CC} for proper operation.

NB7L14M

Table 2. ATTRIBUTES

Characteristics		Value	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1500 V > 50 V > 500 V	
Moisture Sensitivity (Note 3)		Pb Pkg	Pb-Free Pkg
	QFN-16	Level 1	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count		387	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	$V_{EE} = 0\text{ V}$		3.6	V
V_I	Input Voltage	$V_{EE} = 0\text{ V}$	$V_{EE} \leq V_I \leq V_{CC}$	3.6	V
V_{INPP}	Differential Input Voltage CLK - $\overline{\text{CLK}}$	$V_{CC} - V_{EE} \geq 2.8\text{ V}$ $V_{CC} - V_{EE} < 2.8\text{ V}$		2.8 $ V_{CC} - V_{EE} $	V V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	QFN-16		-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN-16 QFN-16	42 36	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 4)	QFN-16	3 to 4	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder	Pb Pb-Free		265 265	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power).

NB7L14M

Table 4. DC CHARACTERISTICS, CLOCK Inputs, CML Outputs ($V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
(Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Open)		140	190	mA
V_{OH}	Output HIGH Voltage (Note 6)	$V_{CC} - 60$	$V_{CC} - 20$	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 6)	$V_{CC} - 530$	$V_{CC} - 420$	$V_{CC} - 360$	mV

Differential Input Driven Single-Ended (see Figures 10 & 12) (Note 8)

V_{th}	Input Threshold Reference Voltage Range (Note 7)	800		$V_{CC} - 75$	mV
V_{IH}	Single-ended Input HIGH Voltage	1200		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage	V_{EE}		$V_{CC} - 150$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2500	mV

Differential Inputs Driven Differentially (see Figures 11 & 13) (Note 9)

V_{IHCLK}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILCLK}	Differential Input LOW Voltage	V_{EE}		$V_{CC} - 75$	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 10)	800		$V_{CC} - 38$	mV
V_{ID}	Differential Input Voltage ($V_{IHCLK} - V_{ILCLK}$)	75		2500	mV
I_{IH}	Input HIGH Current CLK / \overline{CLK} ($V_{TCLK}/\sqrt{V_{TCLK}}$ Open)	0	25	100	μA
I_{IL}	Input LOW Current CLK / \overline{CLK} ($V_{TCLK}/\sqrt{V_{TCLK}}$ Open)	-10	0	10	μA
R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω
$R_{Temp\ Coef}$	Internal I/O Termination Resistor Temperature Coefficient		6.38		$\text{m}\Omega/^\circ\text{C}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} .
6. CML outputs require $50\ \Omega$ receiver termination resistors to V_{CC} for proper operation.
7. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL})/2$.
8. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
9. V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with V_{EE} . V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

NB7L14M

Table 5. AC CHARACTERISTICS ($V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$; Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figure 4) $f_{in} \leq 6\text{ GHz}$ $f_{in} \leq 8\text{ GHz}$	280 125	400 300		280 125	400 300		280 125	400 300		mV
f_{data}	Maximum Operating Data Rate	10	12		10	12		10	12		Gb/s
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	70	110	150	70	110	150	70	110	150	ps
t_{SKEW}	Duty Cycle Skew (Note 12) Within-Device Skew Device-to-Device Skew (Note 13)		2.0 6.0 20	5.0 15 50		2.0 6.0 20	5.0 15 50		2.0 6.0 20	5.0 15 50	ps
t_{JITTER}	RMS Random Clock Jitter (Note 14) Peak/Peak Data Dependent Jitter (Note 15) $f_{in} = 6\text{ GHz}$ $f_{in} = 8\text{ GHz}$ $f_{in} = 2.488\text{ Gb/s}$ $f_{data} = 5\text{ Gb/s}$ $f_{data} = 10\text{ Gb/s}$		0.2 0.2 2.0 5.0 6.0	0.5 0.5 5.0 8.0 10		0.2 0.2 2.0 5.0 6.0	0.5 0.5 5.0 8.0 10		0.2 0.2 2.0 5.0 6.0	0.5 0.5 5.0 8.0 10	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 16)	75	400	2500	75	400	2500	75	400	2500	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz (20% – 80%) Q, \bar{Q}		30	60		30	60		30	60	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured by forcing V_{INPP} (TYP) from a 50% duty cycle clock source. All loading with an external $R_L = 50\ \Omega$ to V_{CC} . Input edge rates 40 ps (20% – 80%).
12. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @1 GHz.
13. Device to device skew is measured between differential outputs under identical transition @ 1 GHz.
14. Additive RMS jitter with 50% duty cycle clock signal at 10 GHz.
15. Additive peak-to-peak data dependent jitter with input NRZ data at PRBS $2^{23}-1$.
16. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$. Input voltage swing is a single-ended measurement operating in differential mode.

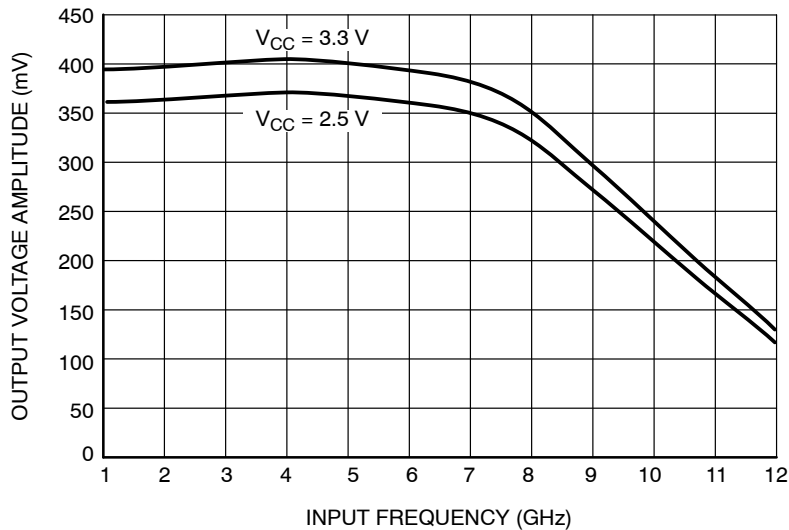


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) at Ambient Temperature (Typical) ($V_{INPP} = 400\text{ mV}$)

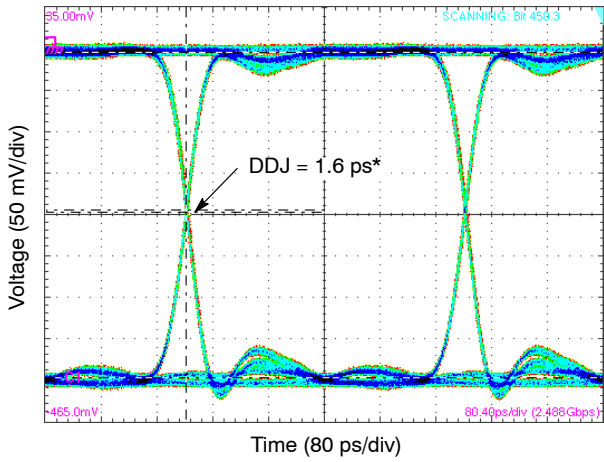


Figure 4. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

*Input signal DDJ = 6.4 ps

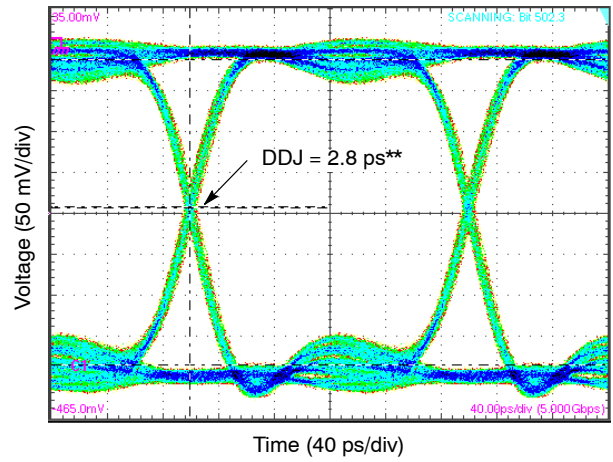


Figure 5. Typical Output Waveform at 5 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

**Input signal DDJ = 7.2 ps

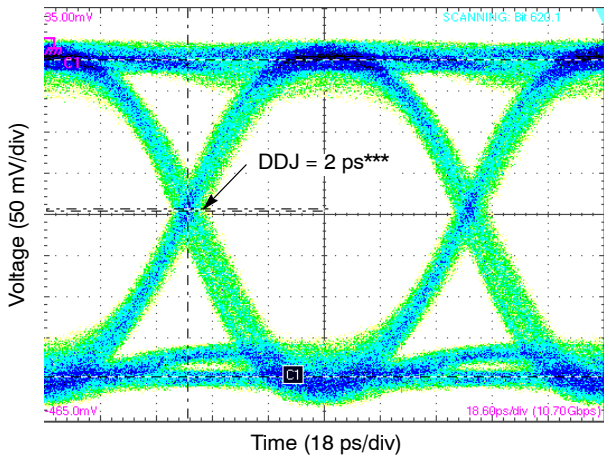


Figure 6. Typical Output Waveform at 10.7 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

***Input signal DDJ = 11 ps

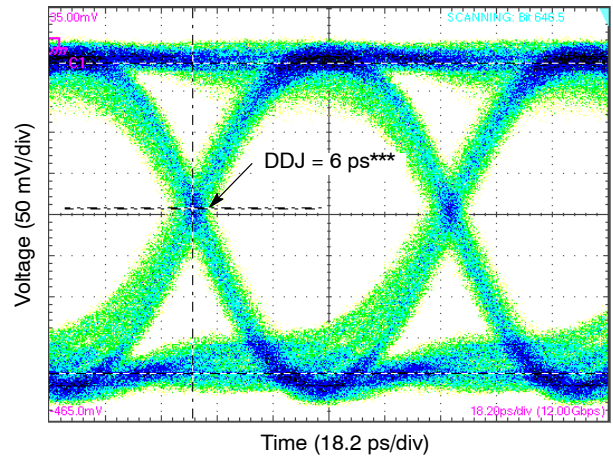


Figure 7. Typical Output Waveform at 12 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

***Input signal DDJ = 13 ps

NB7L14M

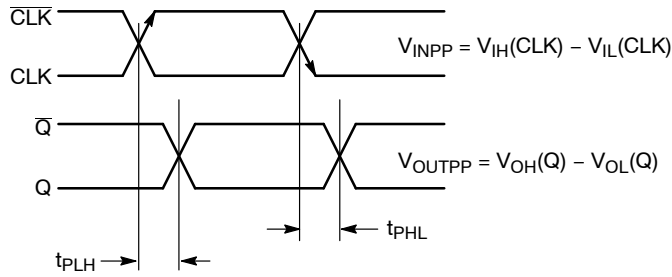


Figure 8. AC Reference Measurement

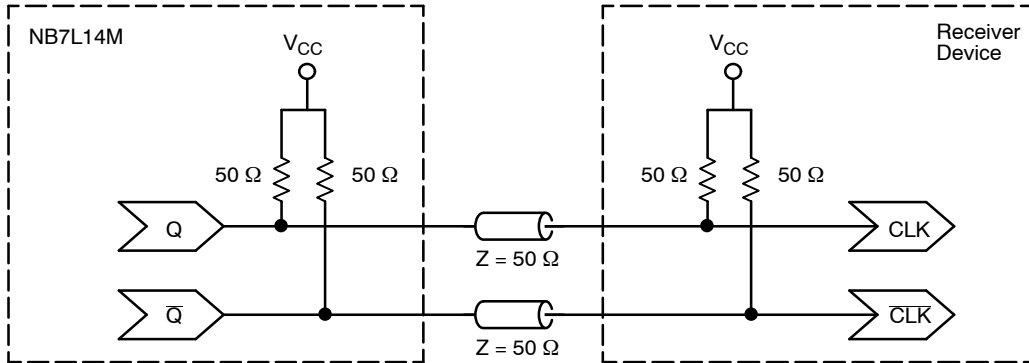


Figure 9. Typical Termination for 16 mA Output Driver and Device Evaluation (Refer to Application Notes AND8020/D and AND8173/D)

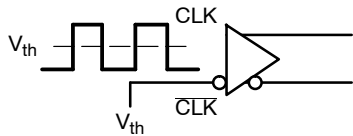


Figure 10. Differential Input Driven Single-Ended

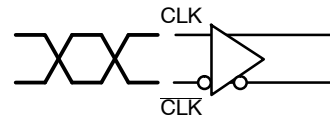


Figure 11. Differential Inputs Driven Differentially

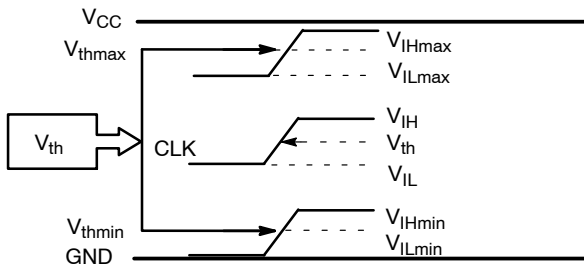


Figure 12. V_{th} Diagram

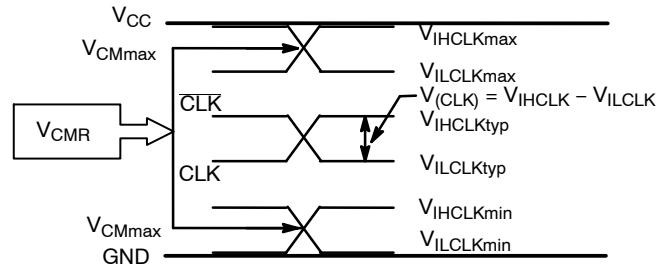


Figure 13. V_{CMR} Diagram

NB7L14M

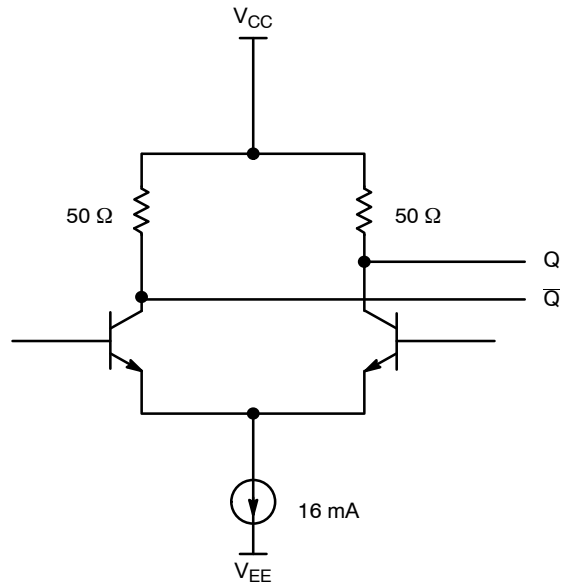


Figure 14. CML Output Structure

Table 6. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect V_{TCLK} and $\overline{V_{TCLK}}$ to V_{CC}
LVDS	Connect V_{TCLK} , $\overline{V_{TCLK}}$ Together for CLK Input
AC-COUPLED	Bias V_{TCLK} , $\overline{V_{TCLK}}$ Inputs within (VCMR) Common Mode Range
RSECL, LVPECL	Standard ECL Termination Techniques. See AND8020/D.
LVTTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTTL and $V_{CC}/2$ for LVCMOS inputs.

NB7L14M

Application Information

All NB7L14M inputs can accept PECL, CML, LVTTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are

minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a $50\ \Omega$ environment ($Z = 50\ \Omega$).

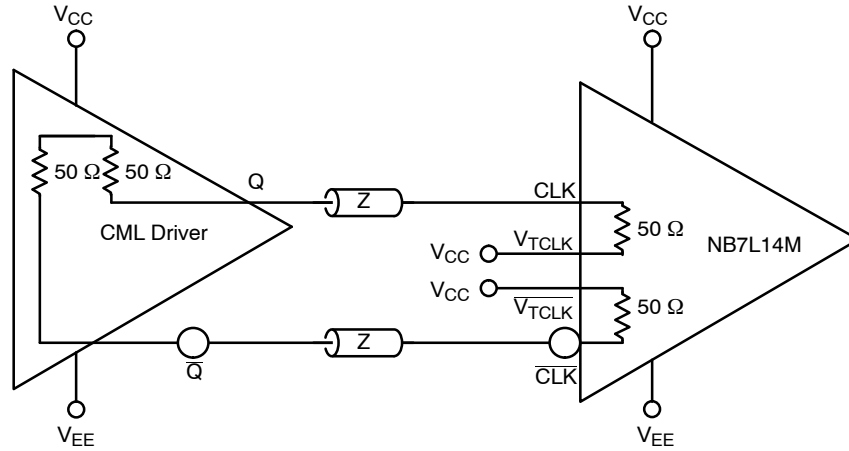


Figure 15. CML to CML Interface

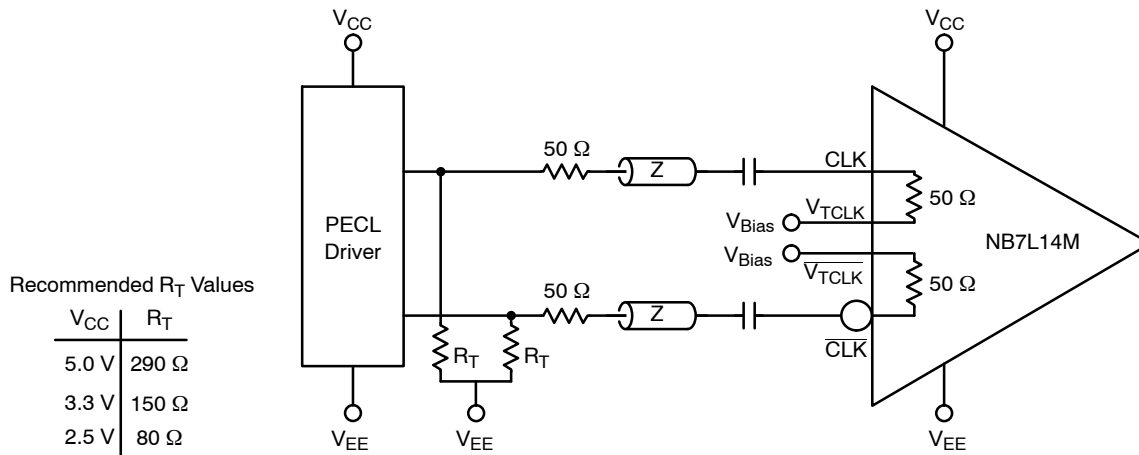


Figure 16. PECL to CML Receiver Interface

NB7L14M

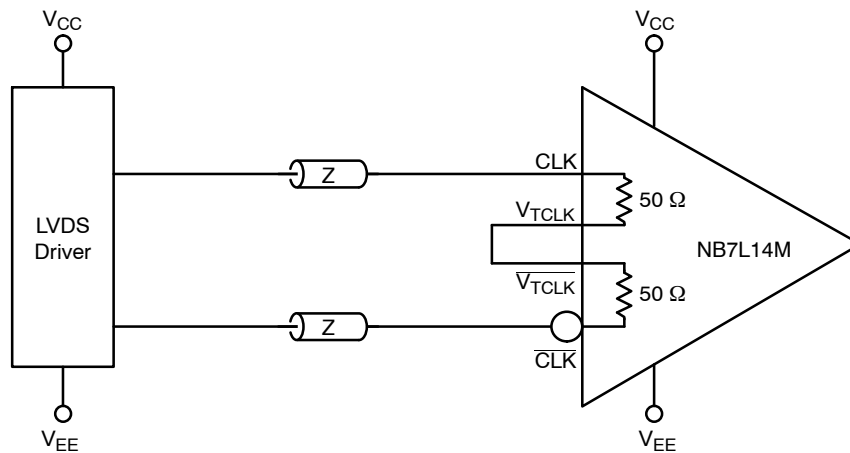


Figure 17. LVDS to CML Receiver Interface

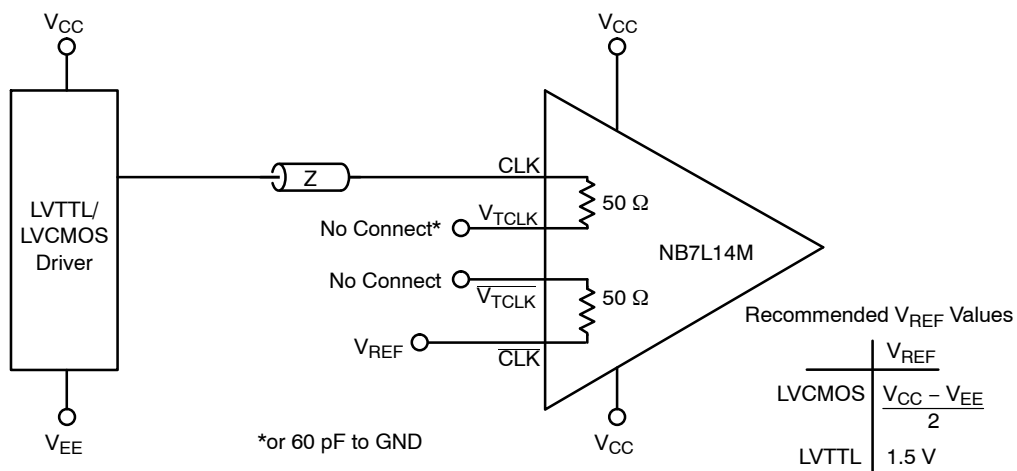


Figure 18. LVCMOS/LVTTL to CML Receiver Interface

ORDERING INFORMATION

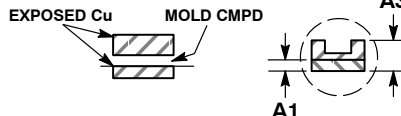
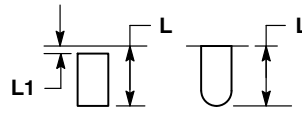
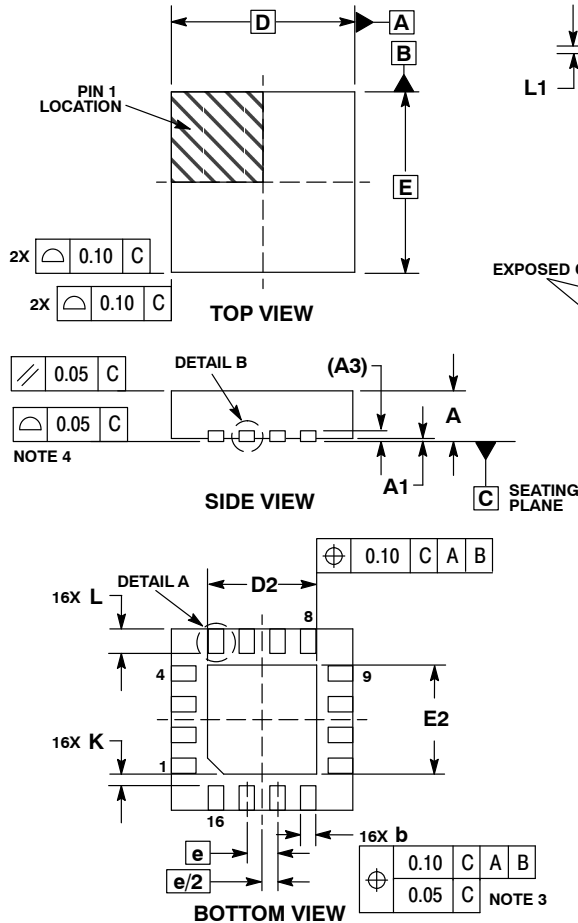
Device	Package	Shipping [†]
NB7L14MMNG	QFN-16 (Pb-Free)	123 Units/Rail
NB7L14MMNR2G	QFN-16 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7L14M

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

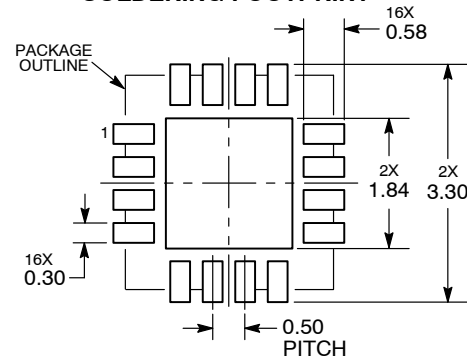


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative