

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NBSG14

2.5 V/3.3 V SiGe Differential 1:4 Clock/Data Driver with RSECL* Outputs

*Reduced Swing ECL

Description

The NBSG14 is a 1-to-4 clock/data distribution chip, optimized for ultra-low skew and jitter.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV. All outputs loaded with 50 Ω to $V_{CC} - 2$ V.

Features

- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.465 V
- RSECL Output Level (400 mV Peak-to-Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices
- These are Pb-Free Devices



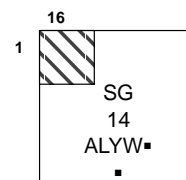
ON Semiconductor®

<http://onsemi.com>



QFN-16
MN SUFFIX
CASE 485G

MARKING DIAGRAMS*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NBSG14

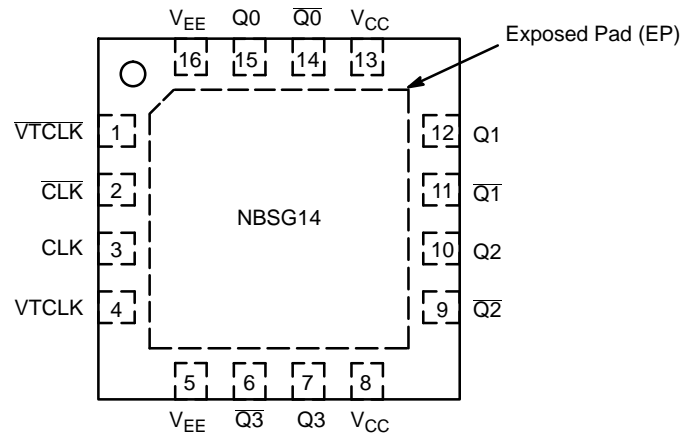


Figure 1. QFN-16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTCLK	-	Internal 50 Ω Termination pin. See Table 2.
2	CLK	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input. Internal 75 k Ω to V_{EE} and 36.5 k Ω to V_{CC} .
3	CLK	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input. Internal 75 k Ω to V_{EE} .
4	VTCLK	-	Internal 50 Ω Termination Pin. See Table 2.
5, 16	V_{EE}	-	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
6	$\overline{Q3}$	RSECL Output	Inverted Differential Output 3. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
7	Q3	RSECL Output	Noninverted Differential Output 3. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
8, 13	V_{CC}	-	Positive Supply Voltage. All V_{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
9	$\overline{Q2}$	RSECL Output	Inverted Differential Output 2. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
10	Q2	RSECL Output	Noninverted Differential Output 2. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
11	$\overline{Q1}$	RSECL Output	Inverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
12	Q1	RSECL Output	Noninverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
14	$\overline{Q0}$	RSECL Output	Inverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
15	Q0	RSECL Output	Noninverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2 V$
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pins (VTCLK, VTCLK) are connected to a common termination voltage, if no signal is applied then the device will be susceptible to self-oscillation.

NBSG14

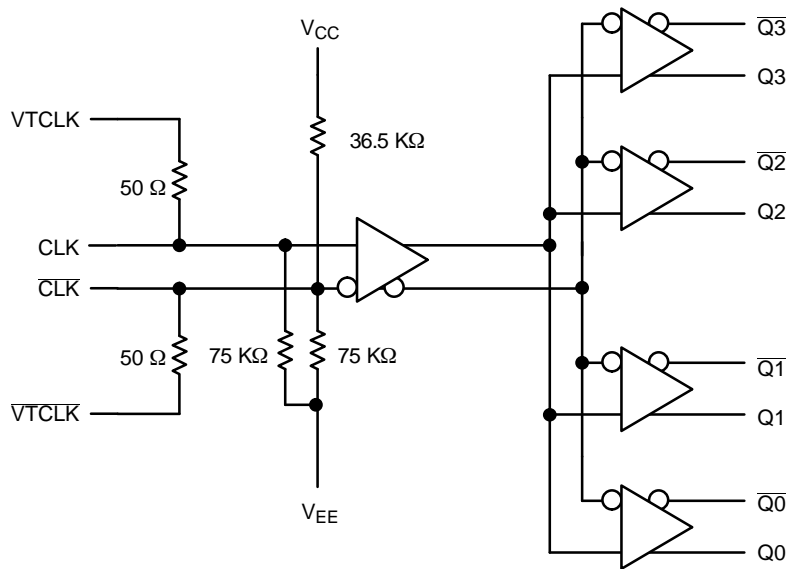


Figure 2. Logic Diagram

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and \overline{VTCLK} to V_{CC}
LVDS	Connect VTCLK and \overline{VTCLK} Together
AC-COUPLED	Bias VTCLK and \overline{VTCLK} Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTTL, LVCMOS	An External Voltage (V_{th}) should be Applied to the Unused Differential Input. Nominal V_{th} is 1.5 V for LVTTTL and $V_{CC}/2$ for LVCMOS Inputs. This Voltage must be within the V_{th} Specification.

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (CLK, \overline{CLK})	75 kΩ
Internal Input Pullup Resistor (\overline{CLK})	36.5 kΩ
ESD Protection	Human Body Model Machine Model > 2 kV > 100 V
Moisture Sensitivity (Note 1)	Pb-Free Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	158
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

NBSG14

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	$V_{EE} = 0\text{ V}$		3.6	V
V_{EE}	Negative Power Supply	$V_{CC} = 0\text{ V}$		-3.6	V
V_I	Positive Input Negative Input	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V
V_{INPP}	Differential Input Voltage [CLK-CLK]	$V_{CC} - V_{EE} \geq 2.8\text{ V}$ $V_{CC} - V_{EE} < 2.8\text{ V}$		2.8 $ V_{CC} - V_{EE} $	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA
I_{OUT}	Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			-40 to +70 -40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 2)	0 lfpm 500 lfpm		41.6 35.2	$^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 2)		4.0	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder (Pb-Free)			265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NBSG14

Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT

($V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$) (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

POWER SUPPLY CURRENT

I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
----------	-------------------------------	----	----	----	----	----	----	----	----	----	----

RSPECL OUTPUTS (Note 4)

V_{OH}	Output HIGH Voltage	1525	1575	1625	1550	1610	1650	1575	1635	1675	mV
V_{OUTPP}	Output Voltage Amplitude	315	405	495	315	405	495	315	405	495	mV

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 5)

V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		$V_{IH} - 150$	0		$V_{IH} - 150$	0		$V_{IH} - 150$	mV
V_{th}	Input Threshold Voltage Range (Note 6)	950		$V_{CC} - 75$	950		$V_{CC} - 75$	950		$V_{CC} - 75$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 7)

V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		$V_{IHD} - 75$	0		$V_{IHD} - 75$	0		$V_{IHD} - 75$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 8) (Figure 9)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@ V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
-----------	-------------------------------------	----	----	----	----	----	----	----	----	----	----------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} .
- All outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
- V_{IHD} , V_{ILD} , V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
- V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NBSG14

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT

($V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$) (Note 9)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

POWER SUPPLY CURRENT

I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
----------	-------------------------------	----	----	----	----	----	----	----	----	----	----

RSPECL OUTPUTS (Note 10)

V_{OH}	Output HIGH Voltage	2325	2375	2425	2350	2410	2450	2375	2435	2475	mV
V_{OUTPP}	Output Voltage Amplitude	350	440	530	350	440	530	350	440	530	mV

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 11)

V_{IH}	Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage	0		$V_{IH} - 150$	0		$V_{IH} - 150$	0		$V_{IH} - 150$	mV
V_{th}	Input Threshold Voltage Range (Note 12)	950		$V_{CC} - 75$	950		$V_{CC} - 75$	950		$V_{CC} - 75$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 13)

V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		$V_{IHD} - 75$	0		$V_{IHD} - 75$	0		$V_{IHD} - 75$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14) (Figure 9)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@ V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
-----------	-------------------------------------	----	----	----	----	----	----	----	----	----	----------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with V_{CC} .

10. All outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

11. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.

12. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.

13. V_{IHD} , V_{ILD} , V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.

14. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NBSG14

Table 7. DC CHARACTERISTICS, NECL or RSNECL INPUT WITH NECL OUTPUT

($V_{CC} = 0$ V; $V_{EE} = -3.465$ V to -2.375 V) (Note 15)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

POWER SUPPLY CURRENT

I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
----------	-------------------------------	----	----	----	----	----	----	----	----	----	----

RSPECL OUTPUTS (Note 16)

V_{OH}	Output HIGH Voltage	-975	-925	-875	-950	-890	-850	-925	-865	-825	mV
V_{OUTPP}	Output Voltage Amplitude -3.465 V \leq $V_{EE} \leq$ -3.0 V -3.0 V $<$ $V_{EE} \leq$ -2.375 V	350 315	440 405	530 495	350 315	440 405	530 495	350 315	440 405	530 495	mV

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 5 & 7) (Note 17)

V_{IH}	Input HIGH Voltage	$V_{EE} + 1200$		V_{CC}	$V_{EE} + 1200$		V_{CC}	$V_{EE} + 1200$		V_{CC}	mV
V_{IL}	Input LOW Voltage	V_{EE}		$V_{IH} - 150$	V_{EE}		$V_{IH} - 150$	V_{EE}		$V_{IH} - 150$	mV
V_{th}	Input Threshold Voltage Range (Note 18)	$V_{EE} + 950$		$V_{CC} - 75$	$V_{EE} + 950$		$V_{CC} - 75$	$V_{EE} + 950$		$V_{CC} - 75$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	150		2600	150		2600	150		260	mV

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 & 8) (Note 19)

V_{IHD}	Differential Input HIGH Voltage	$V_{EE} + 1200$		V_{CC}	$V_{EE} + 1200$		V_{CC}	$V_{EE} + 1200$		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		$V_{IHD} - 75$	V_{EE}		$V_{IHD} - 75$	V_{EE}		$V_{IHD} - 75$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 20) (Figure 9)	$V_{EE} + 1200$		0	$V_{EE} + 1200$		0	$V_{EE} + 1200$		0	mV
I_{IH}	Input HIGH Current (@ V_{IH})		80	150		80	150		80	150	μ A
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μ A

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
-----------	-------------------------------------	----	----	----	----	----	----	----	----	----	----------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

15. Input and output parameters vary 1:1 with V_{CC} .

16. All outputs loaded with 50 Ω to $V_{CC} - 2.0$ V.

17. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.

18. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.

19. V_{IHD} , V_{ILD} , V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.

20. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NBSG14

Table 8. AC CHARACTERISTICS

($V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.465 V ; $V_{EE} = 0\text{ V}$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input Clock Frequency (See Figure 3) (Note 21)	10.5	12		10.5	12		10.5	12		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
t_{SKEW}	Duty Cycle Skew (Note 22) Within-Device Skew (Note 23) Device-to-Device Skew (Note 24)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
t_{JITTER}	RMS Random Clock Jitter (Figure 3) (Note 26) $f_{in} < 10\text{ GHz}$ Peak-to-Peak Data Dependent Jitter (Note 27) $f_{in} < 10\text{ Gb/s}$		0.2	1		0.2 10	1		0.2	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 25)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, \bar{Q} (20% – 80%) @ 1 GHz	15	30	55	20	30	55	20	30	55	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

21. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$. Input edge rates 40 ps (20% – 80%)

22. See Figure 10. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.

23. Within-Device skew is measured between outputs under identical transitions and conditions on any one device.

24. Device-to-Device skew for identical transitions at identical V_{CC} levels.

25. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (applicable only when $V_{CC} - V_{EE} < 2600\text{ mV}$).

26. Additive RMS Jitter with 50% duty cycle clock signal at 10 GHz.

27. Additive Peak-to-Peak data dependent jitter with NRZ PRBS $2^{31}-1$ data at 10 Gb/s.

NBSG14

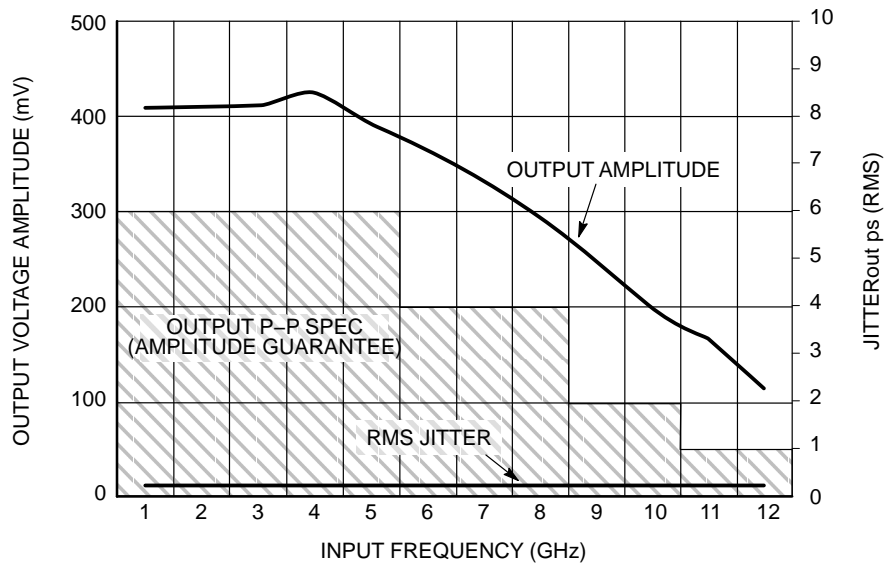
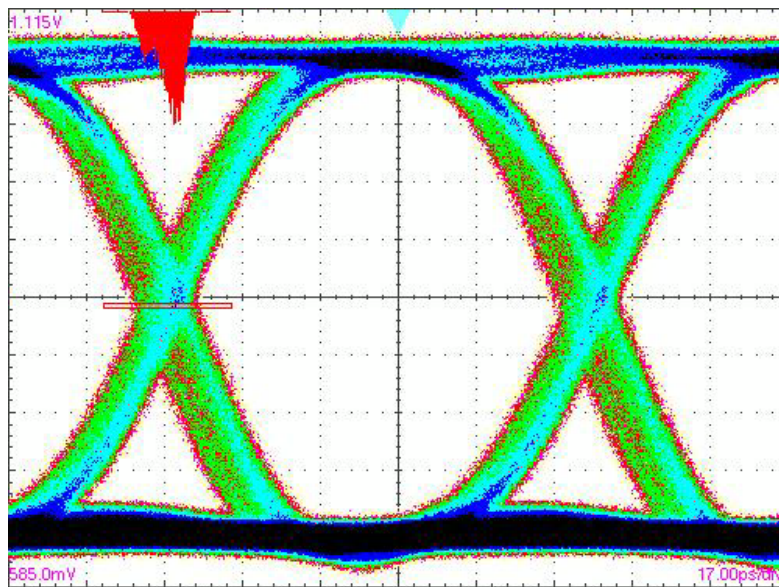


Figure 3. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)



X = 17 ps/DIV, Y = 53 mV/DIV

Figure 4. Eye Diagram at 10.8 Gbps
 ($V_{CC} - V_{EE} = 3.3 \text{ V}$ @ 25°C with Input Data Pattern of $2^{31}-1$ PRBS.
 Total Pk-Pk System Jitter Including Signal Generator is 18 ps.
 This Data was taken by Acquiring 7000 Waveforms.)

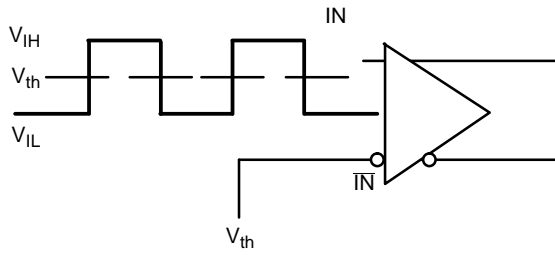


Figure 5. Differential Input Driven Single-Ended

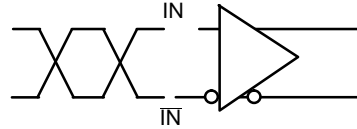


Figure 6. Differential Inputs Driven Differentially

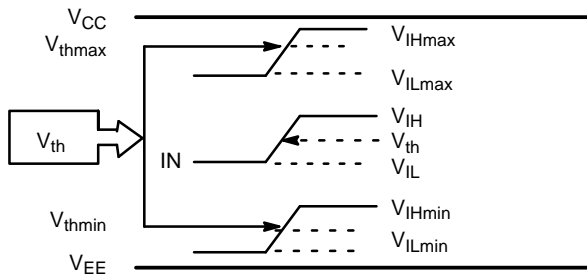


Figure 7. V_{th} Diagram

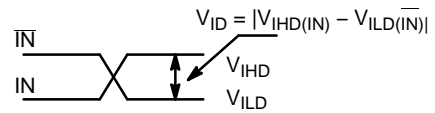


Figure 8. Differential Inputs Driven Differentially

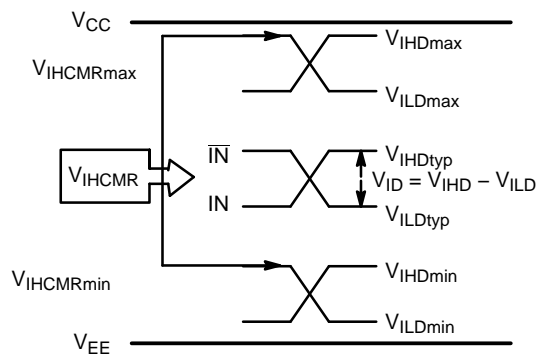


Figure 9. V_{IHCMR} Diagram

NBSG14

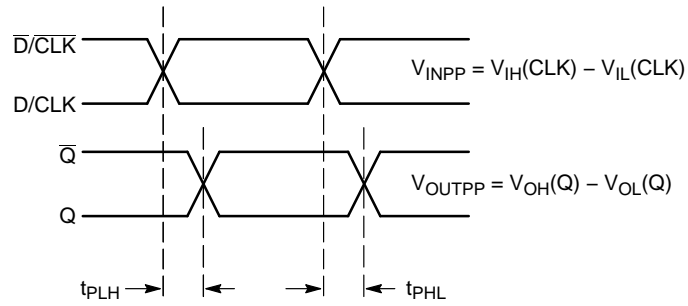


Figure 10. AC Reference Measurement

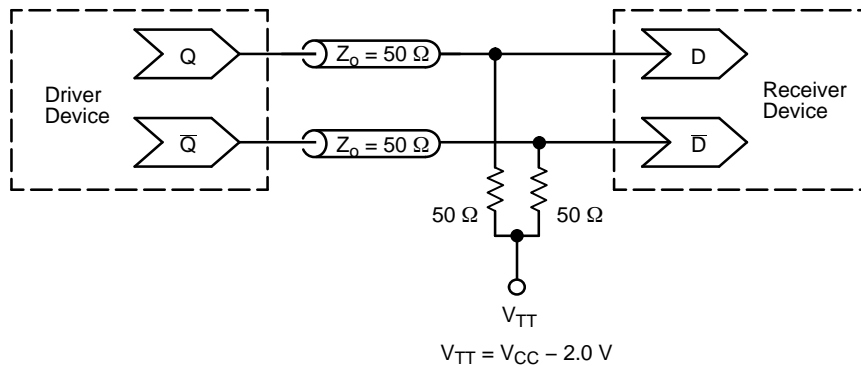


Figure 11. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

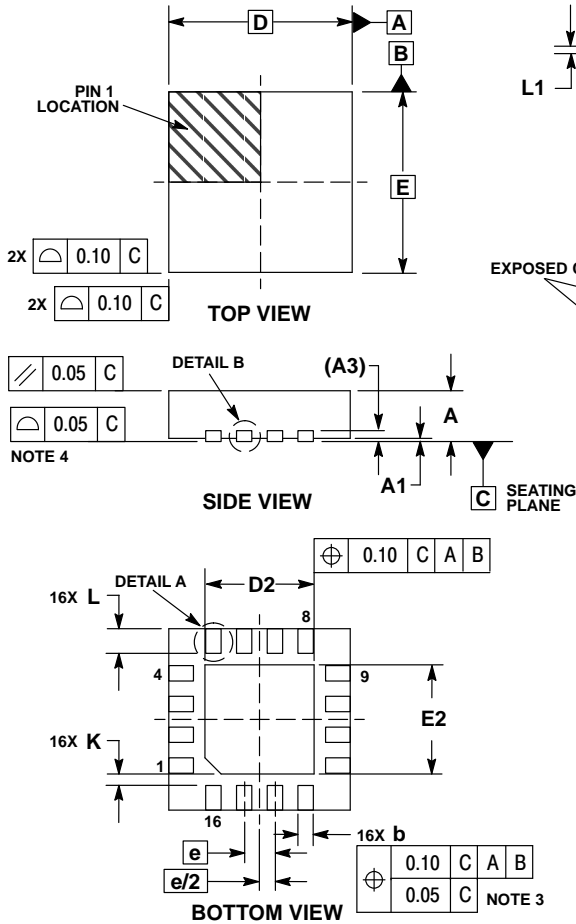
Device	Package	Shipping [†]
NBSG14MNG	QFN-16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG14MNR2G	QFN-16 (Pb-Free / Halide-Free)	3000 / Tape & Reel
NBSG14MNHTBG	QFN-16 (Pb-Free / Halide-Free)	100 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NBSG14

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

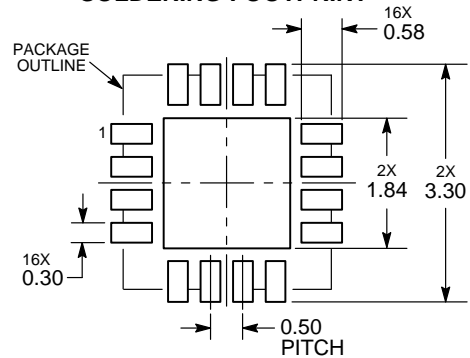


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative