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OSCILLATOR, MULTIPLIER, AND BUFFER WITH 8 OUTPUTS ICS552A-01

Description

The ICS552A-01 produces 8 low-skew copies of the multiple input clock or fundamental, parallel-mode crystal. Unlike other clock drivers, these parts do not require a separate oscillator for the input. Using IDT's patented Phase-Locked Loop (PLL) to multiply the input frequency, it is ideal for generating and distributing multiple high-frequency clocks. **This is a single chip used for 3 different applications:**

1) ICS552A-01 (A mode) — an Oscillator mutiplier

2) ICS552A-01 (B mode) — a Dual 1:4 buffer

3) ICS552A-01 (C mode) — a 1:8 Oscillator buffer

Features (all)

- Packaged as 20-pin SSOP (QSOP)
- Pb-free packaging available
- Operating voltages of 3.0 V to 5.5 V
- Industrial temperature available

Features (specific)

ICS552A-01 (for A mode)

- Contains on-chip multiplier with selections of x1, x1.33, x2, x2.66, x3, x3.33, x4, x4.66, x5, and x6
- Power-down and Tri-state modes

ICS552A-01 (for B mode)

- Up to 200 MHz clock input/output at 3.3 V
- Low skew of 250 ps maximum for any bank of four
- Inputs can be connected together for a 1 to 8 buffer with 250 ps skew between any outputs
- Non-inverting buffer mode
- Ideal for clock networks
- Output Enable mode tri-states outputs
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process

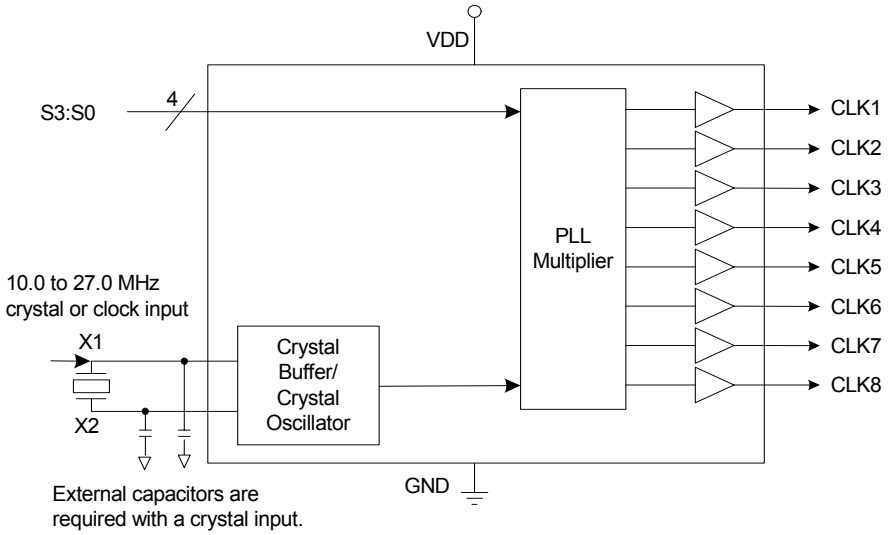
ICS552A-01 (for C mode)

- Use with 25 MHz crystal for networking
- Use with 27 MHz crystal for MPEG

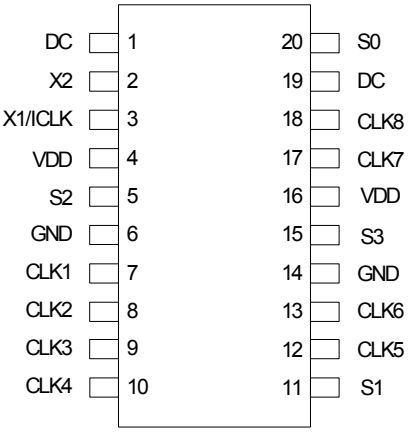
ICS552A-01 (for A and C modes)

- Input frequency of 10.0 to 27.0 MHz
- Provides 8 low-skew outputs (<250 ps)
- Output clock duty cycle of 40/60 at 3.3 V

Block Diagram (ICS552A-01—A mode)



Pin Assignment (ICS552A-01—A mode)



20-pin (150 mil) SSOP (QSOP)

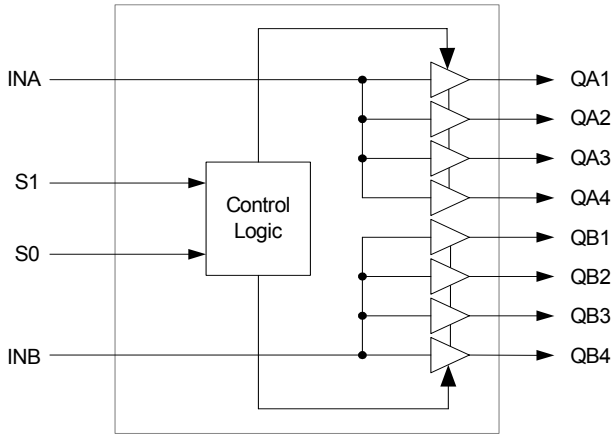
Multiplier Select Table

S3	S2	S1	S0	Multiplier
0	0	0	0	Power Down
0	0	0	1	x1
0	0	1	0	x1.333
0	0	1	1	x2
0	1	0	0	x2.666
0	1	0	1	x3
0	1	1	0	x3.333
0	1	1	1	x4
1	0	0	0	x5
1	0	0	1	x4.66
1	0	1	0	x6
1	1	0	1	Tri-state all

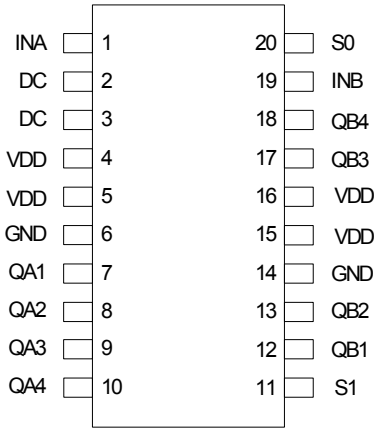
Pin Descriptions (ICS552A-01—A mode)

Pin Number	Pin Name	Pin Type	Pin Description
1	DC	—	Do not connect.
2	X2	XO	Crystal connection. Connect to a 10 - 27 MHz fundamental mode crystal.
3	X1/ICLK	XI	Crystal connection. Connect to a 10 - 27 MHz fundamental mode crystal or clock.
4	VDD	Power	Connect to +3.3 V or 5 V. Decouple with pin 6. Must be same as other VDDs.
5	S2	Input	Multiplier Select pin 2 per table above.
6	GND	Power	Connect to ground.
7	CLK1	Output	Output clock 1.
8	CLK2	Output	Output clock 2.
9	CLK3	Output	Output clock 3.
10	CLK4	Output	Output clock 4.
11	S1	Input	Multiplier Select pin 1 per table above
12	CLK5	Output	Output clock 5.
13	CLK6	Output	Output clock 6.
14	GND	Power	Connect to ground.
15	S3	Input	Multiplier Select pin 3 per table above
16	VDD	Power	Connect to +3.3 V or 5 V. Decouple with pin 14. Must be same as other VDDs.
17	CLK7	Output	Output clock 7.
18	CLK8	Output	Output clock 8.
19	DC	—	Do not connect.
20	S0	Input	Multiplier Select pin 0 per table above

Block Diagram (ICS552A-01—B mode)



Pin Assignment (ICS552A-01—B mode)



20-pin (150 mil) SSOP (QSOP)

Clock Output Select Table (ICS552A-01—B mode)

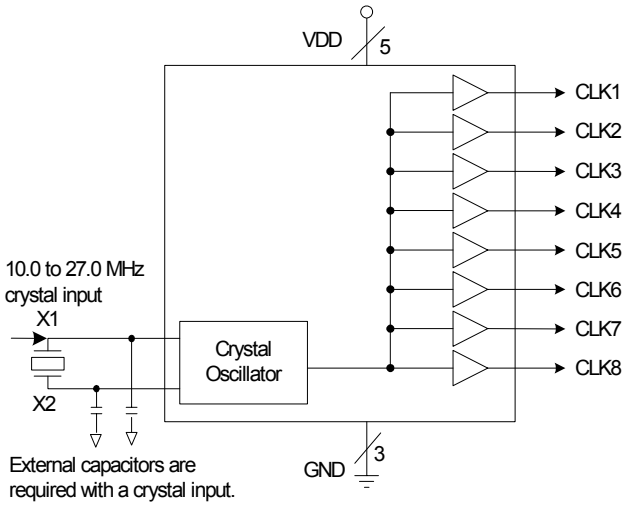
S1	S0	Mode
0	0	QA1:4 and QB1:4 running
0	1	Test mode
1	0	OE. All outputs in high impedance
1	1	QA1:4 only. QB1:4 stopped low

Pin Descriptions (ICS552A-01—B mode)

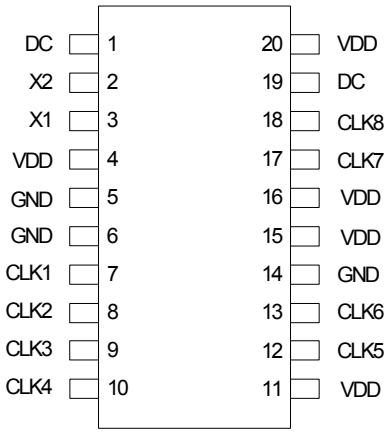
Pin Number	Pin Name	Pin Type	Pin Description
1	INA	CI	Input to buffer A. Outputs QA1:4 will be the same frequency. Internal pull-up resistor.
2	DC	—	Do not connect.
3	DC	—	Do not connect.
4	VDD	Power	Connect to +3.3 V or 5.0 V. Must be same as other VDDs.
5	VDD	Power	Connect to +3.3 V or 5.0 V. Must be same as other VDDs.
6	GND	Power	Connect to ground.
7	QA1	Output	Output 1 from buffer A.
8	QA2	Output	Output 2 from buffer A.
9	QA3	Output	Output 3 from buffer A.
10	QA4	Output	Output 4 from buffer A.
11	S1	I	Mode Select pin 1. Selects mode for outputs. Must be at GND for all clocks on. Internal pull-up resistor.
12	QB1	Output	Output 1 from buffer B.
13	QB2	Output	Output 2 from buffer B.
14	GND	Power	Connect to ground.
15	VDD	Power	Connect to +3.3 V or 5.0 V. Must be same as other VDDs.
16	VDD	Power	Connect to +3.3 V or 5.0 V. Must be same as other VDDs.
17	QB3	Output	Output 3 from buffer B.
18	QB4	Output	Output 4 from buffer B.
19	INB	CI	Input to buffer B. Outputs QA1:4 will be the same frequency. Internal pull-up resistor.
20	S0	I	Mode Select pin 0. Selects mode for outputs. Must be at GND for all clocks on. Internal pull-up resistor.

KEY: CI = clock input with pull-up resistor; I = input with internal pull-up resistor.

Block Diagram (ICS552A-01—C mode)



Pin Assignment (ICS552A-01—C mode)



20-pin (150 mil) SSOP (QSOP)

Pin Descriptions (ICS552A-01—C mode)

Pin Number	Pin Name	Pin Type	Pin Description
1	DC	—	Do not connect.
2	X2	XO	Crystal connection. Connect to a 10 - 27 MHz fundamental mode crystal.
3	X1	XI	Crystal connection. Connect to a 10 - 27 MHz fundamental mode crystal.
4	VDD	Power	Connect to +3.3 V or 5 V. Decouple with pin 6. Must be same as other VDDs.
5	GND	Power	Connect to ground.
6	GND	Power	Connect to ground.
7	CLK1	Output	Output clock 1.
8	CLK2	Output	Output clock 2.
9	CLK3	Output	Output clock 3.
10	CLK4	Output	Output clock 4.
11	VDD	Power	Connect to +3.3 V or 5 V. Must be same as other VDDs.
12	CLK5	Output	Output clock 5.
13	CLK6	Output	Output clock 6.
14	GND	Power	Connect to ground.
15	VDD	Power	Connect to +3.3 V or 5 V. Must be same as other VDDs.
16	VDD	Power	Connect to +3.3 V or 5 V. Decouple with pin 14. Must be same as other VDDs.
17	CLK7	Output	Output clock 7.
18	CLK8	Output	Output clock 8.
19	DC	—	Do not connect.
20	VDD	Power	Connect to +3.3 V or 5 V. Must be same as other VDDs.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS552A-01 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and GND on pins 4 and 6, and 16 and 14. Other VDDs and GNDs can be connected to these pins or directly to their respective ground planes.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -12 pF)*2. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 18 pF load capacitance, two 12 pF capacitors should be used. For a clock input, connect it X1/ICLK and leave X2 unconnected (floating).

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS552A-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	°C
Ambient Operating Temperature (industrial)	-40		+85	°C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V or 5 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1	VDD/2		V
Input Low Voltage	V_{IL}	ICLK		VDD/2	VDD/2-1	V
Input High Voltage	V_{IH}	S3:S0	2			V
Input Low Voltage	V_{IL}	S3:S0			0.8	V
Output High Voltage	V_{OH}	VDD = 3.3 V, I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	VDD = 3.3 V, I_{OL} = 8 mA			0.4	V
Output High Voltage	V_{OH}	VDD = 3.3 V or 5 V, I_{OH} = -8 mA	VDD-0.4			V
Short Circuit Current	I_{OS}	VDD = 3.3 V, each output		±50		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	I_{DD}	at 3.3 V, no load, 25 MHz in, x4		35		mA
Operating Supply Current	I_{DD}	at 5 V, no load, 25 MHz in, x4		59		mA
Power-down Supply Current	I_{DD}	S3:S0 = 0 (GND)		55		µA

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V or 5 V**, Ambient Temperature -40 to +85° C

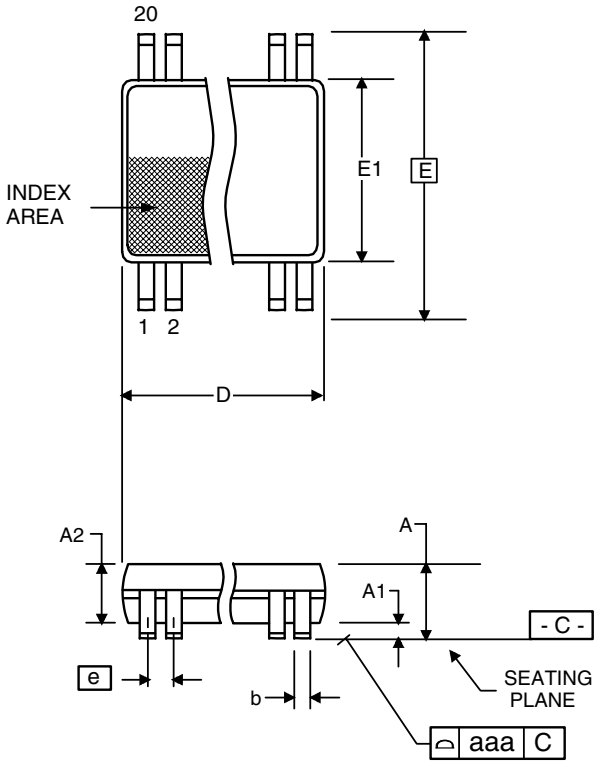
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental crystal	10		27	MHz
		Input clock–non-buffer mode	10		27	MHz
		Input clock–buffer mode only	10		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V			1.5	ns
Duty Cycle		at VDD/2	40	50	60	%
Output-to-Output Skew		All modes, Rising edges at VDD/2			250	ps
Absolute Jitter		Mode A, Deviation from Mean		±75		ps
One Sigma Clock Period Jitter		Mode A		25		ps

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		135		°C/W
	θ_{JA}	1 m/s air flow		93		°C/W
	θ_{JA}	3 m/s air flow		78		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	--	1.50	--	0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	.635 Basic		.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
552AR-01LF	552AR-01LF	Tubes	20-pin SSOP	0 to +70° C
552AR-01LFT	552AR-01LF	Tape and Reel	20-pin SSOP	0 to +70° C
552ARI-01LF	552ARI01LF	Tubes	20-pin SSOP	-40 to +85° C
552ARI-01LFT	552ARI01LF	Tape and Reel	20-pin SSOP	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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