

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

USER CONFIGURABLE DIVIDER

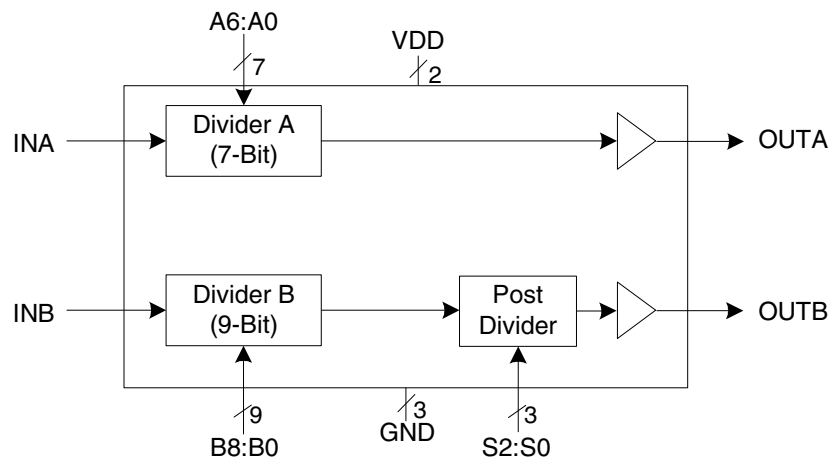
ICS674-01

Description

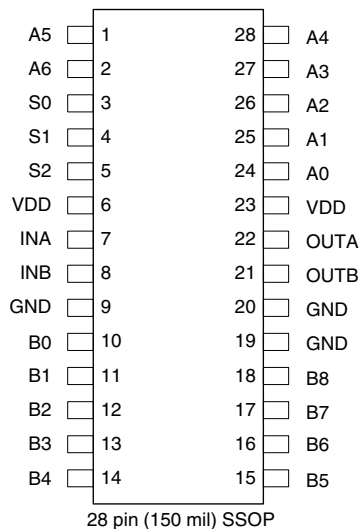
The ICS674-01 consists of two separate configurable dividers. The A Divider is a 7-bit divider and can divide by 3 to 129. The B Divider consists of a 9-bit divider followed by a post divider. The 9-bit divider can divide by 12 to 519. The post divider has eight settings of 1, 2, 4, 5, 6, 7, 8, and 10; giving a maximum total divide of 5190. The A and B Dividers can be cascaded to give a maximum divide of 669510. The ICS674-01 supports the ICS673 PLL Building Block and enables the user to build a full custom PLL synthesizer.

Features

- Packaged in 28-pin SSOP (150 mil body)
- Pb (lead) free package, RoHS compliant
- General purpose programmable divider
- Supports ICS673 PLL Building Block
- User determines the divide by setting input pins
- Pull-ups on all select inputs
- Includes one 7-bit Divider for OUTA
- Includes one 9-bit Divider and one selectable Post Divider for OUTB
- Industrial temperature range available
- 25 mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltage of 3.3 V or 5 V

Block Diagram


Pin Assignment



Post Divider Table

S2 Pin 5	S1 Pin 4	S0 Pin 3	Post Divide
0	0	0	10
0	0	1	2
0	1	0	8
0	1	1	4
1	0	0	5
1	0	1	7
1	1	0	1
1	1	1	6

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 2, 24 - 28	A5, A6, A0-A4	Input	Divider A word input pins. Forms a number from 1 to 127. Internal pull-up resistors. See page 3 for details.
3 - 5	S0, S1, S2	Input	Select pins for Post Divider. See table above. Internal pull-up resistors.
6, 23	VDD	Power	Connect to VDD.
7	INA	Input	Divider A input.
8	INB	Input	Divider B input.
9, 19 - 20	GND	Power	Connect to ground.
10 - 18	B0 - B8	Input	Divider B word input pins. Forms a number from 4 to 511. Internal pull-up resistors. See page 3 for details.
21	OUTB	Output	Divider B output.
22	OUTA	Output	Divider A output.

External Components

The ICS674-01 requires a minimum number of external components for proper operation. A 0.01 μ F decoupling capacitor should be connected between each VDD and GND as close to the device as possible. A series termination resistor of 33 Ω should be used in series with OUTA and OUTB pins.

Determining (setting) the Divider

The user has full control in setting the desired divide. The user should connect the appropriate divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, ensuring that the ICS674-01 will automatically produce the correct divide when all components are soldered. It is also possible to connect the inputs to parallel I/O ports in order to change divides. The divides of the ICS674-01 can be determined by the following equations:

$$\text{Divide A} = \text{DAW} + 2$$

Where Divider A Word (DAW) = 1 to 127 (0 is not permitted)

$$\text{Divide B} = (\text{DBW} + 8) \times \text{PD}$$

Where Divider B Word (DBW) = 4 to 511 (0, 1, 2, 3 are not permitted)

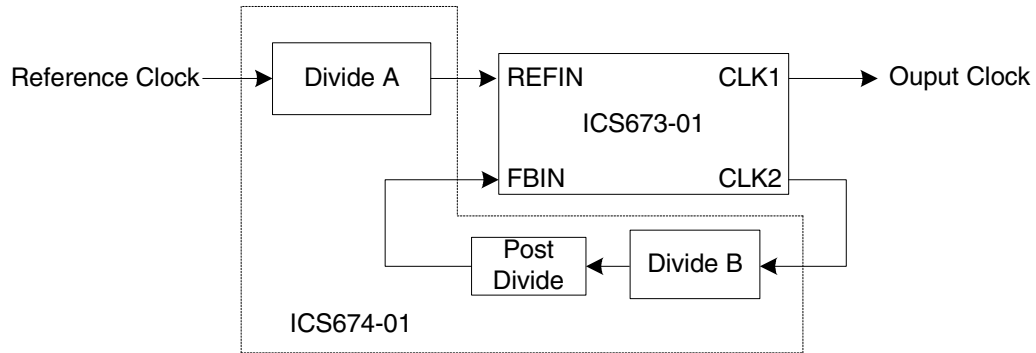
Post Divider (PD) = values on page 2

For example, suppose Divide A is desired to be 61 and Divide B is desired to be 284, then DAW = 59, DBW = 276, and PD = 1. This means A6:A0 is 0111011, B8:B0 is 100010100 and S2:S0 is 110. Since all inputs have pull-ups, it is only necessary to ground the zero pins, namely A6, A2, B7, B6, B5, B1, B0, and S0.

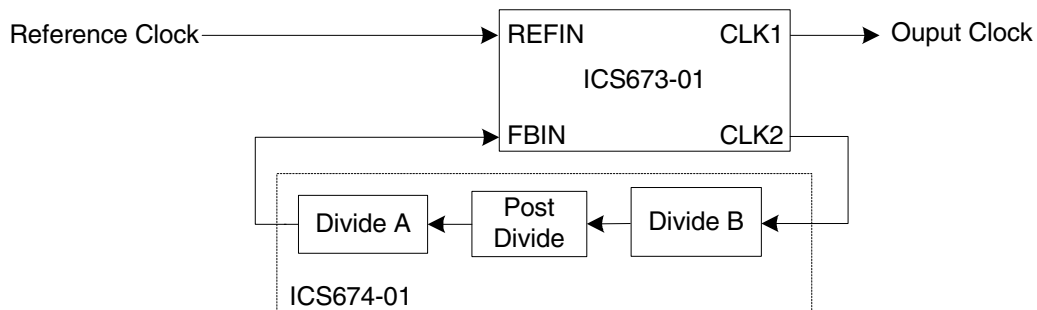
These configuration pins can be changed at any time during operation.

Using the ICS674-01 with the ICS673-01:

The ICS674-01 may be used with the ICS673-01 to build a frequency synthesizer. The following example shows a typical application when the reference clock is in the MHz range:



If the reference is in the kHz range, for example 8 kHz, the following configuration may be more typical:



Note that in both examples, Divide B is connected to the output of the ICS673. This is because Divide B has a higher operating frequency than Divide A.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS674-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
CLKIN and FBIN inputs	-0.5 V to 5.5 V
Electrostatic Discharge	2000 V
Ambient Operating Temperature	0 to +70° C
Ambient Operating Temperature (I version)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=5 V ±10%, Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V _{IH}	All A, B, and S pins	2			V
Input Low Voltage	V _{IL}	All A, B, and S pins			0.8	V
Input High Voltage	V _{IH}	INA and INB only	(VDD/2)+1	VDD/2		V
Input Low Voltage	V _{IL}	INA and INB only		VDD/2	(VDD/2)-1	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
Operating Supply Current DivA=DivB=20	IDD	No load, f _{in} =100 MHz 3.3 V		3		mA
		No load, f _{in} =100 MHz 5 V		5		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Short Circuit Current	I_{OS}	Each output		±70		mA
On-Chip Pull-up Resistor	R_{PU}	A, B, S select pins		270		kΩ
Input Capacitance	C_{IN}	A, B, S select pins		5		pF

AC Electrical Characteristics

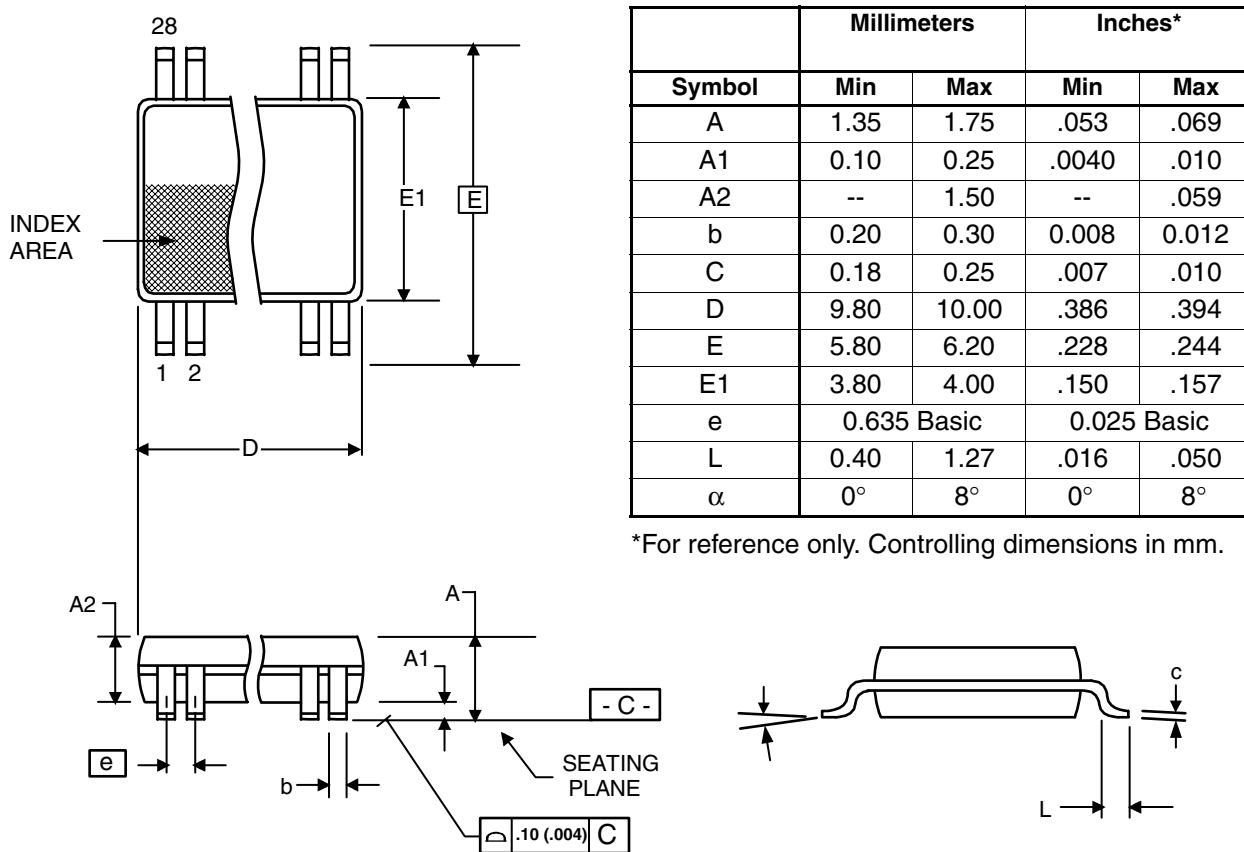
VDD = 5 V, Ambient Temperature -40 to +85° C, C_{LOAD} at CLK = 15 pF, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, Divider A	f_{IN}	3.3 V	0		135	MHz
Input Frequency, Divider B		3.3 V	0		180	MHz
Input Frequency, Divider A		5 V	0		200	MHz
Input Frequency, Divider B		5 V	0		235	MHz
Input Frequency, Divider A (Industrial temperature)	f_{IN}	at 3.3 V, +85° C	0		125	MHz
Input Frequency, Divider B (Industrial temperature)		at 3.3 V, +85° C	0		170	MHz
Input Frequency, Divider A (Industrial temperature)		at 5 V, +85° C	0		190	MHz
Input Frequency, Divider B (Industrial temperature)		at 5 V, +85° C	0		220	MHz
Output Rise Time	t_{OR}	20% to 80%		1.5		ns
Output Fall Time	t_{OF}	80% to 20%		1.5		ns
OUTB Clock Duty Cycle ¹	t_{DC}	at VDD/2	45	49 to 51	55	%
OUTB Clock Duty Cycle odd post dividers		at VDD/2, except PD=1	40		60	%
OUTA Clock Duty Cycle ¹		at VDD/2	20		98.5	%
Peak-to-Peak Jitter		15 pF			400	ps
Cycle-to-Cycle Jitter		30 pF loads			300	ps
Propagation Delay, Divider A	T_{PA}	VDD = 3.3 V, +25° C		6.5		ns
		VDD = 5.0 V, +25° C		4.5		ns
Propagation Delay, Divider B + Post Divider	T_{PB}	VDD = 3.3 V, +25° C		20		ns
		VDD = 5.0 V, +25° C		13		ns

¹ The duty cycle of OUTA is dependent on the selected divide. This because OUTA goes low for 1 input clock cycles on INA. For example, if a divide of 20 is selected, the duty cycle will be 90%. Similarly, if PD=1 is selected for OUTB, the duty cycle will be dependent on the selected divide. In this case, OUTB goes high for approximately 8 input clock cycles on INB.

Package Outline and Package Dimensions (28-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
674R-01LF	674R-01LF	Tubes	28-pin SSOP	0 to +70° C
674R-01LFT	674R-01LF	Tape and Reel	28-pin SSOP	0 to +70° C
674R-01ILF	674R-01ILF	Tubes	28-pin SSOP	-40 to 85° C
674R-01ILFT	674R-01ILF	Tape and Reel	28-pin SSOP	-40 to 85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high-reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com