

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

LOCO™ PLL CLOCK MULTIPLIER
ICS511
Description

The ICS511 LOCO™ is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz.

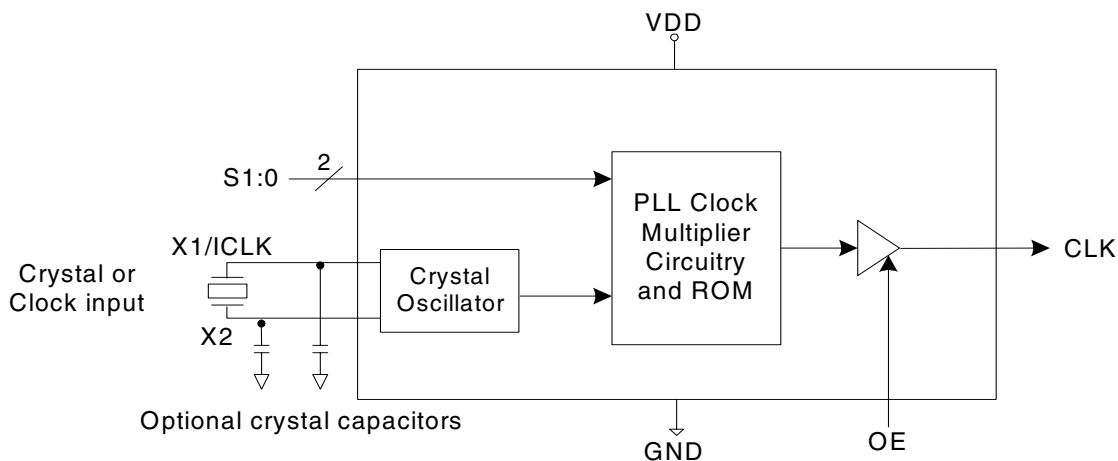
Stored in the chip's ROM is the ability to generate nine different multiplication factors, allowing one chip to output many common frequencies (see table on page 2).

The device also has an output enable pin which tri-states the clock output when the OE pin is taken low.

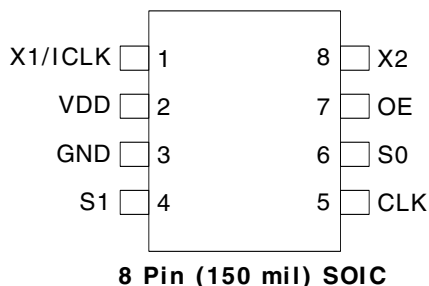
This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed. For applications which require defined input to output skew, use the ICS570B.

Features

- Packaged as 8-pin SOIC or die
- Pb (lead) free package
- Upgrade of popular ICS501 with:
 - changed multiplier table
 - faster operating frequencies
 - output duty cycle at VDD/2
- Zero ppm multiplication error
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 200 MHz
- Extremely low jitter of 25 ps (one sigma)
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 200 MHz
- Mask option for nine selectable frequencies
- Operating voltage of 3.3 V or 5 V
- Tri-state output for board level testing
- Industrial temperature version available
- Advanced, low power CMOS process

Block Diagram


Pin Assignment



Clock Output Table

S1	S0	CLK
0	0	4X input
0	M	5.333X input
0	1	5X input
M	0	2.5X input
M	M	2X input
M	1	3.333X input
1	0	6X input
1	M	3X input
1	1	8X input

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Common Output Frequency Examples (MHz)

Output	20	24	30	32	33.33	37.5	40	48	50	60	64
Input	10	12	10	16	16.66	15	10	12	20	10	16
Selection (S1, S0)	M, M	M, M	1, M	M, M	M, M	M, 0	0, 0	0, 0	M, 0	1, 0	0, 0
Output	66.66	72	75	80	83.33	90	100	120	125	133.3	150
Input	20	12	25	10	25	15	20	15	25	25	25
Selection (S1, S0)	M, 1	1, 0	1, M	1, 1	M, 1	1, 0	0, 1	1, 1	0, 1	0, M	1, 0

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI/ICLK	Input	Crystal connection or clock input.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	S1	Tri-level input	Select 1 for output clock. Connect to GND or VDD or float.
5	CLK	Output	Clock output per table above.

Pin Number	Pin Name	Pin Type	Pin Description
6	S0	Tri-level Input	Select 0 for output clock. Connect to GND or VDD or float.
7	OE	Input	Output enable. Tri-states CLK output when low. Internal pull-up resistor.
8	X2	Output	Crystal connection. Leave unconnected for clock input.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS511 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01μF must be connected between VDD and the GND. It must be connected close to the ICS511 to minimize lead inductance. No external power supply filtering is required for the ICS511.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the

stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 12 \text{ pF}) \times 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF $[(16-12) \times 2] = 8$.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS511. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (Commercial grade)	0 to +70° C
Ambient Operating Temperature (Industrial grade)	-40 to +85° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.135		+5.25	V

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, ICLK only	V _{IH}	ICLK (pin 1)	(VDD/2)+0.7			V
Input Low Voltage, ICLK only	V _{IL}	ICLK (pin 1)			(VDD/2)-0.7	V
Input High Voltage	V _{IH}	OE (pin 7)	2.0			V
Input Low Voltage	V _{IL}	OE (pin 7)			0.8	V
Input High Voltage	V _{IH}	S0, S1	VDD-0.5			V
Input Low Voltage	V _{IL}	S0, S1			0.5	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
IDD Operating Supply Current, 20 MHz crystal		No load, 100M		8		mA
Short Circuit Current		CLK output		±70		mA
On-Chip Pull-up Resistor		Pin 7		270		kΩ
Input Capacitance, S1, S0, and OE		Pins 4, 6, 7		4		pF
Nominal Output Impedance				20		Ω

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F _{IN}		5		27	MHz
Input Frequency, clock input	F _{IN}		2		50	MHz
Output Frequency	F _{OUT}	0° C to +70° C	14		160	MHz
		-40° C to +85° C	14		145	MHz
Output Clock Rise Time	t _{OR}	0.8 to 2.0 V, Note 1		1	1.5	ns
Output Clock Fall Time	t _{OF}	2.0 to 8.0 V, Note 1		1	1.5	ns
Output Clock Duty Cycle	t _{OD}	1.5 V, up to 160 MHz	45	49-51	55	%
PLL Bandwidth			10			kHz
Output Enable Time, OE high to output on				50		ns
Output Disable Time, OE low to tri-state				50		ns
Absolute Clock Period Jitter	t _{ja}	Deviation from mean		±70		ps
One Sigma Clock Period Jitter	t _{js}			25		ps

Note 1: Measured with 15 pF load.

DC Electrical Characteristics

VDD=5.0 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.75		5.25	V
Input High Voltage, ICLK only	V _{IH}	ICLK (pin 1)	(VDD/2)+1			V
Input Low Voltage, ICLK only	V _{IL}	ICLK (pin 1)			(VDD/2)-1	V
Input High Voltage	V _{IH}	OE (pin 7)	2.0			V
Input Low Voltage	V _{IL}	OE (pin 7)			0.8	V
Input High Voltage	V _{IH}	S0, S1	VDD-0.5			V
Input Low Voltage	V _{IL}	S0, S1			0.5	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
IDD Operating Supply Current, 20 MHz crystal		No load, 100M		9		mA
Short Circuit Current		CLK output		±70		mA
On-Chip Pull-up Resistor		Pin 7		270		kΩ
Input Capacitance, S1, S0, and OE		Pins 4, 6, 7		4		pF
Nominal Output Impedance				20		Ω

AC Electrical Characteristics

VDD = 5.0 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

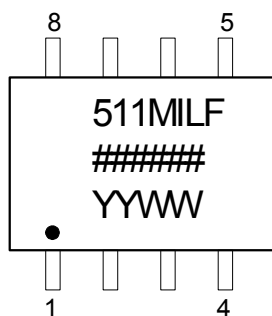
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F _{IN}		5		27	MHz
Input Frequency, clock input	F _{IN}		2		50	MHz
Output Frequency	F _{OUT}	0° C to +70° C	14		200	MHz
		-40° C to +85° C	14		160	MHz
Output Clock Rise Time	t _{OR}	0.8 to 2.0 V, Note 1		1	1.5	ns
Output Clock Fall Time	t _{OF}	2.0 to 8.0 V, Note 1		1	1.5	ns
Output Clock Duty Cycle	t _{OD}	1.5 V, up to 160 MHz	45	49-51	55	%
PLL Bandwidth			10			kHz
Output Enable Time, OE high to output on				50		ns
Output Disable Time, OE low to tri-state				50		ns
Absolute Clock Period Jitter	t _{ja}	Deviation from mean		±70		ps
One Sigma Clock Period Jitter	t _{js}			25		ps

Note 1: Measured with 15 pF load.

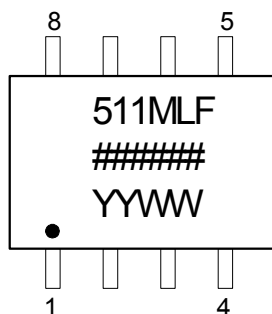
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram (industrial)



Marking Diagram

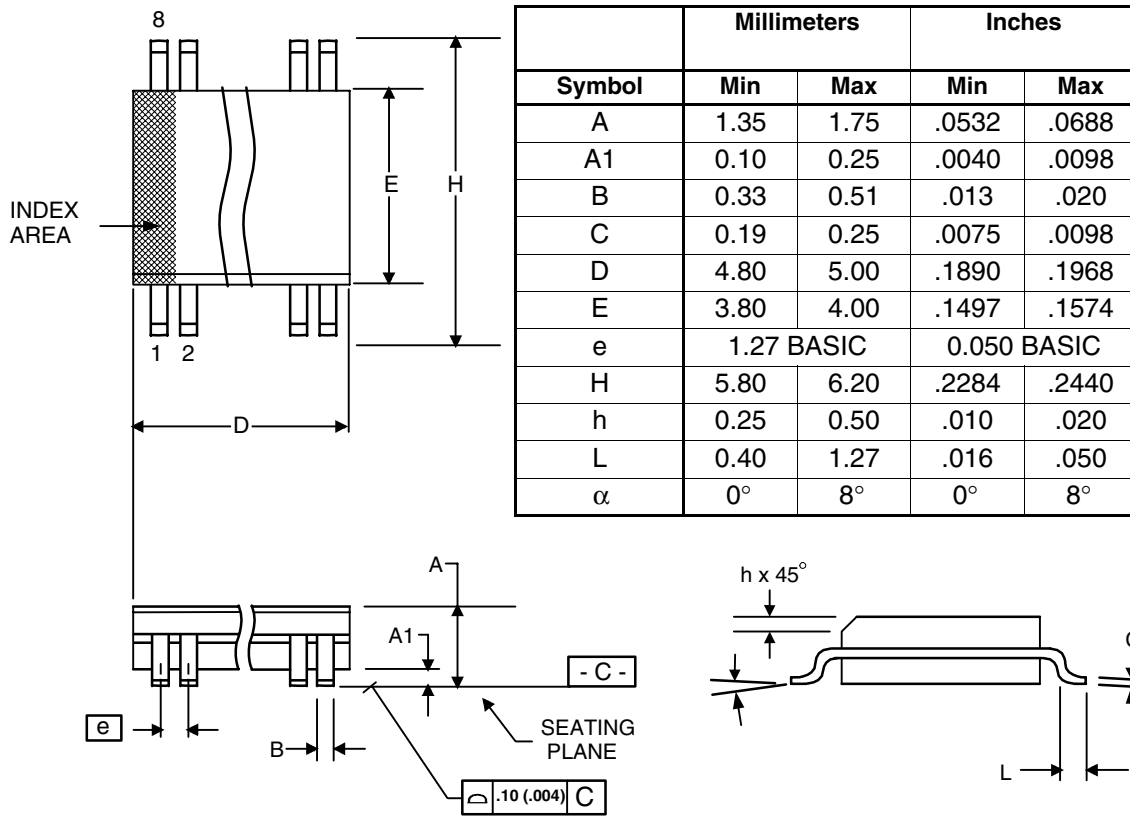


Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "LF" denotes Pb (lead) free package.
4. "I" denotes industrial grade.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
511MLF	511MLF	Tubes	8-pin SOIC	0 to +70° C
511MLFT	511MLF	Tape and Reel	8-pin SOIC	0 to +70° C
511MILF	511MILF	Tubes	8-pin SOIC	-40 to +85° C
511MILFT	511MILF	Tape and Reel	8-pin SOIC	-40 to +85° C
511-DWF	-	Die on uncut, probed wafers		0 to +70° C
511-DPK	-	Tested die in waffle pack		0 to +70° C

“LF” designates Pb (lead) free packaging.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com



www.IDT.com

