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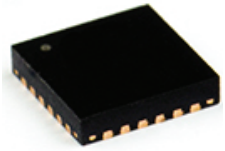
High Performance MEMS Jitter Attenuator



4.0 x 4.0 x 0.85 mm 24-Pin QFN

ABMJB-903

ESD Sensitive

RoHS/RoHS II Compliant

Moisture Sensitivity Level: MSL=1

FEATURES:

- Low power and miniature package programmable jitter attenuator
- Input frequency up to 200MHz
- Output frequency up to 840MHz
- Jitter attenuation 20dB at 3 MHz spur frequency
- Additive phase jitter or phase jitter floor:
  - 55fs for 1.875MHz to 20MHz
  - 251fs for 12MHz to 20MHz
- Single ended CMOS input
- One differential or two single ended outputs. Output logic types supported are LVPECL, LVDS, HCSL and LVCMOS (single ended or differential).
- Operating temperature range from -40°C to +85°C
- 24-pin QFN RoHS-complaint package
- Related devices:
  - ABMJB-902: LVCMOS, period jitter cleaning.

APPLICATIONS:

- 1/10/40/100 Gigabiy Ethernet (GbE)
- SONET/SDH
- PCI-Express
- CPRI/OBSAI wireless base stations
- Fibre Channel
- SAS/SATA
- DIMM

STANDARD SPECIFICATIONS:

Absolute Maximum Ratings (1)

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Voltage (V_{DD}, V_{DDO})			+4.6	V	
Input Voltage (V_{IN})	-0.5		V_{DD} +0.5	V	
Lead Temperature			+260	ºC	Soldering, 20s
Case Temperature			+115	ºC	
Storage Temperature (T_S)	-65		+150	ºC	

Operation Ratings (2)

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Voltage (V_{DD}, V_{DDO})	+2.375		+3.465	V	
Junction Thermal Resistance ($_{JA}$) (3)			50	ºC/W	Still-Air
Ambient Temperature (T_A)	-40		+85	ºC	

DC Electrical Characteristics (4)

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40ºC to +85ºC

Parameters	Min.	Typ.	Max.	Units	Notes
Power Supply Voltage (V_{DD})	+2.375		+3.465	V	
Total Supply Current, V_{DD} + V_{DDO} (I_{DD})		100	120	mA	LVPECL, 321.5MHz, Outputs open
		80	100	mA	HCSL (PCIe), 100MHz, Outputs terminated with 50 to V_{SS}
		70	90	mA	2 x LVCMOS, 125MHz, Outputs open

LVCMOS Inputs (OE, REFIN) DC Electrical Characteristics (4)

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40ºC to +85ºC

Parameters	Min.	Typ.	Max.	Units	Notes
Input High Voltage (V_{IH})	70% V_{DD}		V_{DD}+0.3	V	
Input Low Voltage (V_{IN})	V_{SS}-0.3		30% V_{DD}	V	
Input High Current (I_{IH})			150	µA	V_{DD} = V_{IN} = 3.465V
Input Low Current (I_{IL})	-150			µA	V_{DD} = 3.465V, V_{IN} = 0V

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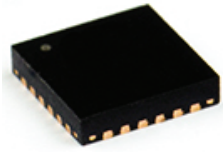


LVDS Output DC Electrical Characteristics (4)

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40°C to +85°C; R_L = 100Ω across Q and /Q

Parameters	Min.	Typ.	Max.	Units	Notes
Differential Output Voltage (V_{OD})	275	350	475	mV	See page 10
V_{OD} Magnitude Change (ΔV_{OD})			40	mV	
Offset Voltage (V_{OS})	1.15	1.25	1.5	V	
V_{OD} Magnitude Change (ΔV_{OS})			50	mV	

HCSL Output DC Electrical Characteristics (4)

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40°C to +85°C; R_L = 50Ω to V_{SS}

Parameters	Min.	Typ.	Max.	Units	Notes
Output High Voltage (V_{OH})	660	700	850	mV	See page 8 & 10
Output Low Voltage (V_{OL})	-150	0	27	mV	See page 8 & 10
Output Voltage Swing (V_{SWING})	630	700	1000	mV	See page 8 & 10

LVPECL Output DC Electrical Characteristics (4)

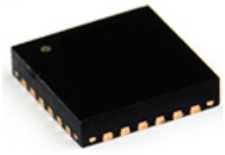
V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5%; T_A = -40°C to +85°C; R_L = 50Ω to V_{DD} - 2V

Parameters	Min.	Typ.	Max.	Units	Notes
Output High Voltage (V_{OH})	V_{DD}-1.145	V_{DD}-0.97	V_{DD}-0.845	V	See page 8 & 9
Output Low Voltage (V_{OL})	V_{DD}-1.945	V_{DD}-1.77	V_{DD}-1.645	V	See page 8 & 9
Output Voltage Swing (V_{SWING})	0.6	0.8	1.0	V	See page 8 & 9

LVCMOS Output DC Electrical Characteristics (4)

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5%; T_A = -40°C to +85°C; R_L = 50Ω to V_{DD}/2

Parameters	Min.	Typ.	Max.	Units	Notes
Output High Voltage (V_{OH})	V_{DD}-0.7			V	See page 8 & 10
Output Low Voltage (V_{OL})			0.6	V	



4.0 x 4.0 x 0.85 mm 24-Pin QFN

LVPECL AC Electrical Characteristics [4, 5, 6, 10]

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40°C to +85°C, unless otherwise noted

Parameters	Min.	Typ.	Max.	Units	Notes
Output Frequency (F_{OUT})	12		840	MHz	
LVPECL Output Rise/Fall Time (T_R/T_F)	80	175	350	ps	20% - 80%
Output Duty Cycle (ODC)	48	50	52	%	F_{OUT} < 350MHz
	45	50	55		F_{OUT} ≥ 350MHz
PLL Lock Time (T_{LOCK})			20	ms	
RMS Phase Jitter @ 156.25MHz with Clean Input Signal (T_{jit}(Ø))		251		fs	Integration range (12kHz to 20MHz)
		55		fs	Integration range (1.875MHz to 20MHz)

LVDS AC Electrical Characteristics [4, 5, 6, 7]

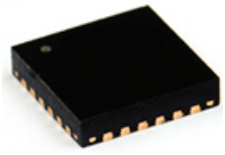
V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40°C to +85°C, unless otherwise noted

Parameters	Min.	Typ.	Max.	Units	Notes
Output Frequency (F_{OUT})	12		840	MHz	
LVDS Output Rise/Fall Time (T_R/T_F)	100	160	400	ps	20% - 80%
Output Duty Cycle (ODC)	48	50	52	%	< 350MHz
	45	50	55		≥350MHz
PLL Lock Time (T_{LOCK})			20	ms	
RMS Phase Jitter @ 156.25MHz (T_{jit}(Ø))		60		fs	Integration range (1.875MHz to 20MHz)

HCSL AC Electrical Characteristics [4, 5, 6, 8]

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40°C to +85°C, unless otherwise noted

Parameters	Min.	Typ.	Max.	Units	Notes
Output Frequency (F_{OUT})	12		840	MHz	
LVDS Output Rise/Fall Time (T_R/T_F)	150	300	450	ps	20% - 80%
Output Duty Cycle (ODC)	48	50	52	%	< 350MHz
	45	50	55		≥350MHz
PLL Lock Time (T_{LOCK})			20	ms	
RMS Phase Jitter @ 100MHz (T_{jit}(Ø))		250		fs	Integration range (12kHz to 20MHz)



LVCMOS AC Electrical Characteristics [4, 5, 6, 9]

V_{DD} = V_{DDO} = 3.3V±5% or 2.5V±5% ; T_A = -40°C to +85°C, unless otherwise noted

Parameters	Min.	Typ.	Max.	Units	Notes
Output Frequency (F_{OUT})	12		250	MHz	
REFIN Frequency (F_{REF})	12		200	MHz	
REFIN Amplitude (V_{REF})	40% V_{DD}		V_{DD} + 0.6	V_{PP}	
Output Rise/Fall Time (T_R/T_F)	100		500	ps	20% - 80%
Output Duty Cycle (ODC)	45	50	55		
PLL Lock Time (T_{LOCK})			20	ms	
RMS Phase Jitter @ 125MHz (T_{jit}(Ø))		55		fs	Integration range (1.875MHz to 20MHz)

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside tis operating ratings.
3. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.
5. See Section 7.1.7 through 7.1.10 for load test circuit examples.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system.
7. Outputs terminated 100Ω between Q and /Q. All unused outputs must be terminated.
8. Output load is 50Ω to V_{SS}.
9. Output load is 50Ω to V_{DD}/2.
10. Output load is 50Ω to V_{DD}-2V.

OPTIONS AND PART IDENTIFICATION:

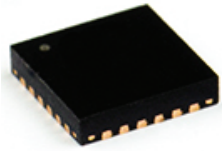
Please refer to the ABMJB-903 Part Number and Configuration Guide for available part numbers and configurations.

High Performance MEMS Jitter Attenuator

ABMJB-903

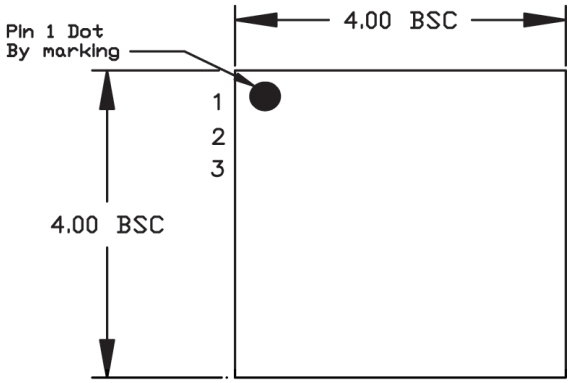
ESD Sensitive

RoHS/RoHS II Compliant

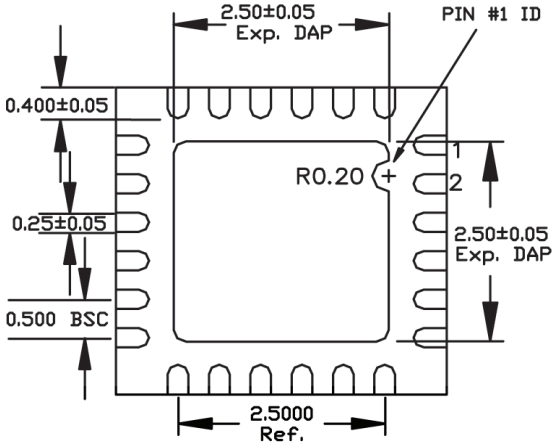


4.0 x 4.0 x 0.85 mm 24-Pin QFN

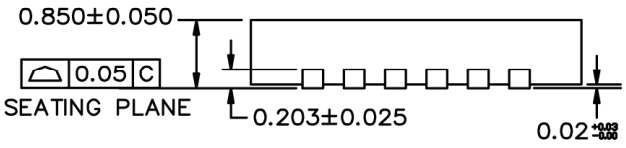
OUTLINE DIMENSION:



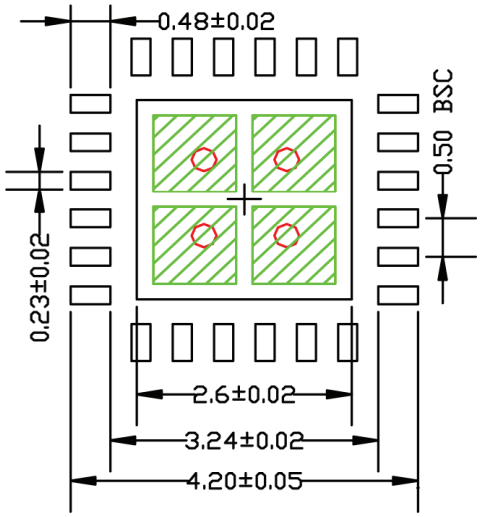
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN

Pin No.	Configuration
22	Q
23	/Q
3	REFIN
12	OE
1, 20	VDD
17, 24	VDDO
2, 8, 13, 14, 15, 21	VSS
4, 5, 7, 9, 11, 16, 18	DNC
6, 10, 19	DNC
ePad	Exposed Pad

Notes:

1. Max package warpage is 0.05mm.
2. Max allowable burr is 0.076mm in all directions.
3. Pin 1is on top and will be laser marked.
4. Red circles in land pattern indicate thermal vias. Size should be 0.30 – 0.35M in diameter and should be connected to GND for max thermal performance.
5. Green rectangles (shaded area) indicate solder stencil opening on exposed pad area. Size should be 1.00 x 1.00 mm in size, 1.20mm pitch.

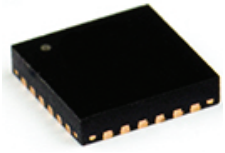
Dimension: mm

High Performance MEMS Jitter Attenuator

ABMJB-903

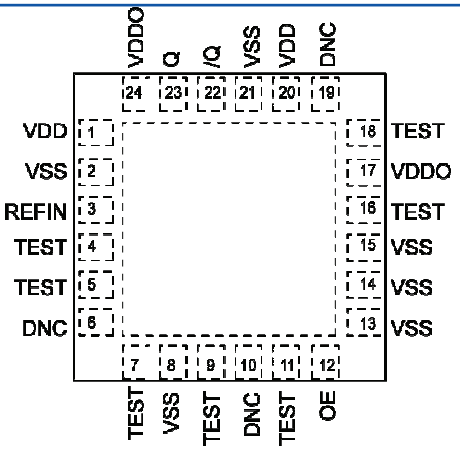
ESD Sensitive

RoHS/RoHS II Compliant



4.0 x 4.0 x 0.85 mm 24-Pin QFN

PIN DESCRIPTION:



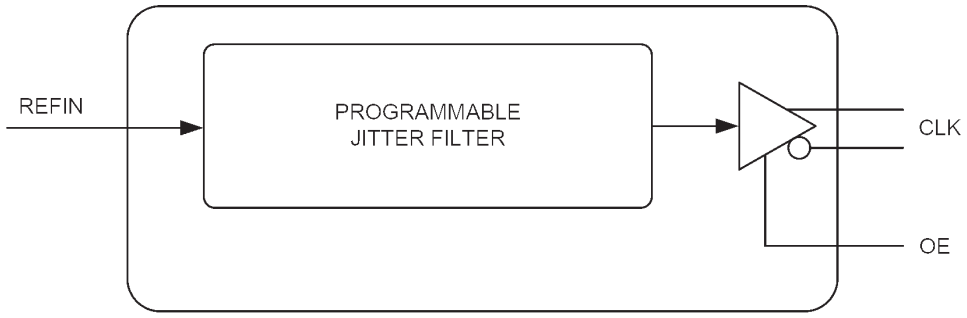
24-Pin QFN package

Pin No.	Pin Name	Pin Type	Pin Level	Function
22	Q	O	Various	Clock output Can be programmed to one of the following logic types: (1) LVPECL, LVDS, HCSL or LVCMOS
23	/Q			
3	REFIN	I, (SE)	Various	Reference clock input Can be programmed to either LVCMOS levels or smaller amplitude signals from other logic types
12	OE	I	LVCMOS	Output enable control input with pull-up (45k)
1, 20	VDD	PWR		Core power supply
17, 24	VDDO	PWR		Output buffer power supply
2, 8, 13, 14, 15, 21	VSS	PWR		Power supply ground
4, 5, 7, 9, 11, 16, 18	DNC			Used for production test Do not connect anything to these pins
6, 10, 19	DNC			Not internally connected. No need to connect anything to these pins.
ePad	Exposed Pad	GND		The center pad must be connected to the ground plane both for electrical ground and thermal relief.

Notes:

1. In case of LVCMOS, the output pair can provide two single-ended LVCMOS outputs.

BLOCK DIAGRAM:



High Performance MEMS Jitter Attenuator

ABMJB-903

ESD Sensitive

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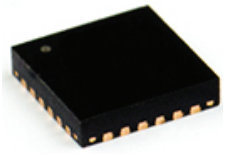

4.0 x 4.0 x 0.85 mm 24-Pin QFN

FUNCTIONAL DESCRIPTION

ABMJB-903 series is a very flexible, advanced programmable jitter filter design for high performance, small form-factor applications. The ABMJB-903 accepts a reference clock input between 12MHz and 200MHz and is capable of producing one differential output up to 840MHz or two single ended outputs up to 250MHz. The most common configuration will be with the same input and output frequency but this flexible design also allows frequency translation from one frequency to another frequency, as long as both frequencies are within the specified ranges for input and output.

Jitter Attenuation

Typically the jitter attenuation settings will be optimized for one particular input and output frequency. Customization of attenuation properties is possible.

The lowest possible output phase jitter, or phase jitter floor, is 251fs for the 12kHz to 20MHz integration range and 55fs for the Gigabit Ethernet integration range of 1.875MHz to 20MHz. The ABMLB-903 excels at attenuating deterministic jitter that presents itself as spurs in the phase noise plot above 1MHz.

Clock Output

The output pins Q and /Q make a differential output that can be programmed to several different logic types: LVPECL, LVDS, HCSL or LVCMOS. In the case of LVCMOS, there are three possible configurations:

1. One single-ended output with the complementary pin disabled to a high impedance.
2. Two single-ended, in-phase outputs.
3. A differential output with opposite phases at the two output pins

Output Frequency

The most common configuration is where the output frequency is the same as the input frequency. However, frequency translations are possible. The input frequency upper limit is 200MHz, but the output can go up to 840MHz.

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 45kΩ pull-up resistor giving a default condition of logic “1” that enables the output(s).

Reference (Noisy) Clock Input (REFIN)

The input requires a single-ended CMOS signal. The frequency range for the input is 12MHz to 200MHz.

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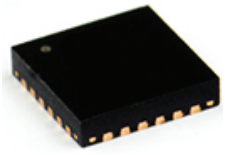
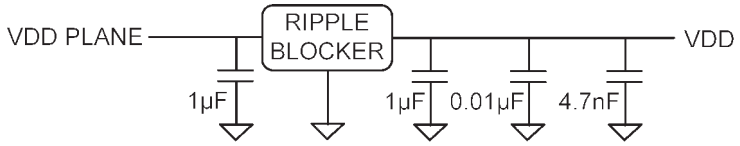


4.0 x 4.0 x 0.85 mm 24-Pin QFN

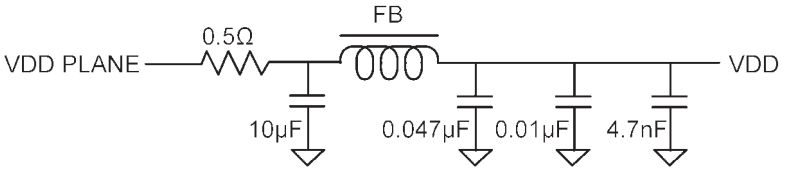
APPLICATION INFORMATION

Power Supply Filtering Recommendations

Preferred filter, using Micrel's MIC94300 or MIC94310 Ripple Blocker™:



Alternative, traditional filter, using a ferrite bead:



Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the ABMJB-903.

The impedance value of the ferrite bead (FB) needs to be between 240 and 600 with a saturation current ≥150mA.

VDDO pins connect directly to the VDD plane. All VDD pins on the ABMJB-903 connect to VDD after the power supply filter.

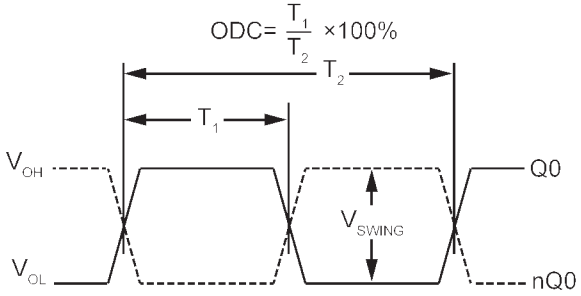
Output Traces

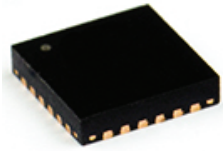
Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 resistor in series with the output, as close as possible to the output pin, and start a 50 trace on the other side of the resistor.

For differential traces, you can either use a differential design or two separate 50 traces. For EMI reasons, it is better to use a differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

Duty Cycle Timing

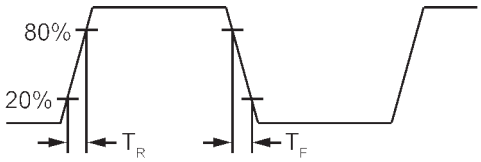




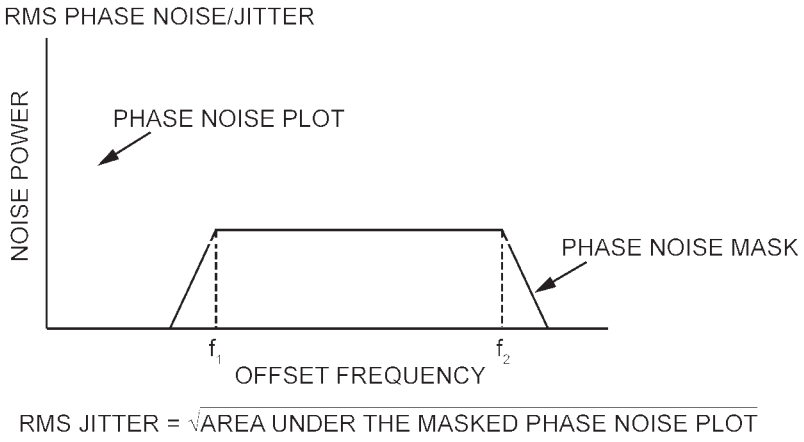
4.0 x 4.0 x 0.85 mm 24-Pin QFN

APPLICATION INFORMATION

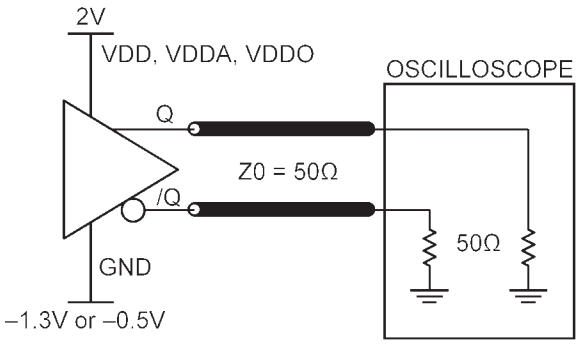
All Outputs Rise/Fall Time

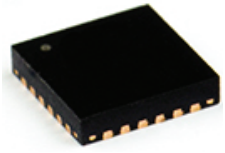


RMS Phase Noise Jitter



LVPECL Output Load and Test Circuit

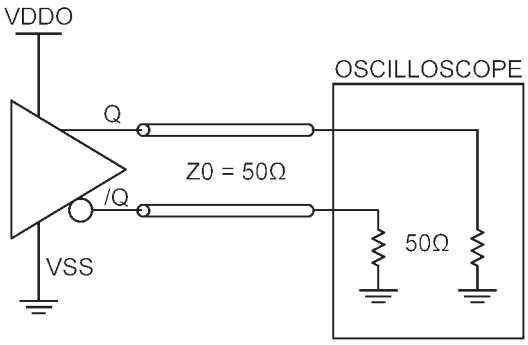




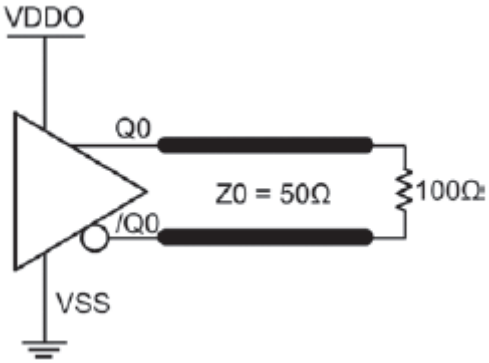
4.0 x 4.0 x 0.85 mm 24-Pin QFN

APPLICATION INFORMATION

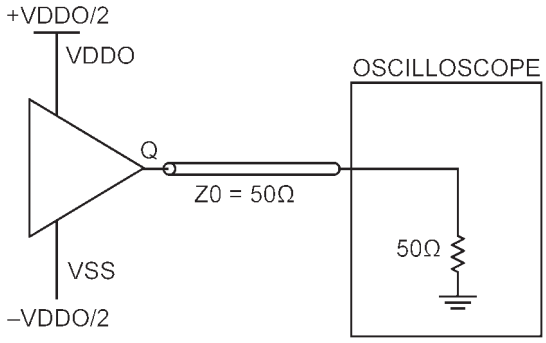
HCSL Output Load and Test Circuit



LVDS Output Load and Test Circuit



LVCMOS Output Load and Test Circuit



2 Faraday, Suite# B | Irvine | CA 92618 **Revised: 03.26.15**
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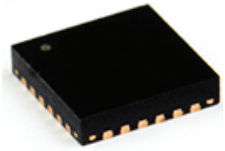
High Performance MEMS Jitter Attenuator

ABMJB-903

ESD Sensitive

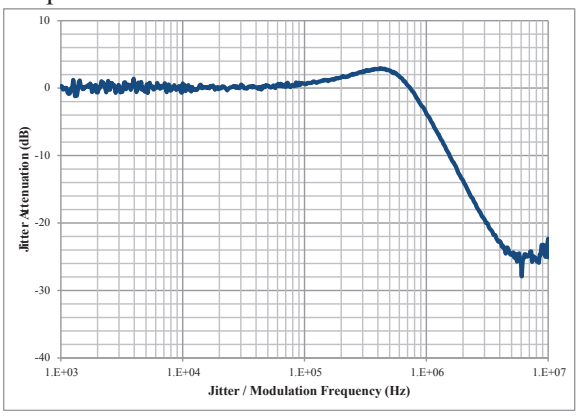
RoHS/RoHS II Compliant



4.0 x 4.0 x 0.85 mm 24-Pin QFN

JITTER ATTENUATION PERFORMANCE

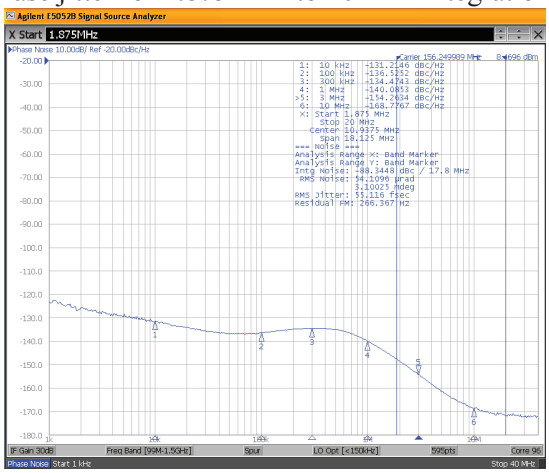
The jitter attenuating frequency response was measured at 156.25MHz.



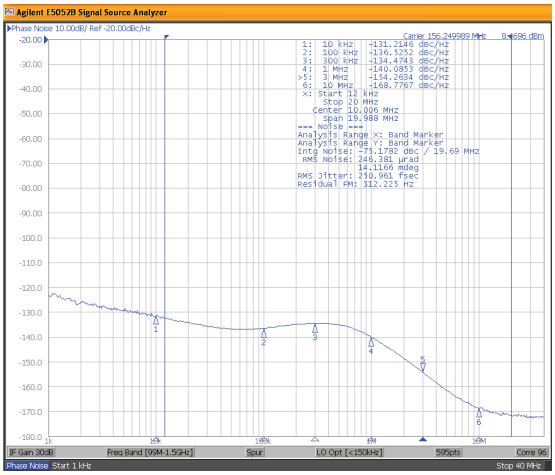
The jitter attenuation works like a low-pass filter for frequency modulated signals or noise. The bandwidth for this low pass filter is 500kHz with a 12dB/octave slope above 500kHz. At about 6MHz the noise floor of this measurement is reached but in reality, the attenuation continues with the 12dB/octave slope.

Phase noise performance with a clean input clock:

156.25MHz with 55fs$_{RMS}$ for phase jitter for 1.875MHz to 20MHz integration range



156.25MHz with 251fs$_{RMS}$ for phase jitter for 12kHz to 20MHz integration range



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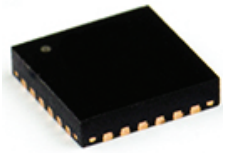
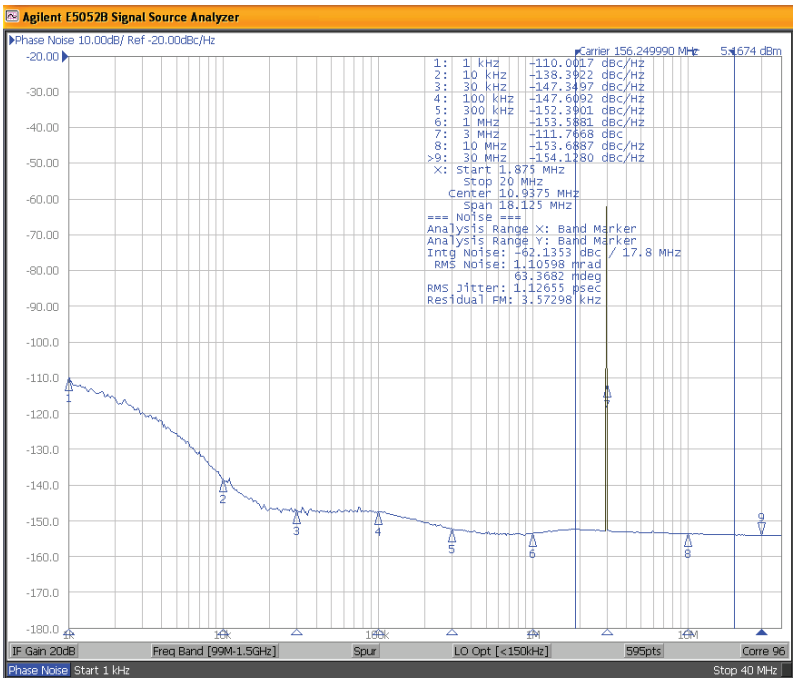


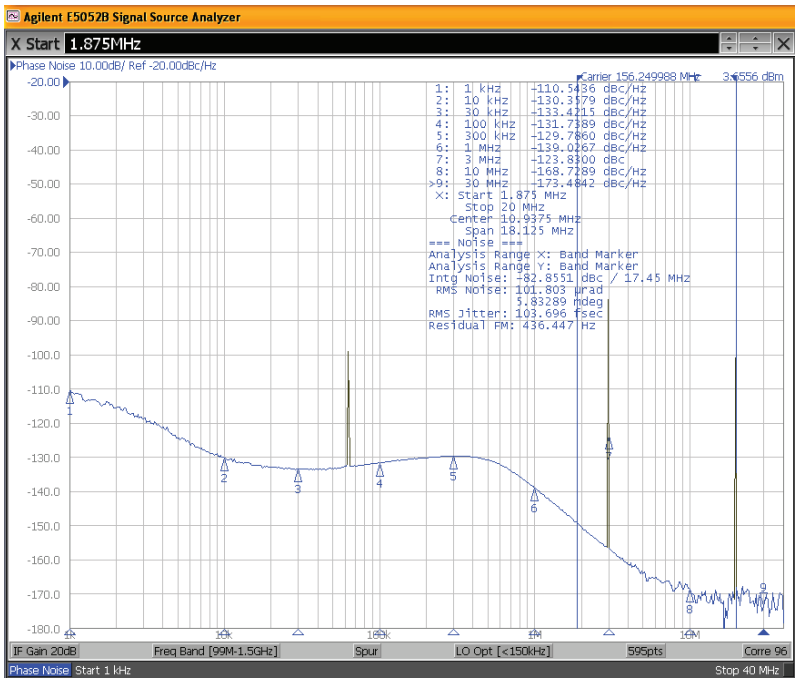
4.0 x 4.0 x 0.85 mm 24-Pin QFN

JITTER ATTENUATION PERFORMANCE

Example: 156.25MHz input test clock with bad phase jitter caused by a 3MHz spur – 1.1ps$_{RMS}$ of phase jitter for 1.875MHz to 20MHz integration range



Output Clock from ABMJB-903: The 3MHz spur is attenuated by 20dB, resulting in a phase jitter reduction from 1.1ps to 0.10ps for 1.875MHz to 20MHz integration range

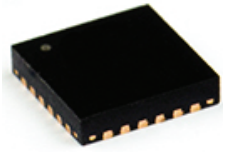


High Performance MEMS Jitter Attenuator

ABMJB-903

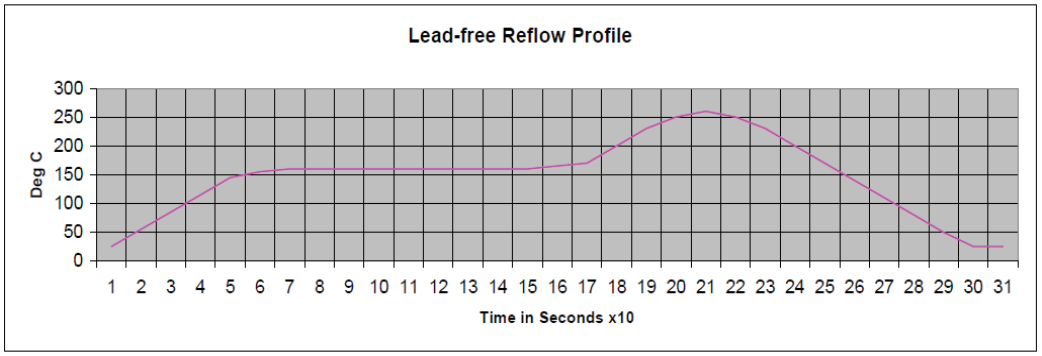
ESD Sensitive

RoHS/RoHS II Compliant



4.0 x 4.0 x 0.85 mm 24-Pin QFN

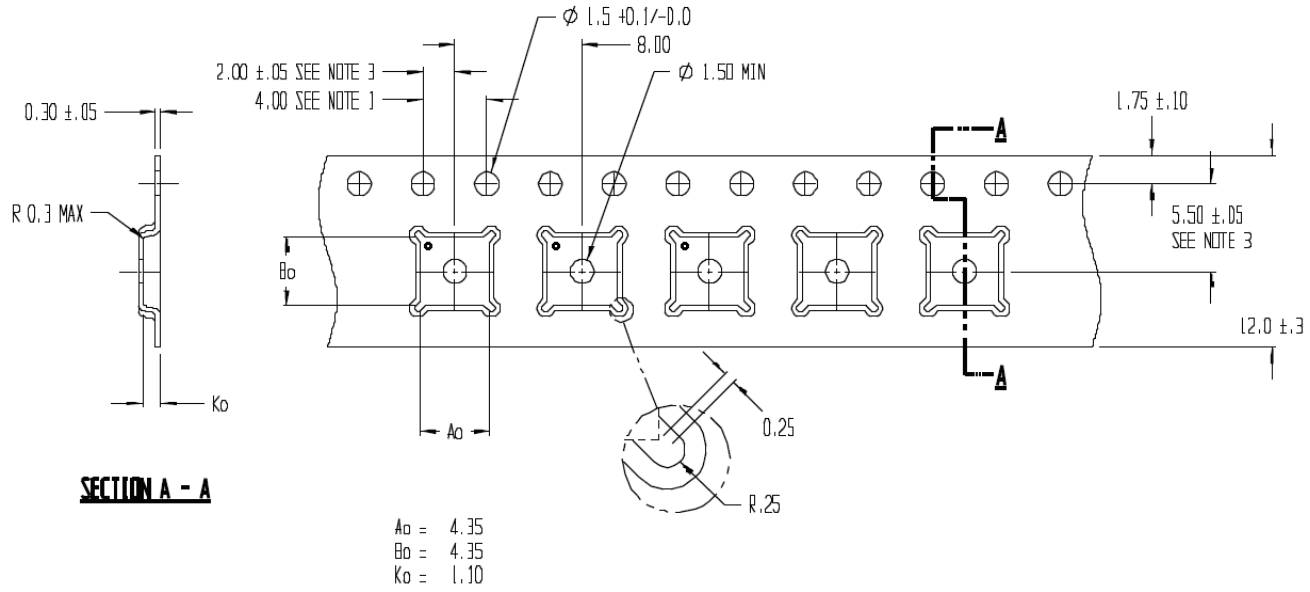
REFLOW PROFILE:



Parameters	Specifications
Average Ramp-up Rate	3℃ /second max.
Pre-Heat Temp 150 – 200℃	60 – 180 second
Temp > 217℃	60 – 150 second
Time @ Peak Temperature	20 – 40 second
Peak Temperature	260℃ + 0℃ / -5℃
Ramp-down Rate	-6℃ / second max.
Time 25℃ to Peak Temp.	8 minutes max.

TAPE & REEL:

Packaging:
T: 1000pcs/reel
T5: 500pcs/reel



Dimensions: mm